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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	SH2A
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f72375adfp-v0

Classification	Symbol	I/O	Name	Function
I/O ports	PA18 to PA15, PA9 to PA6, PA1, PA0	I/O	General port	Ten general input/output port pins.
	PB21 to PB16, PB4 to PB0*2	I/O	General port	Eleven general input/output port pins.
	PC15 to PC0	I/O	General port	Sixteen general input/output port pins.
	PD15 to PD0	I/O	General port	Sixteen general input/output port pins.
	PE15 to PE0	I/O	General port	Sixteen general input/output port pins.
	PF15 to PF0	Input	General port	Sixteen general input port pins.
User debugging interface (H-UDI)	TCK	Input	Test clock	Test-clock input pin.
	TMS	Input	Test mode select	Test-mode select signal input pin.
	TDI	Input	Test data input	Serial input pin for instructions and data.
	TDO	Output	Test data output	Serial output pin for instructions and data.
	$\overline{\text{TRST}}$	Input	Test reset	Initialization-signal input pin. Input a low level when not using the H-UDI.
Advanced user debugger (AUD)	AUDATA3 to AUDATA0	Output	AUD data	Branch destination/source address output pin
	AUDCK	Output	AUD clock	Sync clock output pin
	$\overline{\text{AUDSYNC}}$	Output	AUD sync signal	Data start-position acknowledge-signal output pin

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PFC[2:0]	101	R/W	Peripheral Clock (Pϕ) Frequency Division Ratio These bits specify the frequency division ratio of the peripheral clock. Settings must be such that the output clock signal is at a frequency no higher than 40 MHz and no higher than that of Bϕ in the case of the SH7239A and SH7237A, and no higher than 50 MHz and no higher than that of Bϕ in the case of the SH7239B and SH7237B. 000: × 1 001: × 1/2 010: Setting prohibited 011: × 1/4 100: Setting prohibited 101: × 1/8 Others: Setting prohibited

Table 6.4 Interrupt Exception Handling Vectors and Priorities

Interrupt Source Number		Interrupt Vector: Vector	Interrupt Vector: Vector Table Address Offset	Interrupt Priority (Initial Value)	Corresponding IPR (Bit)	IPR Setting Unit Internal Priority	Default Priority
NMI		11	H'0000002C to H'0000002F	16	—	—	High
UBC		12	H'00000030 to H'00000033	15	—	—	
H-UDI		14	H'00000038 to H'0000003B	15	—	—	
IRQ	IRQ0	64	H'00000100 to H'00000103	0 to 15 (0)	IPR01 (15 to 12)	—	
	IRQ1	65	H'00000104 to H'00000107	0 to 15 (0)	IPR01 (11 to 8)	—	
	IRQ2	66	H'00000108 to H'0000010B	0 to 15 (0)	IPR01 (7 to 4)	—	
	IRQ3	67	H'0000010C to H'0000010F	0 to 15 (0)	IPR01 (3 to 0)	—	
	IRQ4	68	H'00000110 to H'00000113	0 to 15 (0)	IPR02 (15 to 12)	—	
	IRQ5	69	H'00000114 to H'00000117	0 to 15 (0)	IPR02 (11 to 8)	—	
	IRQ6	70	H'00000118 to H'0000011B	0 to 15 (0)	IPR02 (7 to 4)	—	
ROM, FLD	FIFE	91	H'0000016C to H'0000016F	15	—	—	
ADC	ADI0	92	H'00000170 to H'00000173	0 to 15 (0)	IPR05 (7 to 4)	—	
	ADI1	96	H'00000180 to H'00000183	0 to 15 (0)	IPR05 (3 to 0)	—	
	ADI2	100	H'00000190 to H'00000193	0 to 15 (0)	IPR17 (7 to 4)	—	Low

8.5.10 DTC Activation Priority Order

If multiple DTC activation requests are generated while the DTC is inactive, whether to start the DTC transfer from the first activation request* or according to the DTC activation priority can be selected through the DTPR bit setting in the bus function extending register (BSCEHR). If multiple activation requests are generated while the DTC is active, transfer is performed according to the DTC activation priority. Figure 8.17 shows an example of DTC activation according to the priority.

Note: * When one DTC-activation request is generated before another, transfer starts with the first request. When an activation request with a higher priority is generated before a pending DTC request is accepted, transfer starts for the request with higher priority. Timing of DTC request generation varies according to the operating state of internal buses.

Table 11.18 TIORH_4 (Channel 4)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_4 Function**	**TIOC4B Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

(1) Example of PWM Mode Setting Procedure

Figure 11.25 shows an example of the PWM mode setting procedure.

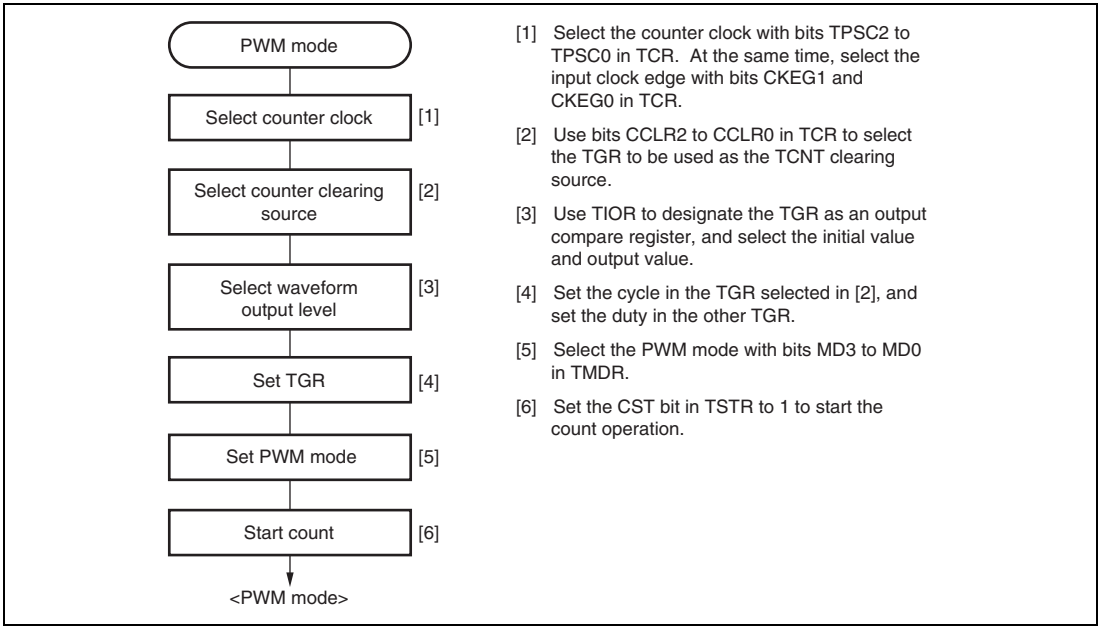


Figure 11.25 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 11.26 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the period, and the values set in the TGRB registers are used as the duty levels.

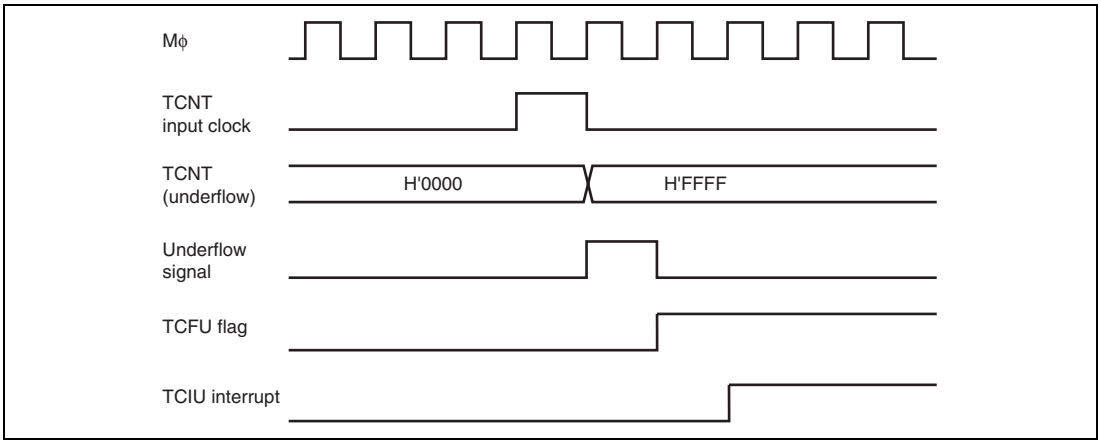


Figure 11.114 TCIU Interrupt Setting Timing

(4) Status Flag Clearing Timing

After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DMAC is activated, the flag is cleared automatically. Figures 11.115 and 116 show the timing for status flag clearing by the CPU, and figure 11.117 shows the timing for status flag clearing by the DMAC.

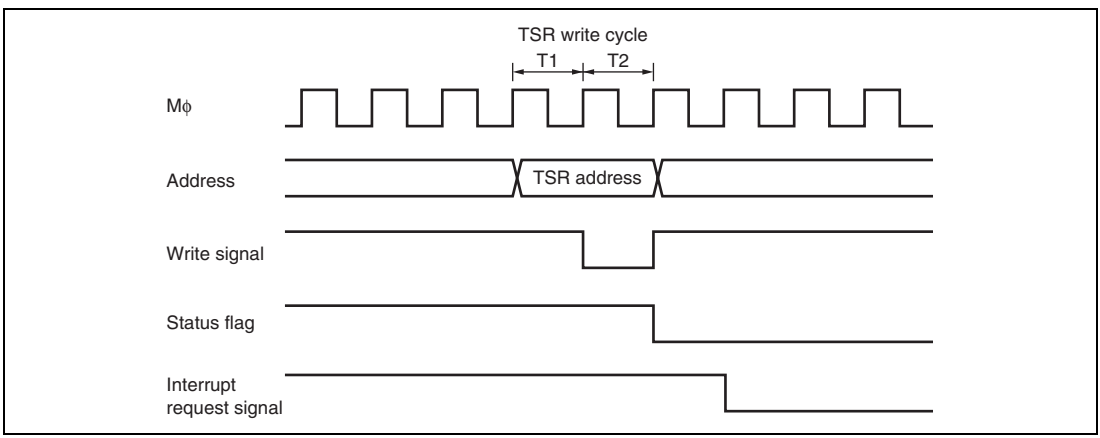


Figure 11.115 Timing for Status Flag Clearing by CPU (Channels 0 to 4)

Table 16.3 SCSMR Settings

		SCSMR Settings	
n	**Clock Source**	**CKS1**	**CKS0**
0	Pϕ	0	0
1	Pϕ/4	0	1
2	Pϕ/16	1	0
3	Pϕ/64	1	1

Note: The bit rate error in asynchronous is given by the following formula:

- When the ABCS bit in serial extended mode register (SCSEMR) is 0

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

- When the ABCS bit in serial extended mode register (SCSEMR) is 1

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 32 \times 2^{2n-1}} - 1 \right\} \times 100$$

(1) Transmit/Receive Formats

Table 16.16 shows the transfer formats that can be selected in asynchronous mode. Any of 12 transfer formats can be selected according to the SCSMR settings.

Table 16.16 Serial Transfer Formats (Asynchronous Mode)

SCSMR Settings				Serial Transfer Format and Frame Length											
CHR	PE	MP	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	0	S	8-bit data								STOP		
0	0	0	1	S	8-bit data								STOP	STOP	
0	1	0	0	S	8-bit data								P	STOP	
0	1	0	1	S	8-bit data								P	STOP	STOP
1	0	0	0	S	7-bit data							STOP			
1	0	0	1	S	7-bit data							STOP	STOP		
1	1	0	0	S	7-bit data							P	STOP		
1	1	0	1	S	7-bit data							P	STOP	STOP	
0	x	1	0	S	8-bit data								MPB	STOP	
0	x	1	1	S	8-bit data								MPB	STOP	STOP
1	x	1	0	S	7-bit data							MPB	STOP		
1	x	1	1	S	7-bit data							MPB	STOP	STOP	

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit
x: Don't care

16.7.6 Note on Using DTC

When the external clock source is used for the clock for synchronization, input the external clock after waiting for five or more cycles of the peripheral operating clock after SCTDR is modified through the DTC. If a transmit clock is input within four cycles after SCTDR is modified, a malfunction may occur (figure 16.23).

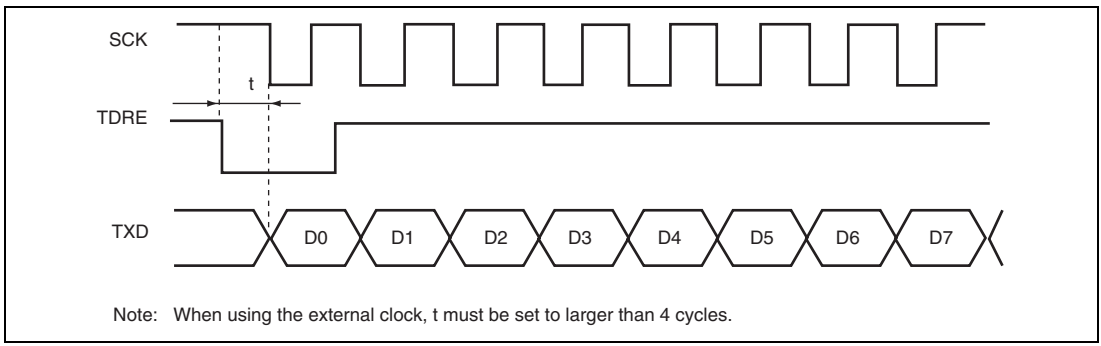


Figure 16.23 Example of Clock Synchronous Transfer Using DTC

When data is written to SCTDR by activating the DTC by a TXI interrupt, the TEND flag value becomes undefined. In this case, do not use the TEND flag as the transmit end flag.

16.7.7 Note on Using External Clock in Clock Synchronous Mode

TE and RE must be set to 1 after waiting for four or more cycles of the peripheral operating clock after the SCK external clock is changed from 0 to 1.

TE and RE must be set to 1 only while the SCK external clock is 1.

16.7.8 Module Standby Mode Setting

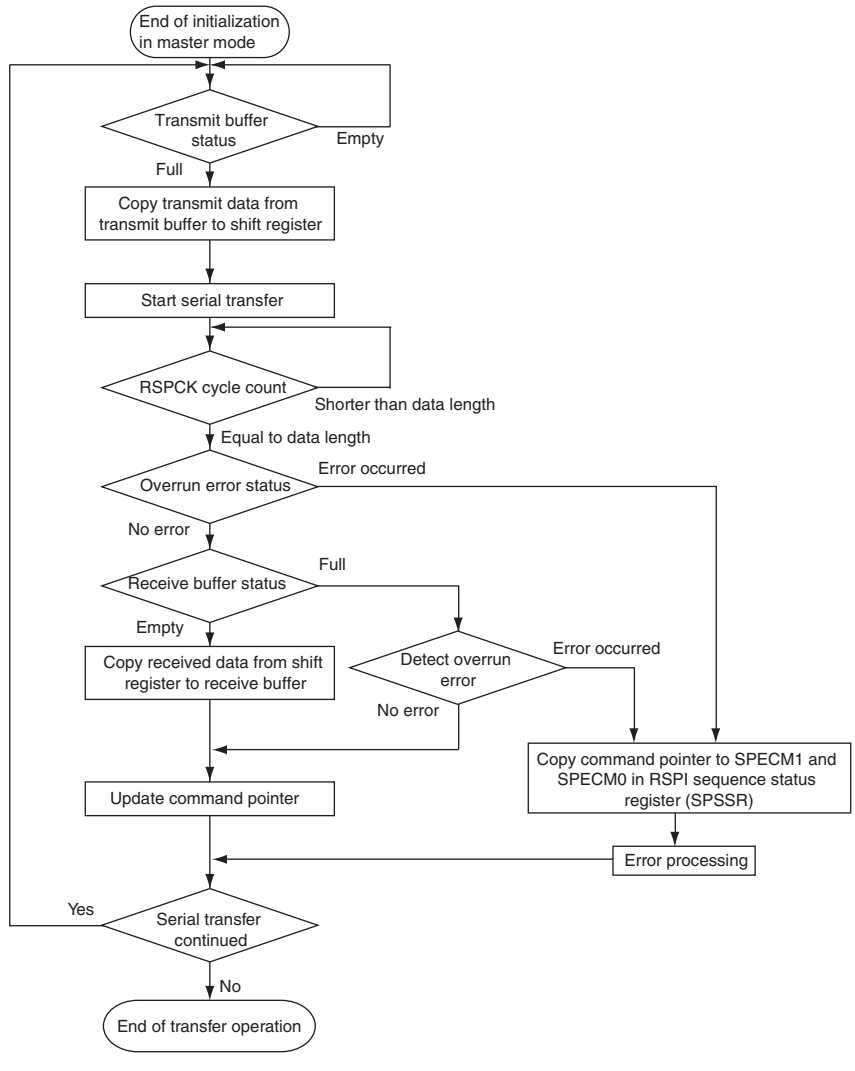
SCI operation can be disabled or enabled using the standby control register. The initial setting is for SCI operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 26, Power-Down Modes.

16.7.9 Note for RXD Pin State on Setting RE Bit

To use the SCI, be sure to drive the RXD pin state high before setting the RE bit to 1. If the RE bit is set to 1 with the RXD pin being low, reception may be started.

(2-9) Transfer Operation Flowchart

Figure 18.24 shows an example of transfer operation flowchart for using the RSPI in master mode during SPI operation.



Note: When the SSL0 input signal is asserted in multi-master mode, the RSPI detects a mode fault error irrespective of the hardware status. When detecting the error, the RSPI copies the command pointer to the SPECM[1:0] bits in the RSPI sequence status register (SPSSR).

Figure 18.24 Example of Transfer Operation Flowchart in Master Mode

21.1.3 Port A Pull-Up MOS Control Registers H and L (PAPCRH and PAPCRL)

PAPCRH and PAPCRL control on and off of the input pull-up MOS of port A in bits.

(1) Port A Pull-Up MOS Control Register H (PAPCRH)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	PA18 PCR	PA17 PCR	PA16 PCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	PA18PCR	0	R/W	The corresponding input pull-up MOS turns on when one of these bits is set to 1.
1	PA17PCR	0	R/W	
0	PA16PCR	0	R/W	

22.4.1 Register Descriptions

Port D has the following registers. See section 28, List of Registers for details on the register address and states in each operating mode.

Table 22.7 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port D data register L	PDDRL	R/W	H'0000	H'FFFE3982	8, 16
Port D port register L	PDPRL	R	—	H'FFFE399E	8, 16

22.4.2 Port D Data Register L (PDDRL)

PDDRL is a 16-bit readable/writable registers that stores port D data. When a pin function is general output, if a value is written to PDDRL, the value is output directly from the pin, and if PDDRL is read, the register value is returned directly regardless of the pin state. When a pin function is general input, if PDDRL is read, the pin state, not the register value, is returned directly. If a value is written to PDDRL, although that value is written into PDDRL, it does not affect the pin state.

Table 22.8 summarizes read/write operations of port D data register.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PD15 DR	PD14 DR	PD13 DR	PD12 DR	PD11 DR	PD10 DR	PD9 DR	PD8 DR	PD7 DR	PD6 DR	PD5 DR	PD4 DR	PD3 DR	PD2 DR	PD1 DR	PD0 DR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ROMAE	0	R/(W)*	• An access command is issued to an address other than ROM program/erase addresses H'80800000 to H'80807FFF while the user boot MAT is selected. [Clearing condition] • A 0 is written to this bit after reading a 1 from the ROMAE bit.
6, 5	—	All 0	R	Reserved The write value should always be 0; otherwise normal operation cannot be guaranteed.
4	CMDLK	0	R	FCU Command Lock Indicates whether the FCU is in command-locked state (see section 23.9.3, Error Protection). 0: The FCU is not in a command-locked state 1: The FCU is in a command-locked state [Setting condition] • The FCU detects an error and enters command-locked state. [Clearing condition] • The FCU completes the status-clear command processing while FASTAT is H'10.
3	EEPAE	0	R/(W)*	FLD Access Error Refer to section 24, Data Flash (FLD).
2	EEPIFE	0	R/(W)*	FLD Instruction Fetch Error Refer to section 24, Data Flash (FLD).
1	EEPRPE	0	R/(W)*	FLD Read Protect Error Refer to section 24, Data Flash (FLD).
0	EEPWPE	0	R/(W)*	FLD Program/Erase Protect Error Refer to section 24, Data Flash (FLD).

Note: * Only 0 can be written to clear the flag after 1 is read.

26.3.5 Standby Control Register 5 (STBCR5)

STBCR5 is an 8-bit readable/writable register that controls the operation of modules in power-down modes. STBCR5 is initialized to H'FF by a power-on reset but retains its previous value by a manual reset or in software standby mode. Only byte access is possible.

Bit:	7	6	5	4	3	2	1	0
	MSTP57	MSTP56	MSTP55	-	-	MSTP52	MSTP51	MSTP50
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	MSTP57	1	R/W	Module Stop 57 When the MSTP57 bit is set to 1, the supply of the clock to the SCI0 is halted. 0: SCI0 runs. 1: Clock supply to SCI0 halted.
6	MSTP56	1	R/W	Module Stop 56 When the MSTP56 bit is set to 1, the supply of the clock to the SCI1 is halted. 0: SCI1 runs. 1: Clock supply to SCI1 halted.
5	MSTP55	1	R/W	Module Stop 55 When the MSTP55 bit is set to 1, the supply of the clock to the SCI2 is halted. 0: SCI2 runs. 1: Clock supply to SCI2 halted.
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
MTU2	Timer general register W_5	TGRW_5	16	H'FFFE40A2	16
	Timer compare match clear register	TCNTCMPCLR	8	H'FFFE40B6	8
	Timer start register	TSTR	8	H'FFFE4280	8, 16
	Timer synchronous register	TSYR	8	H'FFFE4281	8
	Timer counter synchronous start register	TCSYSTR	8	H'FFFE4282	8
	Timer read/write enable register	TRWER	8	H'FFFE4284	8
	Timer output master enable register	TOER	8	H'FFFE420A	8
	Timer output control register 1	TOCR1	8	H'FFFE420E	8, 16
	Timer output control register 2	TOCR2	8	H'FFFE420F	8
	Timer gate control register	TGCR	8	H'FFFE420D	8
	Timer cycle control register	TCDR	16	H'FFFE4214	16, 32
	Timer dead time data register	TDDR	16	H'FFFE4216	16
	Timer subcounter	TCNTS	16	H'FFFE4220	16, 32
	Timer cycle buffer register	TCBR	16	H'FFFE4222	16
	Timer interrupt skipping set register	TITCR	8	H'FFFE4230	8, 16
	Timer interrupt skipping counter	TITCNT	8	H'FFFE4231	8
	Timer buffer transfer set register	TBTER	8	H'FFFE4232	8
	Timer dead time enable register	TDER	8	H'FFFE4234	8
	Timer waveform control register	TWCR	8	H'FFFE4260	8
	Timer output level buffer register	TOLBR	8	H'FFFE4236	8
MTU2S	Timer control register_3S	TCR_3S	8	H'FFFE4A00	8, 16, 32
	Timer mode register_3S	TMDR_3S	8	H'FFFE4A02	8, 16
	Timer I/O control register H_3S	TIORH_3S	8	H'FFFE4A04	8, 16, 32
	Timer I/O control register L_3S	TIORL_3S	8	H'FFFE4A05	8
	Timer interrupt enable register_3S	TIER_3S	8	H'FFFE4A08	8, 16
	Timer status register_3S	TSR_3S	8	H'FFFE4A2C	8, 16
	Timer counter_3S	TCNT_3S	16	H'FFFE4A10	16, 32
	Timer general register A_3S	TGRA_3S	16	H'FFFE4A18	16, 32
	Timer general register B_3S	TGRB_3S	16	H'FFFE4A1A	16
	Timer general register C_3S	TGRC_3S	16	H'FFFE4A24	16, 32

Module Name	Register	Power-on Reset	Manual Reset	Software Standby	Module Standby	Sleep
SCIF	SCFDR_3	Initialized	Retained	Retained	Retained	Retained
	SCSPTR_3	Initialized*[5]	Retained	Retained	Retained	Retained
	SCLSR_3	Initialized	Retained	Retained	Retained	Retained
	SCSEMR_3	Initialized	Retained	Retained	Retained	Retained
RSPI	SPCR	Initialized	Retained	Retained	Initialized	Retained
	SSLP	Initialized	Retained	Retained	Initialized	Retained
	SPPCR	Initialized	Retained	Retained	Initialized	Retained
	SPSR	Initialized	Retained	Retained	Initialized	Retained
	SPDR	Initialized	Retained	Retained	Initialized	Retained
	SPSCR	Initialized	Retained	Retained	Initialized	Retained
	SPSSR	Initialized	Retained	Retained	Initialized	Retained
	SPBR	Initialized	Retained	Retained	Initialized	Retained
	SPDCR	Initialized	Retained	Retained	Initialized	Retained
	SPCKD	Initialized	Retained	Retained	Initialized	Retained
	SSLND	Initialized	Retained	Retained	Initialized	Retained
	SPND	Initialized	Retained	Retained	Initialized	Retained
	SPCMD0	Initialized	Retained	Retained	Initialized	Retained
	SPCMD1	Initialized	Retained	Retained	Initialized	Retained
	SPCMD2	Initialized	Retained	Retained	Initialized	Retained
	SPCMD3	Initialized	Retained	Retained	Initialized	Retained

Table 29.5 DC Characteristics (SH7239B and SH7237B)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	$\overline{\text{RES}}$, $\overline{\text{MRES}}$, NMI, MD0, FWE, $\overline{\text{ASEMD0}}$, $\overline{\text{TRST}}$, EXTAL	V_{IH}	VCC – 0.7	—	VCC + 0.3	V	VCC = 4.5 to 5.5 V
	Analog ports		2.2	—	AVCC + 0.3	V	AVCC = 4.5 to 5.5 V
	Input pins other than above (excluding Schmitt pins)		2.2	—	VCC + 0.3		VCC = 4.5 to 5.5 V
Input low voltage	$\overline{\text{RES}}$, $\overline{\text{MRES}}$, NMI, MD0, FWE, $\overline{\text{ASEMD0}}$, $\overline{\text{TRST}}$, EXTAL	V_{IL}	–0.3	—	0.5	V	VCC = 4.5 to 5.5 V
	Input pins other than above (excluding Schmitt pins)		–0.3	—	0.8	V	

29.5 Flash Memory Characteristics

Table 29.26 ROM (Flash Memory for Code Storage) Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	Pϕ = 50 MHz, 40 MHz $N_{PEC} \leq 100$
	8 Kbytes	t_{P8K}	—	45	100	ms	
	256 bytes	t_{P256}	—	2.4	14.4	ms	Pϕ = 50 MHz, 40 MHZ $N_{PEC} > 100$
	8 Kbytes	t_{P8K}	—	54	120	ms	
Erase time	8 Kbytes	t_{E8K}	—	50	120	ms	Pϕ = 50 MHz, 40 MHz $N_{PEC} \leq 100$
	64 Kbytes	t_{E64K}	—	400	875	ms	
	128 Kbytes	t_{E128K}	—	800	1750	ms	
	8 Kbytes	t_{E8K}	—	60	144	ms	Pϕ = 50 MHz, 40 MHz $N_{PEC} > 100$
	64 Kbytes	t_{E64K}		480	1050	ms	
	128 Kbytes	t_{E128K}		960	2100	ms	
Rewrite/erase cycle*1		N_{PEC}	1000*2	—	—	Times	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 29.37
First suspend delay time during erasing (in suspension priority mode)		t_{SESD1}	—	—	220 (Pϕ = 20 MHz), 130 (Pϕ = 40 MHz), 120 (Pϕ = 50 MHz)	µs	Pϕ = 50 MHz, 40 MHz
Second suspend delay time during erasing (in suspension priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	
Resume command interval time		t_{RESI}	1.7	—	—	ms	
Data hold time*3		t_{DDRP}	10	—	—	Years	

Notes: 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)