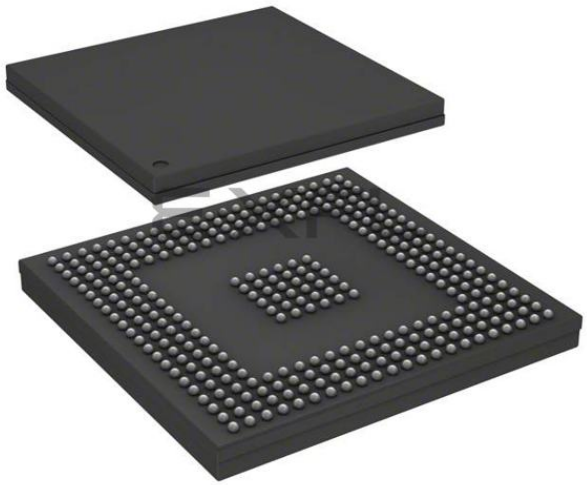

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Peripherals	DMA, POR, PWM, WDT
Number of I/O	220
Program Memory Size	1.5KB (1.5K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5553mvz132

Table 2. Absolute Maximum Ratings [1] (continued)

Spec	Characteristic	Symbol	Min.	Max.	Unit
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} - V_{DDA}$	$-V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C
28	Maximum solder temperature [11] Lead free (Pb-free) Leaded (SnPb)	T_{SDR}	 — —	 260.0 245.0	°C
29	Moisture sensitivity level [12]	MSL	—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond any of the listed maxima can affect device reliability or cause permanent damage to the device.

2 1.5 V ± 10% for proper operation. This parameter is specified at a maximum junction temperature of 150 °C.

3 All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

4 AC signal overshoot and undershoot of up to ± 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

5 Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than –0.6 V on SINB during the internal power-on reset (POR) state.

6 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

7 Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

8 Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

9 Total injection current for all analog input pins must not exceed 15 mA.

10 Lifetime operation at these specification limits is not guaranteed.

11 Moisture sensitivity profile per IPC/JEDEC J-STD-020D.

12 Moisture sensitivity per JEDEC test method A112.

3.2 Thermal Characteristics

The shaded rows in the following table indicate information specific to a four-layer board.

Table 3. MPC5553 Thermal Characteristics

Spec	MPC5553 Thermal Characteristic	Symbol	Packages			Unit
			208 MAPBGA	324 PBGA	416 PBGA	
1	Junction to ambient, natural convection (one-layer board) [1, 2]	$R_{\theta JA}$	41	30	29	°C/W
2	Junction to ambient, natural convection [1, 3] (four-layer board 2s2p)	$R_{\theta JA}$	25	21	21	°C/W
3	Junction to ambient (@200 ft./min., one-layer board)	$R_{\theta JMA}$	33	24	23	°C/W
4	Junction to ambient (@200 ft./min., four-layer board 2s2p)	$R_{\theta JMA}$	22	17	18	°C/W
5	Junction to board (four-layer board 2s2p) [4]	$R_{\theta JB}$	15	12	13	°C/W
6	Junction to case [5]	$R_{\theta JC}$	7	8	9	°C/W
7	Junction to package top, natural convection [6]	Ψ_{JT}	2	2	2	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

3.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the device junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes

- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

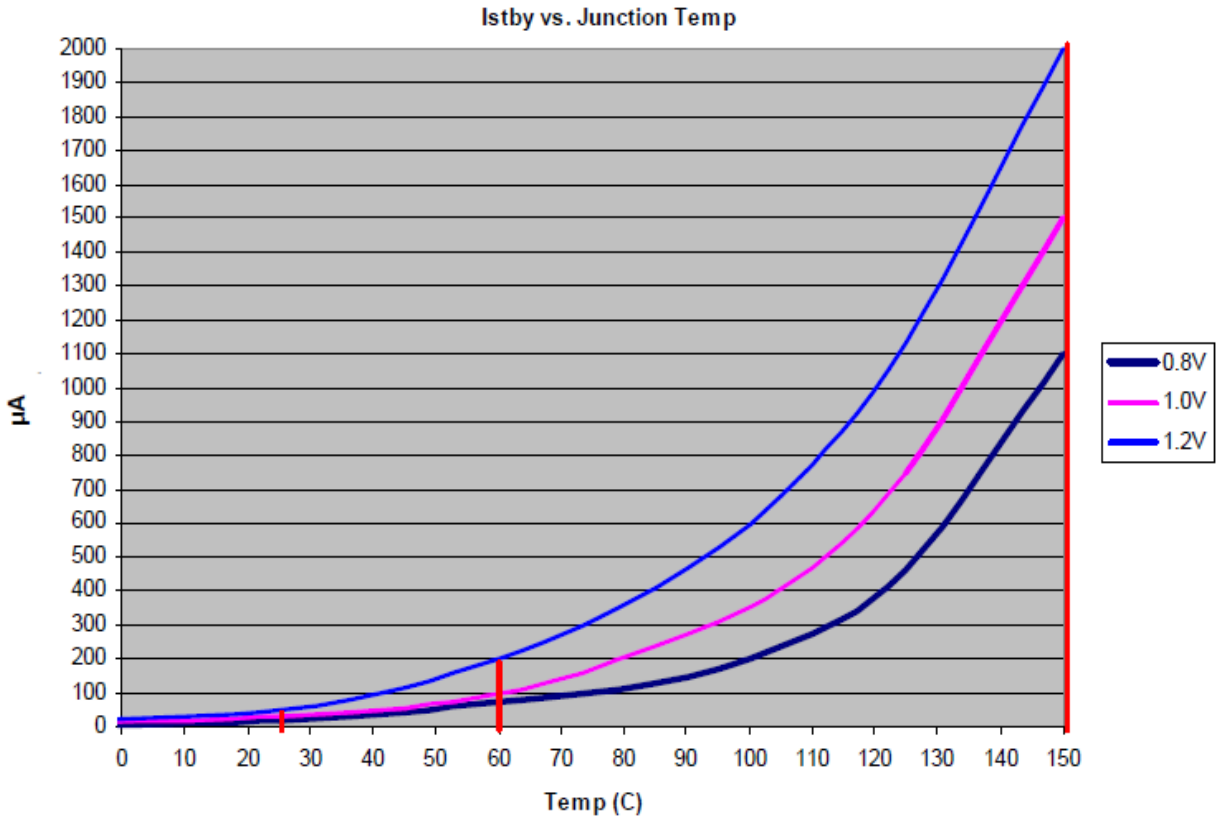
As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

Figure 2 shows an approximate interpolation of the I_{STBY} worst-case specification to estimate values at different voltages and temperatures. The vertical lines shown at 25 °C, 60 °C, and 150 °C in Figure 2 are the actual I_{DD_STBY} specifications (27d) listed in Table 9.

Figure 2. fISTBY Worst-case Specifications



3.7.1 Input Value of Pins During POR Dependent on V_{DD33}

When powering up the device, V_{DD33} must not lag the latest V_{DDSYN} *or* $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6, spec 8. This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and $\overline{\text{RSTCFG}}$ are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} *or* the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification applies during power up only. V_{DD33} has no lead or lag requirements when powering down.

3.7.2 Power-Up Sequence (V_{RC33} Grounded)

The 1.5 V V_{DD} power supply must rise to 1.35 V before the 3.3 V V_{DDSYN} power supply and the $\overline{\text{RESET}}$ power supply rises above 2.0 V. This ensures that digital logic in the PLL for the 1.5 V power supply does not begin to operate below the specified operation range lower limit of 1.35 V. Because the internal 1.5 V POR is disabled, the internal 3.3 V POR or the $\overline{\text{RESET}}$ power POR must hold the device in reset. Since they can negate as low as 2.0 V, V_{DD} must be within specification before the 3.3 V POR and the $\overline{\text{RESET}}$ POR negate.

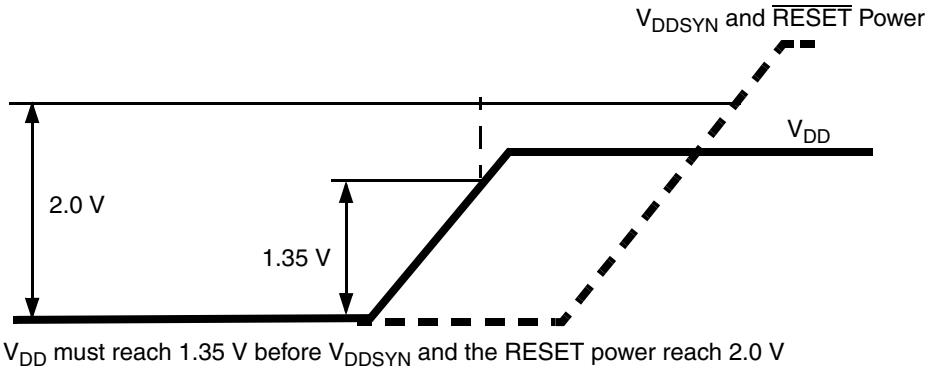


Figure 3. Power-Up Sequence (V_{RC33} Grounded)

3.7.3 Power-Down Sequence (V_{RC33} Grounded)

The only requirement for the power-down sequence with V_{RC33} grounded is if V_{DD} decreases to less than its operating range, V_{DDSYN} or the $\overline{\text{RESET}}$ power must decrease to less than 2.0 V before the V_{DD} power increases to its operating range. This ensures that the digital 1.5 V logic, which is reset only by an ORed POR and can cause the 1.5 V supply to decrease less than its specification value, resets correctly. See Table 6, footnote 1.

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating current 1.5 V supplies @ 132 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	460	mA
	V_{DD} (including V_{DDF} max current) @1.35 V typical use [7, 8]	I_{DD}	—	360	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	510	mA
	V_{DD} (including V_{DDF} max current) @1.35 V high use [8, 9]	I_{DD}	—	410	mA
27b	Operating current 1.5 V supplies @ 114 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	410	mA
	V_{DD} (including V_{DDF} max current) @1.35 V typical use [7, 8]	I_{DD}	—	310	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	460	mA
	V_{DD} (including V_{DDF} max current) @1.35 V high use [8, 9]	I_{DD}	—	370	mA
27c	Operating current 1.5 V supplies @ 82 MHz: [6]				
	V_{DD} (including V_{DDF} max current) @1.65 V typical use [7, 8]	I_{DD}	—	330	mA
	V_{DD} (including V_{DDF} max current) @1.35 V typical use [7, 8]	I_{DD}	—	225	mA
	V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9]	I_{DD}	—	385	mA
	V_{DD} (including V_{DDF} max current) @1.35 V high use [8, 9]	I_{DD}	—	290	mA
27d	RAM standby current.[10]				
	I_{DD_STBY} @ 25° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	20	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	30	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	50	µA
	I_{DD_STBY} @ 60° C				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	70	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	100	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	200	µA
	I_{DD_STBY} @ 150° C (Tj)				
	V_{STBY} @ 0.8 V	I_{DD_STBY}	—	1200	µA
	V_{STBY} @ 1.0 V	I_{DD_STBY}	—	1500	µA
	V_{STBY} @ 1.2 V	I_{DD_STBY}	—	2000	µA
28	Operating current 3.3 V supplies @ f_{MAX} MHz				
	V_{DD33} [11]	I_{DD_33}	—	2 + (values derived from procedure of footnote [11])	mA
	V_{FLASH}	I_{VFLASH}	—	10	mA
	V_{DDSYN}	I_{DDSYN}	—	15	mA
29	Operating current 5.0 V supplies (12 MHz ADCLK):				
	V_{DDA} (V_{DDA0} + V_{DDA1})	I_{DD_A}	—	20.0	mA
	Analog reference supply current (V_{RH}, V_{RL})	I_{REF}	—	1.0	mA
	V_{PP}	I_{PP}	—	25.0	mA

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
30	Operating current V_{DDE} supplies: [12] V_{DDEH1} V_{DDE2} V_{DDE3} V_{DDEH4} V_{DDE5} V_{DDEH6} V_{DDE7} V_{DDEH8} V_{DDEH9}	 I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7} I_{DD8} I_{DD9}	 — — — — — — — — —	 Refer to footnote [12]	 mA mA mA mA mA mA mA mA mA
31	Fast I/O weak pullup current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V	I_{ACT_F}	 10 20 20	 110 130 170	 µA µA µA
	Fast I/O weak pulldown current [13] 1.62–1.98 V 2.25–2.75 V 3.00–3.60 V		 10 20 20	 100 130 170	 µA µA µA
32	Slow and medium I/O weak pullup/down current [13] 3.0–3.6 V 4.5–5.5 V	I_{ACT_S}	 10 20	 150 170	 µA µA
33	I/O input leakage current [14]	I_{INACT_D}	–2.5	2.5	µA
34	DC injection current (per pin)	I_{IC}	–2.0	2.0	mA
35	Analog input current, channel off [15]	I_{INACT_A}	–150	150	nA
35a	Analog input current, shared analog / digital pins (AN[12], AN[13], AN[14], AN[15])	I_{INACT_AD}	–2.5	2.5	µA
36	V_{SS} to V_{SSA} differential voltage [16]	$V_{SS} - V_{SSA}$	–100	100	mV
37	Analog reference low voltage	V_{RL}	$V_{SSA} - 0.1$	$V_{SSA} + 0.1$	V
38	V_{RL} differential voltage	$V_{RL} - V_{SSA}$	–100	100	mV
39	Analog reference high voltage	V_{RH}	$V_{DDA} - 0.1$	$V_{DDA} + 0.1$	V
40	V_{REF} differential voltage	$V_{RH} - V_{RL}$	4.5	5.25	V
41	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} - V_{SS}$	–50	50	mV
42	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} - V_{SS}$	–50	50	mV
43	V_{DDF} to V_{DD} differential voltage	$V_{DDF} - V_{DD}$	–100	100	mV
43a	V_{RC33} to V_{DDSYN} differential voltage	$V_{RC33} - V_{DDSYN}$	–0.1	0.1 [17]	V
44	Analog input differential signal range (with common mode 2.5 V)	V_{IDIFF}	–2.5	2.5	V
45	Operating temperature range, ambient (packaged)	$T_A = (T_L$ to $T_H)$	T_L	T_H	°C
46	Slew rate on power-supply pins	—	—	50	V/ms

1 V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if SIU_ECCR[EBTS] = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if SIU_ECCR[EBTS] = 1.

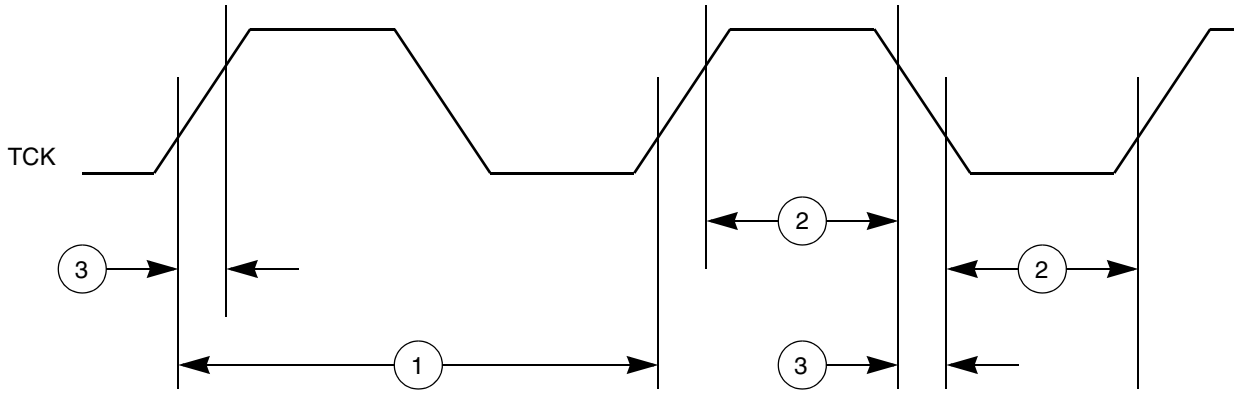


Figure 6. JTAG Test Clock Input Timing

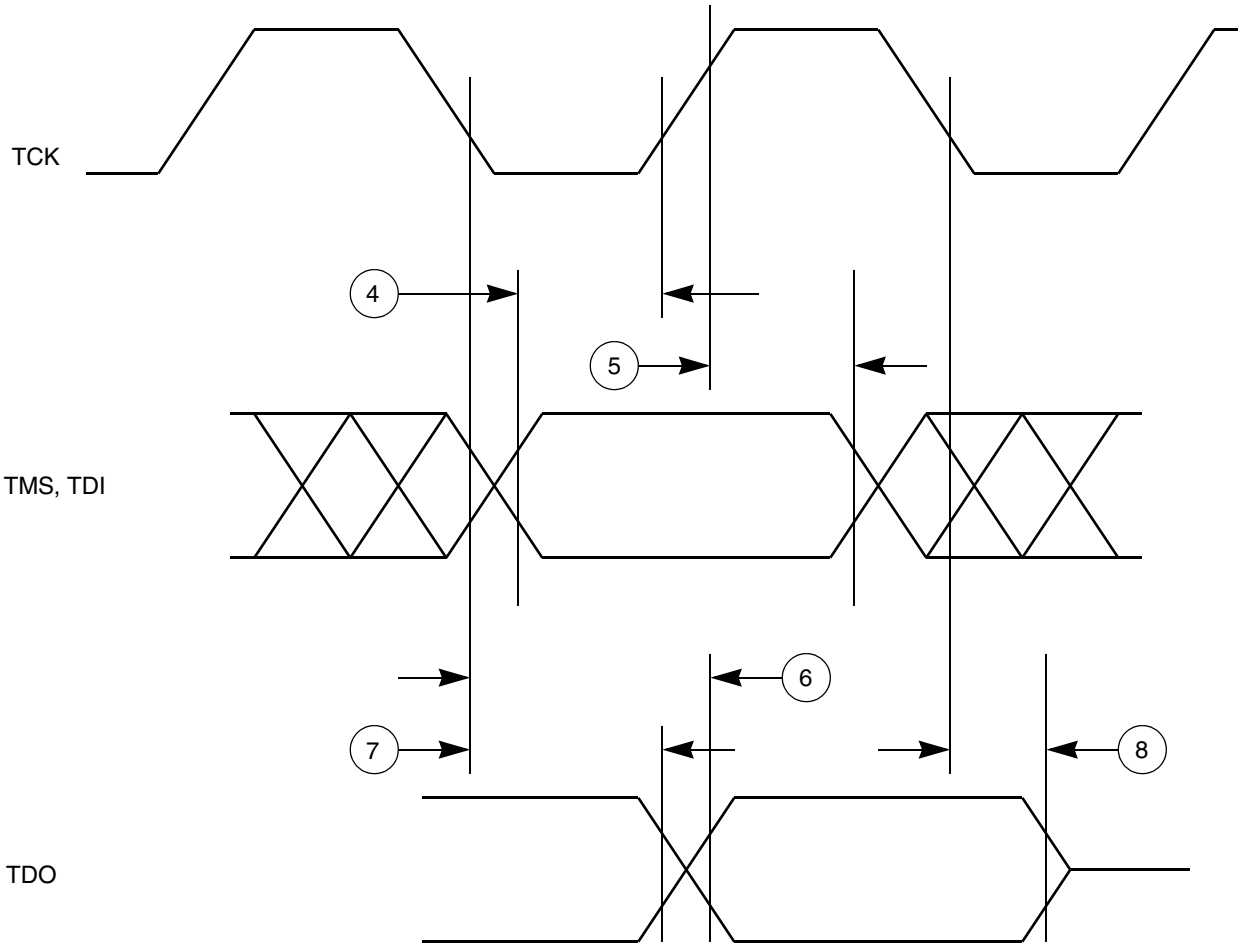


Figure 7. JTAG Test Access Port Timing

3.13.3 Nexus Timing

Table 21. Nexus Debug Port Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	MCKO cycle time	t_{MCYC}	1 [2]	8	t_{CYC}
2	MCKO duty cycle	t_{MDC}	40	60	%
3	MCKO low to MDO data valid [3]	t_{MDOV}	–1.5	3.0	ns
4	MCKO low to $\overline{\text{MSEO}}$ data valid [3]	t_{MSEOV}	–1.5	3.0	ns
5	MCKO low to $\overline{\text{EVTO}}$ data valid [3]	t_{EVTOV}	–1.5	3.0	ns
6	$\overline{\text{EVTI}}$ pulse width	t_{EVTIPW}	4.0	—	t_{TCYC}
7	$\overline{\text{EVTO}}$ pulse width	t_{EVTOPW}	1	—	t_{MCYC}
8	TCK cycle time	t_{TCYC}	4 [4]	—	t_{CYC}
9	TCK duty cycle	t_{TDC}	40	60	%
10	TDI, TMS data setup time	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS data hold time	t_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK low to TDO data valid V_{DDE} = 2.25–3.0 V V_{DDE} = 3.0–3.6 V	t_{JOV}	 0 0	 12 10	 ns ns
13	$\overline{\text{RDY}}$ valid to MCKO [5]	—	—	—	—

1 JTAG specifications apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.35–1.65 V, V_{DDE} = 2.25–3.6 V, V_{DD33} and V_{DDSYN} = 3.0–3.6 V, T_A = T_L to T_H, and CL = 30 pF with DSC = 0b10.

2 The Nexus AUX port runs up to 82 MHz. Set NPC_PCR[MCKO_DIV] to divide-by-two if the system frequency is greater than 82 MHz.

3 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until the next MCKO low cycle occurs.

4 Limit the maximum frequency to approximately 16 MHz (V_{DDE} = 2.25–3.0 V) or 20 MHz (V_{DDE} = 3.0–3.6 V) to meet the timing specification for t_{JOV} of [0.2 x t_{JCYC}] as outlined in the IEEE-ISTO 5001-2003 specification.

5 The $\overline{\text{RDY}}$ pin timing is asynchronous to MCKO and is guaranteed by design to function correctly.

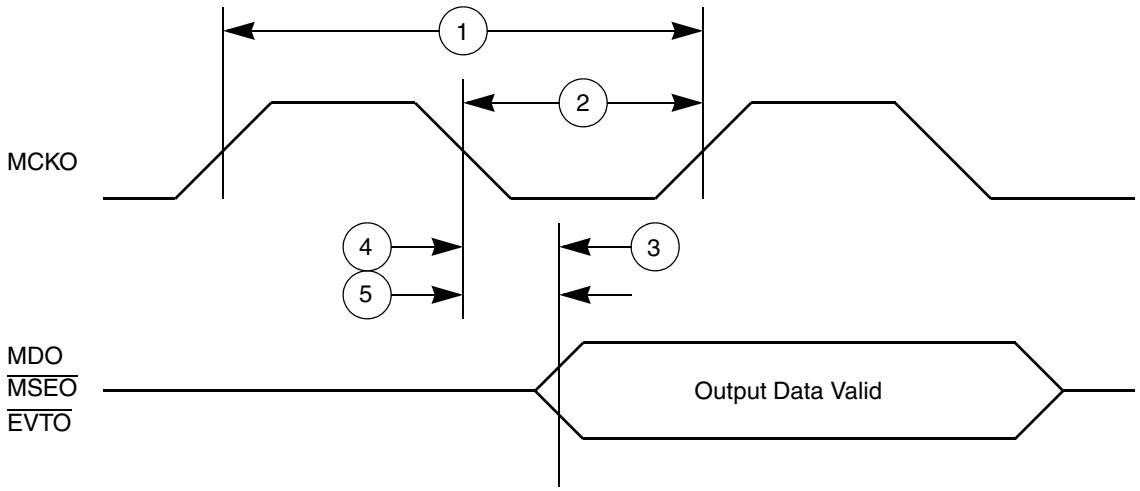


Figure 10. Nexus Output Timing

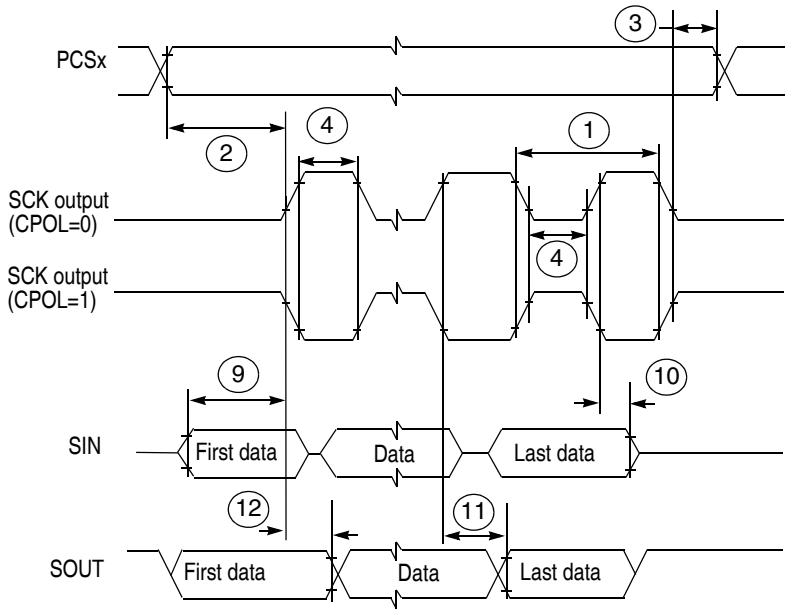


Figure 22. DSPI Modified Transfer Format Timing—Master, CPHA = 0

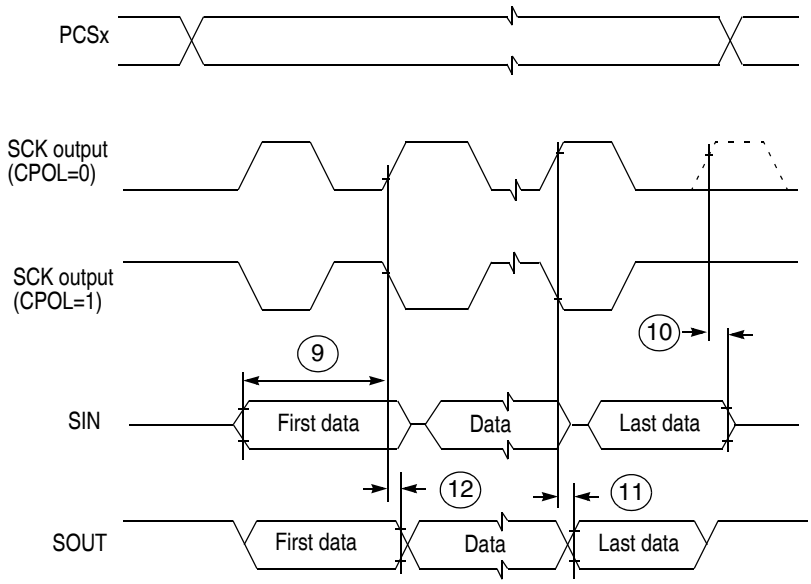


Figure 23. DSPI Modified Transfer Format Timing—Master, CPHA = 1

3.14.3 MII FEC Asynchronous Inputs Signal Timing FEC_CRS and FEC_COL

Table 30 lists MII FEC asynchronous input signal timing.

Table 30. MII FEC Asynchronous Inputs Signal Timing

Spec	Characteristic	Min.	Max	Unit
9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

Figure 30 shows MII FEC asynchronous input timing listed in Table 30.

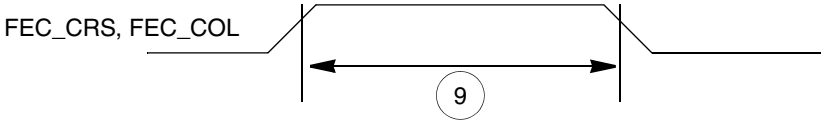


Figure 30. MII FEC Asynchronous Inputs Timing Diagram

3.14.4 MII FEC Serial Management Channel Timing FEC_MDIO and FEC_MDC

Table 31 lists MII FEC serial management channel timing. The FEC functions correctly with a maximum FEC_MDC frequency of 2.5 MHz.

Table 31. MII FEC Serial Management Channel Timing

Spec	Characteristic	Min.	Max	Unit
10	FEC_MDC falling-edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
11	FEC_MDC falling-edge to FEC_MDIO output valid (maximum propagation delay)	—	25	ns
12	FEC_MDIO (input) to FEC_MDC rising-edge setup	10	—	ns
13	FEC_MDIO (input) to FEC_MDC rising-edge hold	0	—	ns
14	FEC_MDC pulse-width high	40%	60%	FEC_MDC period
15	FEC_MDC pulse-width low	40%	60%	FEC_MDC period

Figure 31 shows MII FEC serial management channel timing listed in Table 31.

4.2 MPC5553 324 PBGA Pinouts

Figure 33 is a pinout for the MPC5553 324 PBGA package.

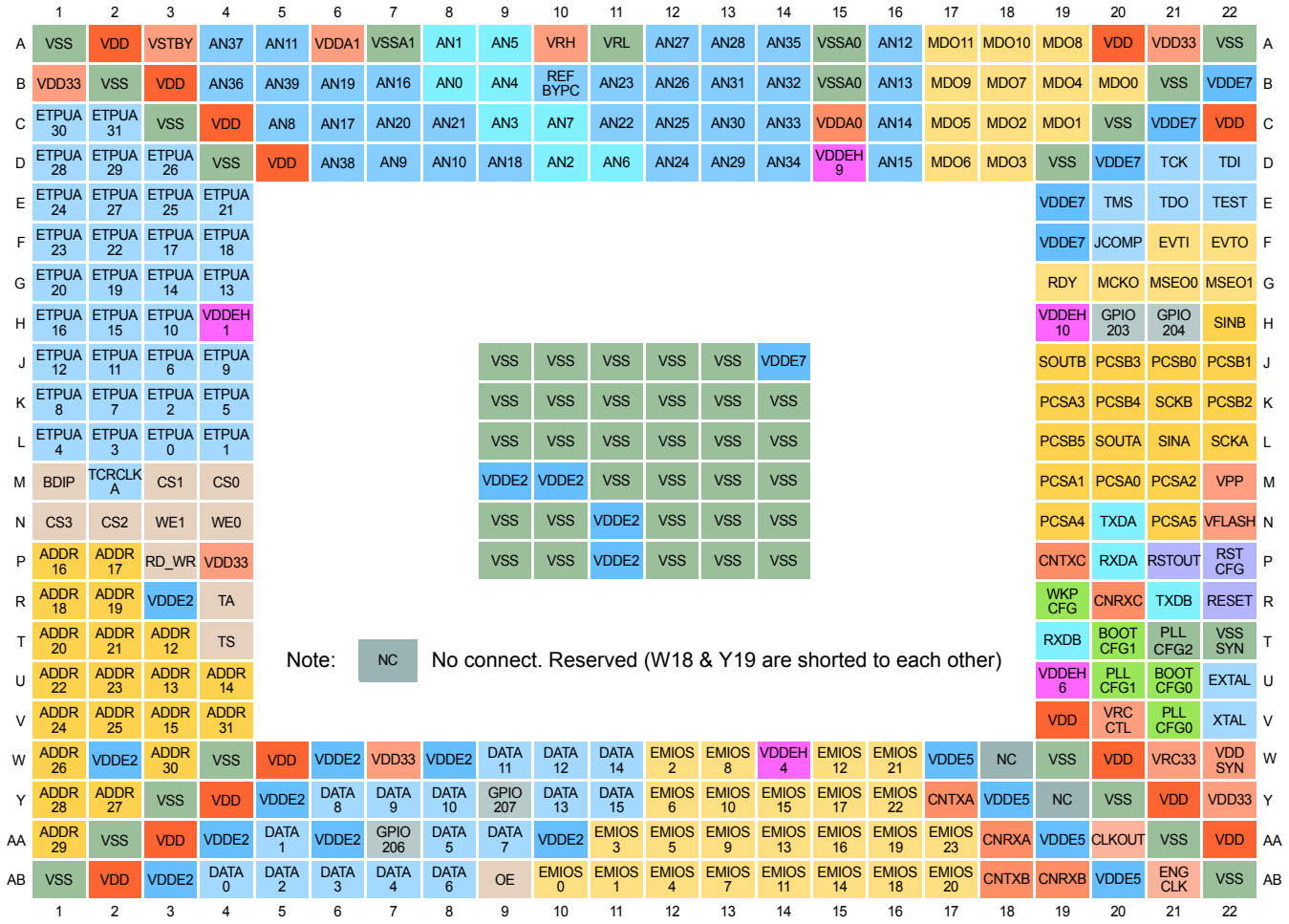


Figure 33. MPC5553 324 Package

4.3 MPC5553 416 PBGA Pinout

Figure 34, Figure 35, and Figure 36 show the pinout for the MPC5553 416 PBGA package. The alternate Fast Ethernet Controller (FEC) signals are multiplexed with the data calibration bus signals.

NOTE

The MPC5500 devices are pin compatible for software portability and use the primary function names to label the pins in the BGA diagram. Although some devices do not support all the primary functions shown in the BGA diagram, the muxed and GPIO signals on those pins remain available. See the signals chapter in the device reference manual for the signal muxing.

14	15	16	17	18	19	20	21	22	23	24	25	26	
VSSA0	AN15	ETRIG 1	ETPUB 18	ETPUB 20	ETPUB 24	ETPUB 27	GPIO 205	MDO11	MDO8	VDD	VDD33	VSS	A
VSSA0	AN14	ETRIG 0	ETPUB 21	ETPUB 25	ETPUB 28	ETPUB 31	MDO10	MDO7	MDO4	MDO0	VSS	VDDE7	B
VDDA0	AN13	ETPUB 19	ETPUB 22	ETPUB 26	ETPUB 30	MDO9	MDO6	MDO3	MDO1	VSS	VDDE7	VDD	C
VDDEH 9	AN12	ETPUB 16	ETPUB 17	ETPUB 23	ETPUB 29	MDO5	MDO2	VDDEH 8	VSS	VDDE7	TCK	TDI	D
									VDDE7	TMS	TDO	TEST	E
									MSEO0	JCOMP	EVTI	EVTO	F
									MSEO1	MCKO	GPIO 204	ETPUB 15	G
									RDY	GPIO 203	ETPUB 14	ETPUB 13	H
									VDDEH 6	ETPUB 12	ETPUB 11	ETPUB 9	J
VDDE7	VDDE7	VDDE7	VDDE7						ETPUB 10	ETPUB 8	ETPUB 7	ETPUB 5	K
VSS	VSS	VSS	VDDE7						ETPUB 6	ETPUB 4	ETPUB 3	ETPUB 2	L
VSS	VSS	VSS	VDDE7						TCRCLKB	ETPUB 1	ETPUB 0	SINB	M
VSS	VSS	VSS	VDDE7						SOUTB	PCSB3	PCSB0	PCSB1	N
VSS	VSS	VSS	VSS						PCSA3	PCSB4	SCKB	PCSB2	P
VSS	VSS	VSS	VSS						PCSB5	SOUTA	SINA	SCKA	R
VDDE2	VDDE2	VSS	VSS						PCSA1	PCSA0	PCSA2	VPP	T
VDDE2	VDDE2	VSS	VSS						PCSA4	TXDA	PCSA5	VFLASH	U
									CNTXC	RXDA	RSTOUT	RST CFG	V
									RXDB	CNRXC	TXDB	RESET	W
									WKP CFG	BOOT CFG1	VRC VSS	VSS SYN	Y
									VDDEH 6	PLL CFG1	BOOT CFG0	EXTAL	AA
									VDD	VRC CTL	PLL CFG0	XTAL	AB
DATA 12	DATA 14	EMIOS 2	EMIOS 8	EMIOS 12	EMIOS 21	VDDEH 4	VDDE5	NC	VSS	VDD	VRC33	VDD SYN	AC
DATA 15	EMIOS 3	EMIOS 6	EMIOS 10	EMIOS 15	EMIOS 17	EMIOS 22	CNTXA	VDDE5	NC	VSS	VDD	VDD33	AD
BG	EMIOS 1	EMIOS 5	EMIOS 9	EMIOS 13	EMIOS 16	EMIOS 19	EMIOS 23	CNRXA	VDDE5	CLKOUT	VSS	VDD	AE
BB	EMIOS 0	EMIOS 4	EMIOS 7	EMIOS 11	EMIOS 14	EMIOS 18	EMIOS 20	CNTXB	CNRXB	VDDE5	ENG CLK	VSS	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Note: NC No connect. AC22 & AD23 reserved

Figure 36. MPC5553 416 Package Right Side (view 2 of 2)

4.5 MPC5553 324-Pin Package Dimensions

The package drawings of the MPC5553 324-pin TEPBGA package are shown in Figure 38.

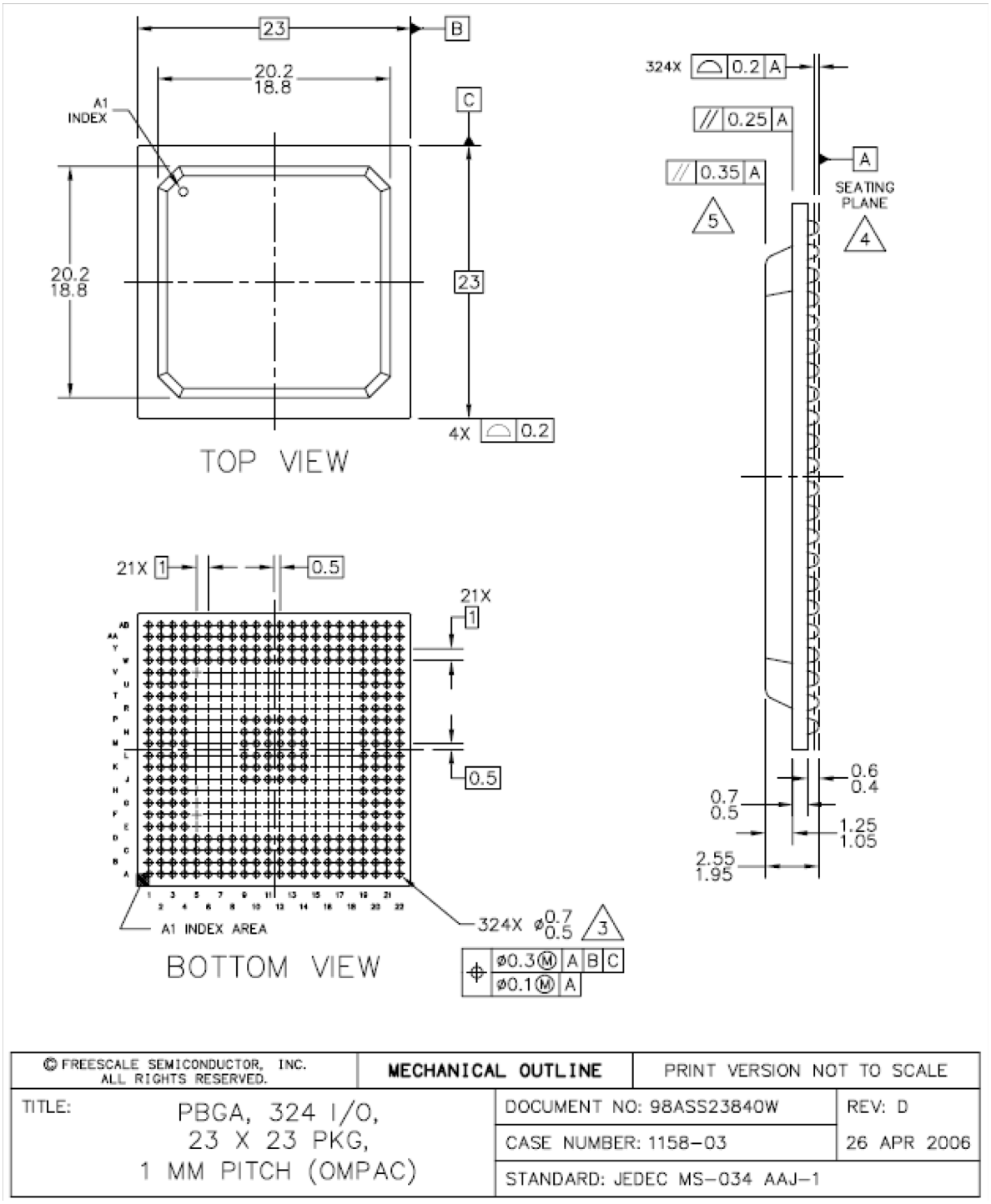


Figure 38. MPC5553 324 TEPBGA Package

4.6 MPC5553 416-Pin Package Dimensions

The package drawings of the MPC5553 416 pin TEPBGA package are shown in Figure 39.

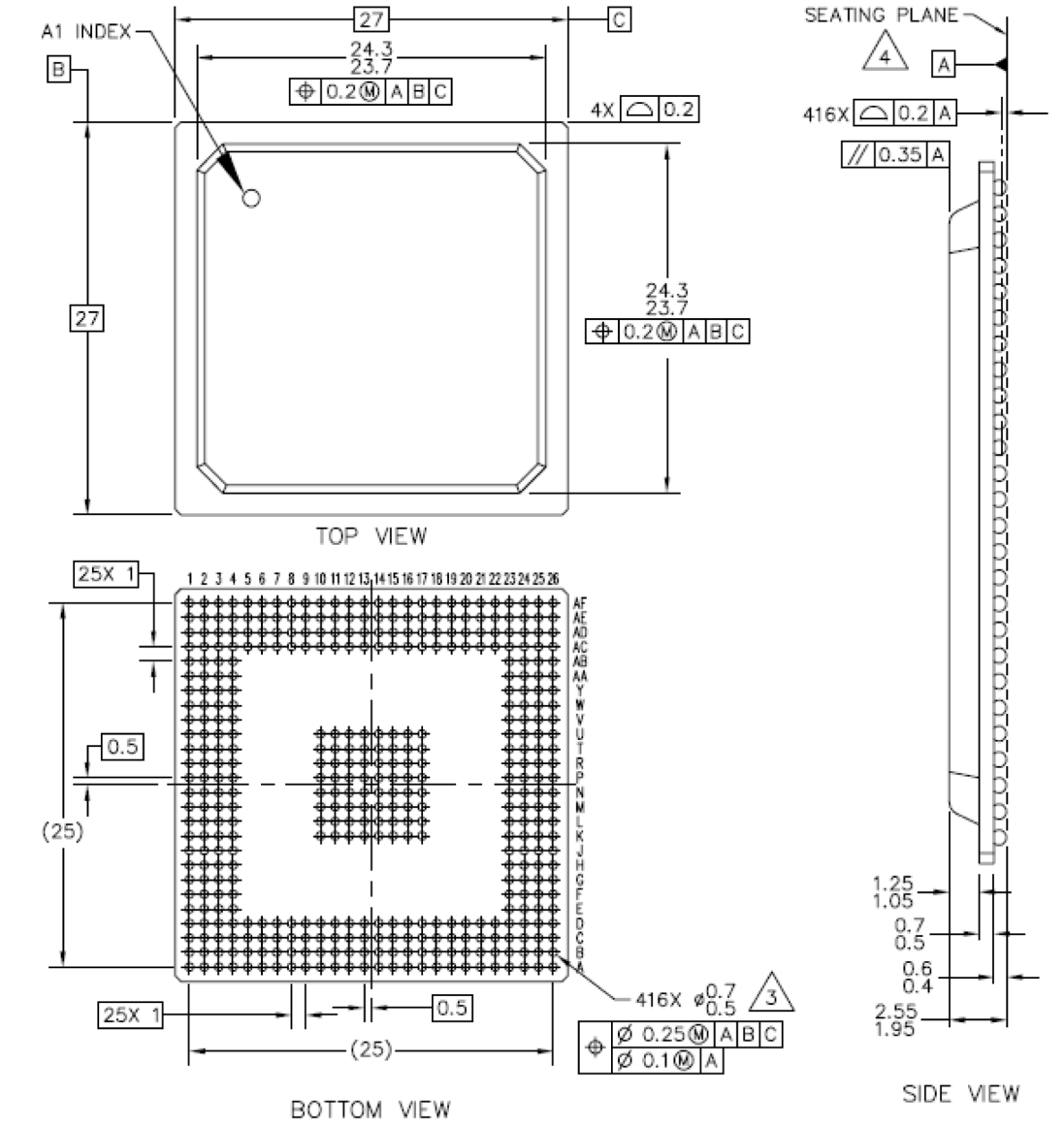


Figure 39. MPC5553 416 TEPBGA Package

Table 32. Global and Text Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Change
Section 1, "Overview":	• Added the sentence directly preceding Table 1: 'Unless noted in this data sheet, all specifications apply from T_L to T_H.' • First paragraph, text changed from "based on the PowerPC Book E architecture" to "built on the Power Architecture embedded technology." • Second paragraph: Changed terminology from PowerPC Book E architecture to Power Architecture terminology.
3.7.1, 3.7.2 and 3.7.3: Reordered sections resulting in the following order and section renumbering:	• Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33," then • Section 3.7.2, "Power-Up Sequence (VRC33 Grounded)," then • Section 3.7.3, "Power-Down Sequence (VRC33 Grounded).
Section 3.7.1, "Input Value of Pins During POR Dependent on VDD33," changed:	From: 'To avoid accidentally selecting the bypass clock because PLLCFG[0:1] and RSTCFG are not treated as ones (1s) when POR negates, V_{DD33} must not lag V_{DDSYN} and the $\overline{\text{RESET}}$ pin power (V_{DDEH6}) when powering the device by more than the V_{DD33} lag specification in Table 6 (V_{RC} and POR Electrical Specifications). V_{DD33} individually can lag either V_{DDSYN} or the $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification. V_{DD33} can lag one of the V_{DDSYN} or V_{DDEH6} supplies, but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.' To: 'When powering the device, V_{DD33} must not lag V_{DDSYN} and the $\overline{\text{RESET}}$ power pin (V_{DDEH6}) by more than the V_{DD33} lag specification listed in Table 6 (V_{RC} and POR Electrical Specifications). This avoids accidentally selecting the bypass clock mode because the internal versions of PLLCFG[0:1] and RSTCFG are not powered and therefore cannot read the default state when POR negates. V_{DD33} can lag V_{DDSYN} or the $\overline{\text{RESET}}$ power pin (V_{DDEH6}), but cannot lag both by more than the V_{DD33} lag specification. This V_{DD33} lag specification only applies during power up. V_{DD33} has no lead or lag requirements when powering down.'
	Added the following text directly before this section and after Table 8 (Pin Status for Medium and Slow Pads During the Power Sequence) *Pin Status for Medium / Slow Pads During the Power-on Sequence*: 'The values in Table 7 (Pin Status for Fast Pads During the Power Sequence) and Table 8 (Pin Status for Medium and Slow Pads During the Power Sequence) do not include the effect of the weak pull devices on the output pins during power up. Before exiting the internal POR state, the voltage on the pins goes to high-impedance until POR negates. When the internal POR negates, the functional state of the signal during reset applies and the weak pull devices (up or down) are enabled as defined in the device *Reference Manual*. If V_{DD} is too low to correctly propagate the logic signals, the weak-pull devices can pull the signals to V_{DDE} and V_{DDEH}. To avoid this condition, minimize the ramp time of the V_{DD} supply to a time period less than the time required to enable the external circuitry connected to the device outputs.'

The following table describes the changes made to information in tables and figures, and is presented in sequential page number order.

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0

Location	Description of Changes
Figure 1 MPC5500 Family Part Numbers:	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ', general market flow' to the M designator, and added an 'S' designator with the description of 'Fully spec. qualified, automotive flow.
Table 1 (Orderable Part Numbers) Orderable Part Numbers:	• Moved the 'Lead-free' or 'Lead' in the Package Description column to a second line and added 'Pb-free' and 'SnPb' respectively. Changed Lead to Leaded. • Footnote 2 changed to read:' The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.' • Footnote 3 changed to read: 'Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM): 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM; and 132 MHz parts allow for 128 MHz system clock + 2% FM;.'
Table 2 (Absolute Maximum Ratings) Absolute Maximum Ratings:	• Deleted Spec 3, "Flash core voltage." • Spec 21, Added the name of the spec, '*V_{RC33} to V_{DDSYN} differential voltage,'* as well as the name and cross reference to Table 9, *DC Electrical Specification*s, to which the Spec was moved. • Spec 28 "Maximum Solder Temperature": Added two lines: Lead-free (Pb-free) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: 'any of' between 'beyond' and 'the listed maxima.' • Deleted footnote 2: 'Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.' • Footnote 6 (now footnote 5): Changed to the following sentence to the end, "Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state."
Table 4 (EMI Testing Specifications) EMI Testing Specifications: Changed the maximum operating frequency to from 132 to f_{MAX}.	
Table 5 (ESD Ratings ,) ESD Characteristics: Added *(Electromagnetic Static Discharge)* in the section title.	

Table 6 (V_{RC} and POR Electrical Specifications), VCR/POR Electrical Specifications:	• Subscript all symbol names that appear after the first underscore character.
	• Removed 'Tj 'after '150 C' in the last line, second column: Characteristic.
	• Reformatted columns.
	• Added footnote 1 to specs 1, 2, and 3 that reads: On power up, assert $\overline{\text{RESET}}$ before V_{POR15}, V_{POR33}, and V_{POR5} negate (internal POR). RESET must remain asserted until the power supplies are within the operating conditions as specified in Table 9 (DC Electrical Specifications ($T_A = T_L$ to T_H)) *DC Electrical Specifications*. On power down, assert $\overline{\text{RESET}}$ before any power supplies fall outside the operating conditions and until the internal POR asserts.
	• Added to Spec 2:
	3.3 V (V_{DDSYN}) POR negated (ramp down) Min. 0.0 Max 0.30 V
	3.3 V (V_{DDSYN}) POR asserted (ramp up) Min. 0.0 Max 0.30 V
	• Specs 7 and 10: added 'at Tj 'at the end of the first line in the second column: Characteristic.
	• Spec 10:
	  • Changed the minimum values of: -40 C = 40; 25 C = 45; 150 C = 55.
	  • Added cross-reference to footnote 6: 'I_{VRCCTL} is measured at the following conditions: V_{DD} = 1.35 V, V_{RC33} = 3.1 V, V_{VRCCTL} = 2.2 V.' Changed '(@ V_{DD} = 1.35 V, $f_{sys} = f_{MAX}$)'to '(@ $f_{sys} = f_{MAX}$).
	• Added a new footnote 7, 'Refer to Table 1 (Orderable Part Numbers) for the maximum operating frequency.'
	• Rewrote old footnote 8 (new footnote 9) to read: Represents the worst-case external transistor BETA. It is measured on a per-part basis and calculated as ($I_{DD} \div I_{VRCCTL}$).
	• Deleted old footnote 9: 'Preliminary value. Final specification pending characterization.'

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 7 (Pin Status for Fast Pads During the Power Sequence) Power Sequence Pin Status for Fast Pads	• Changed title to *Pin Status for Fast Pads During the Power Sequence* • Changed preceding paragraph From: Although there are no power up/down sequencing requirements to prevent issues like latch-up, excessive current spikes, etc., the state of the I/O pins during power up/down varies depending on power. Prior to exiting POR, the pads are in a high impedance state (Hi-Z). To: There are no power up/down sequencing requirements to prevent issues such as latch-up, excessive current spikes, and so on. Therefore, the state of the I/O pins during power up/down varies depending on which supplies are powered.
Table 8 (Pin Status for Medium and Slow Pads During the Power Sequence) Power Sequence Pin Status for Medium/Slow Pads:	• Changed title to *Pin Status for Medium and Slow Pads During the Power Sequence* • Updated preceding paragraph.
Table 9 (DC Electrical Specifications ($T_A = T_{L\ to}\ T_H$)) DC Electrical Specifications:	• Spelled the slash '/' as 'and' as well as 'I/O' as 'input/output.' Still very confusing. Deleted 'input/output'. • Added footnote that reads: V_{DDE2} and V_{DDE3} are limited to 2.25–3.6 V only if EBTS = 0; V_{DDE2} and V_{DDE3} have a range of 1.6–3.6 V if EBTS =1. • Spec 20, column 2, *Characteristics*,' Slow and medium output high voltage (I_{OH_S} = –2.0 mA):' Created a left-justified second line and moved 'I_{OH_S} = –2.0 mA' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OH_S} = –1.0 mA.' • Spec 20, column 4, *Min.*: Added a blank line before and after '0.80 × V_{DDEH}' and put '0.85 × V_{DDEH}' on the last line. • Spec 22, column 2,'*Slow and medium output low voltage (I_{OL_S} = 2.0 mA)*:' Created a left-justified second line and moved 'I_{OL_S} = 2.0 mA.' from the 1st line to the second line and deleted the parentheses. Created a left-justified third line that reads 'I_{OL_S} = 1.0 mA.' Column 5, *Max*: Added a blank line before and after '0.20 × V_{DDEH}' and put '0.15 × V_{DDEH}' on the last line. • Spec 26: Changed 'AN[12]_MA[1]_SDO' to 'AN[13]_MA[1]_SDO'. • Spec 27a: Operating current 1.5 V supplies @ 132 MHz changed to: 1.65 typical = 460 1.35 typical = 360 1.65 high = 510 1.35 high = 410 • Spec 27b, Operating current 1.5 V supplies @ 114 MHz changed to: 1.65 typical = 410 1.35 typical = 310 1.65 high = 460 1.35 high = 370 • Spec 27c, Operating current 1.5 V supplies @ 82 MHz changed to: 1.65 typical = 330 1.35 typical = 225 1.65 high = 385 1.35 high = 290 • Spec 28: Changed 132 MHz to f_{MAX} MHz. • Footnote 3 changed to read: If standby operation is not required, connect V_{STBY} to ground. • Footnote 6 is now: Figure 3 (Power-Up Sequence (VRC33 Grounded))shows an illustration of the IDD_STBY values interpolated for these temperature values. • Deleted footnote 9: 'Preliminary. Final specification pending characterization.' • Deleted duplicate footnote: 'Absolute value of current, measured at V_{IL} and V_{IH}.

Table 33. Table and Figure Changes Between Rev. 2.0 and 3.0 (continued)

Location	Description of Changes
Table 25 (eMIOS Timing) eMIOS Timing:	• Deleted (MTS) from the heading, table, and footnotes. • Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Footnote 1: Deleted 'F_{SYS} = 132 MHz', 'V_{DD} = 1.35–1.65 V', 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V' and 'and CL = 200 pF with SRC = 0b11.' • Added Footnote 2: 'This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).'
Figure 17 (eMIOS Timing) Added *eMIOS Timing* figure.	
Table 26 (DSPI Timing') DSPI Timing:	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Table Title: Added footnote that reads: Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 82 MHz parts allow for 80 MHz system clock + 2% FM; 114 MHz parts allow for 112 MHz system clock + 2% FM, and 132 MHz parts allow for 128 MHz system clock + 2% FM. • Spec 1: SCK cycle time; Changed 80 MHz = 24.4, and 112 MHz = 17.5. • Footnote 1: Changed to read: 'All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on pad type M or MH. DSPI signals using pad types of S or SH have an additional delay based on the slew rate.' Deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6 V.
Table 27 (EQADC SSI Timing Characteristics) EQADC SSI Timing Characteristics:	• Footnote 1, changed 'V_{DDEH} = 4.5–5.5;' to 'V_{DDEH} = 4.5–5.25;' • Deleted from table title '(Pads at 3.3 V or 5.0 V)' • Deleted 1st line in table 'CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.' • Spec 1: FCK frequency -- removed. • Combined footnotes 1 and 2, and moved the new footnote to Spec 2. Moved old footnote 3 that is now footnote 2 to Spec 2. • Footnote 1, deleted 'V_{DD} = 1.35–1.65 V' and 'V_{DD33} and V_{DDSYN} = 3.0–3.6V.' Changed 'CL = 50 pF' to 'CL = 25 pF.' • Footnote 2: added 'cycle' after 'duty' to read: FCK duty cycle is not 50% when. . . .
Section 3.14, "Fast Ethernet AC Timing Specifications": Figure 28 (MII FEC Receive Signal Timing Diagram), Figure 29 (MII FEC Transmit Signal Timing Diagram), Figure 30 (MII FEC Asynchronous Inputs Timing Diagram), and Figure 31 (MII FEC Serial Management Channel Timing Diagram).	Removed the 'M' in the diagram labels that refer to the specification numbers.
Figure 37 (MPC5553 208-Pin Package)MPC5553 208 Package: Deleted the version number and date.	
Figure 38 (MPC5553 324 TEPBGA Package)MPC5553 324 Package: Deleted the version number and date.	
Figure 39 (MPC5553 416 TEPBGA Package) and Figure 39 (MPC5553 416 TEPBGA Package (continued))*MPC5553 416 Package*: Deleted the version number and date.	

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