



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mfcdfp-v1

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Encryption function	AES*3	• Key lengths: 128, 192, and 256 bits • Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	DES*3	• Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) • Support for DES and triple DES • Support for ECB and CBC operating modes • Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode • Compliant with FIPS PUB 46-3 • Compliant with FIPS PUB 81
	SHA*3	• Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) • Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode • Compliant with SHA as defined in FIPS PUB 180-1 and -2 • Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)*3	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$, VCC_USBA = AVCC_USBA = 2.7 to 3.6 V, VBATT = 2.0 to 3.6 V
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C (in planning)
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I ² C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

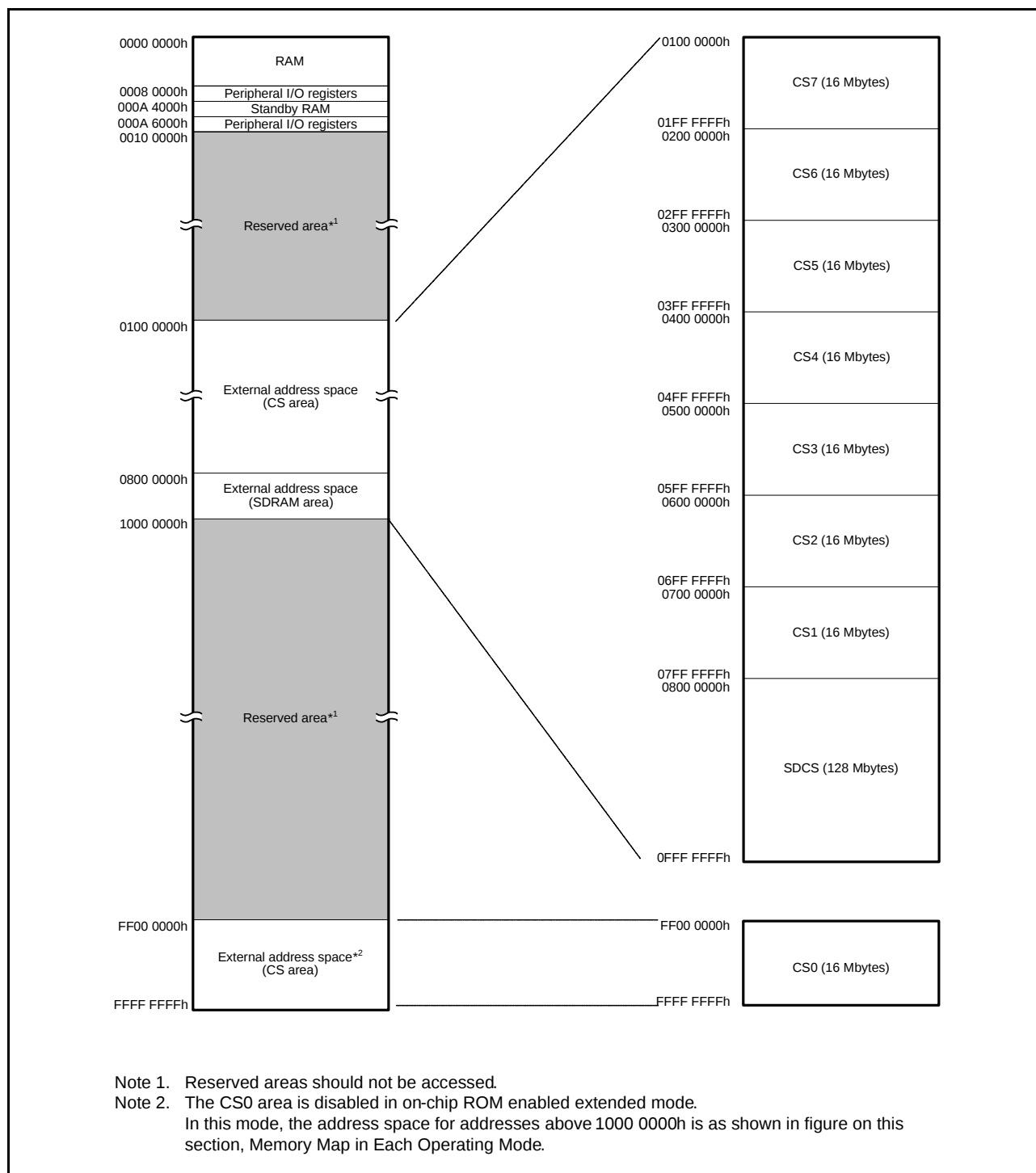
Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (6/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
143		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
144		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
145		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
146		PG0	D24		ET1_RX_CLK/ REF50CK1			
147		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
149		P97	A23/D23		ET1_ERXD3			
150		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
151	VSS							
152		P96	A22/D22		ET1_ERXD2			
153	VCC							
154		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2_B	IRQ2	AN110
155		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
156		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
157		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
158		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
159		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
160		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
161		P91	A17/D17		ET1_COL/SCK7			AN115
162	VSS							
163		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
164	VCC							
165		P47					IRQ15- DS	AN007
166		P46					IRQ14- DS	AN006
167		P45					IRQ13- DS	AN005
168		P44					IRQ12- DS	AN004
169		P43					IRQ11-DS	AN003
170		P42					IRQ10- DS	AN002
171		P41					IRQ9-DS	AN001
172	VREFL0							

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (15 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EAh	PPG0	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EBh	PPG0	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81ECh	PPG0	Next Data Registers H*1	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EDh	PPG0	Next Data Registers L*2	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EEh	PPG0	Next Data Registers H*1	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EFh	PPG0	Next Data Registers L*2	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F0h	PPG1	PPG Trigger Select Register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F6h	PPG1	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F7h	PPG1	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F8h	PPG1	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F9h	PPG1	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FAh	PPG1	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FBh	PPG1	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FCh	PPG1	Next Data Registers H*3	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh	PPG1	Next Data Registers L*4	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FEh	PPG1	Next Data Registers H*3	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FFh	PPG1	Next Data Registers L*4	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR

Table 4.1 List of I/O Registers (Address Order) (24 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A069h	SCI3	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Ah	SCI3	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Bh	SCI3	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Ch	SCI3	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Eh	SCI3	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Fh	SCI3	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Eh	SCI3	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A070h	SCI3	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A071h	SCI3	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A070h	SCI3	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A072h	SCI3	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A080h	SCI4	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A081h	SCI4	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A082h	SCI4	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A083h	SCI4	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A084h	SCI4	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A085h	SCI4	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A086h	SMCI4	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A089h	SCI4	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ah	SCI4	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Bh	SCI4	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ch	SCI4	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h

Table 4.1 List of I/O Registers (Address Order) (28 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2, 3 PCLKB	2 ICLK	DOC
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B101h	ELC	Event Link Setting Register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Ch	ELC	Event Link Setting Register 11	ELSR11	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Eh	ELC	Event Link Setting Register 13	ELSR13	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B131h	ELC	Event Link Setting Register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B133h	ELC	Event Link Setting Register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B134h	ELC	Event Link Setting Register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B135h	ELC	Event Link Setting Register 37	ELSR37	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B136h	ELC	Event Link Setting Register 38	ELSR38	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B139h	ELC	Event Link Setting Register 41	ELSR41	8	8	2, 3 PCLKB	2 ICLK	ELC

Table 4.1 List of I/O Registers (Address Order) (30 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (51 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A10h	MTU6	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRb	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A31h	MTU	Timer Interrupt Skipping Counter 1B	TITCNT1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Ch	MTU	Timer Interrupt Skipping Counter 2B	TITCNT2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Ch	MTU6	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (66 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
000D 049Ch	USBA	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 049Eh	USBA	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04A0h	USBA	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04A2h	USBA	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04D0h	USBA	Device Address 0 Configuration Register	DEVADD0	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04D2h	USBA	Device Address 1 Configuration Register	DEVADD1	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04D4h	USBA	Device Address 2 Configuration Register	DEVADD2	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04D6h	USBA	Device Address 3 Configuration Register	DEVADD3	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04D8h	USBA	Device Address 4 Configuration Register	DEVADD4	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 04DAh	USBA	Device Address 5 Configuration Register	DEVADD5	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0500h	USBA	Low Power Control Register	LPCTRL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0502h	USBA	Low Power Status Register	LPSTS	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0540h	USBA	Battery Charging Control Register	BCCTRL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0544h	USBA	Function L1 Control Register 1	PL1CTRL1	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0546h	USBA	Function L1 Control Register 2	PL1CTRL2	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}^{*2}$	t_{SBYSEQ}^{*3}		
Recovery time after cancellation of software standby mode*1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	$\{ (MSTS[7:0] \text{ bits} \times 32) + 76 \} / 0.216$	$100 \mu s + 7/f_{ICLK} + 2n/f_{MAIN}$	μs	Figure 5.12
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			$\{ (MSTS[7:0] \text{ bits} \times 32) + 138 \} / 0.216$	$100 \mu s + 7/f_{ICLK} + 2n/f_{PLL}$		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	$100 \mu s + 7/f_{ICLK} + 2n/f_{EXMAIN}$		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	$100 \mu s + 7/f_{ICLK} + 2n/f_{PLL}$		
	Sub-clock oscillator operating		t_{SBYSC}			$\{ (SSTS[7:0] \text{ bits} \times 16384) + 13 \} / 0.216 + 10/f_{FCLK}$	$100 \mu s + 4/f_{ICLK} + 2n/f_{SUB}$		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	$100 \mu s + 7/f_{ICLK} + 2n/f_{HOCO}$		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	$100 \mu s + 7/f_{ICLK} + 2n/f_{PLL}$		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	$100 \mu s + 7/f_{ICLK} + 2n/f_{LOCO}$		

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

Note 4. This condition applies when $f_{ICLK}:f_{FCLK} = 1:1$, $2:1$, or $4:1$.

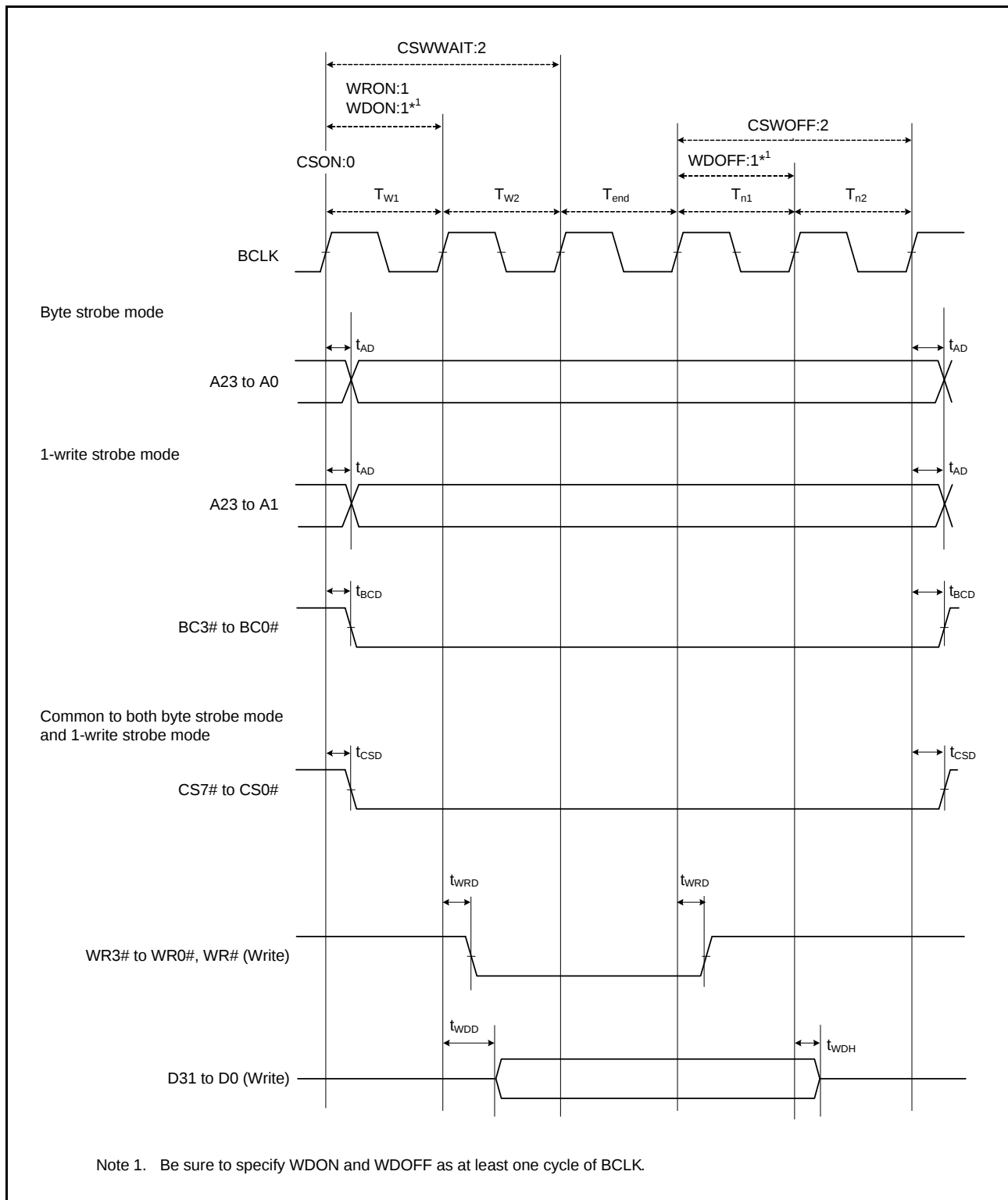


Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

Table 5.33 RSPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{PAcyc}	Figure 5.46	
		Slave		8	4096			
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns		
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—			
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns		
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—			
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input		—	1	μs		
	Data input setup time	Master	t_{SU}	6	—	ns	Figure 5.47 to Figure 5.52	
		Slave		$8.3 - t_{PAcyc}$	—			
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—		ns
				t_H	t_{PAcyc}	—		
		Slave			$8.3 + 2 \times t_{PAcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}		
		Slave		4	—	t_{PAcyc}		
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}		
		Slave		4	—	t_{PAcyc}		
	Data output delay time	Master	t_{OD}	—	6.3	ns		
		Slave		—	$3 \times t_{PAcyc} + 20$			
Data output hold time	Master	t_{OH}	0	—	ns			
	Slave		0	—				
Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns			
	Slave		$4 \times t_{PAcyc}$	—				
MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns			
	Input		—	1	μs			
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns			
	Input		—	1	μs			
Slave access time			t_{SA}	—	4	t_{PAcyc}	Figure 5.51, Figure 5.52	
Slave output release time			t_{REL}	—	3	t_{PAcyc}		

Note 1. t_{PAcyc} : PCLKA cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.

Table 5.41 PDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	ns	Figure 5.72
	PIXCLK input high pulse width	t_{PIXH}	10	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	ns	
	PIXCLK rising time	t_{PIXr}	5	ns	
	PIXCLK falling time	t_{PIXf}	5	ns	
	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	ns	Figure 5.73
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO rising time	t_{PCKr}	5	ns	
	PCKO falling time	t_{PCKf}	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	ns	Figure 5.74
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	ns	
	PIXD input setup time	t_{PIXDS}	10	ns	
	PIXD input hold time	t_{PIXDH}	5	ns	

Note 1. t_{PBcyc} : PCLKB cycle

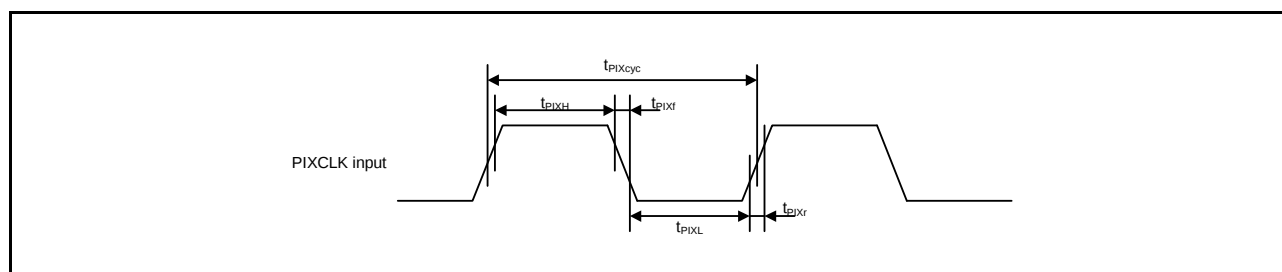
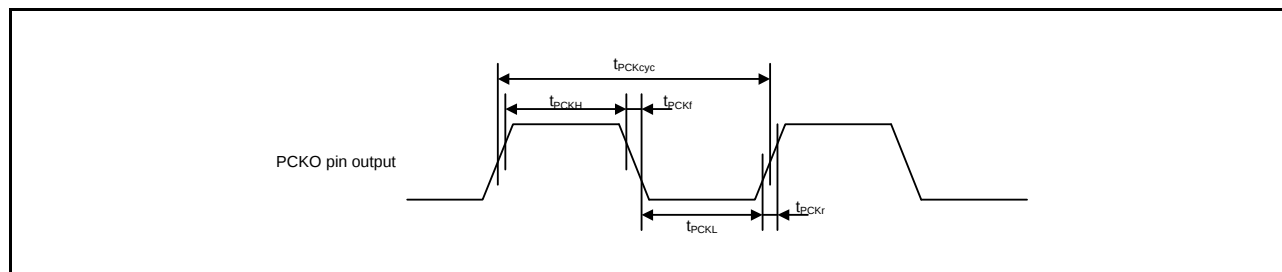
**Figure 5.72 PDC Input Clock Timing****Figure 5.73 PDC Output Clock Timing**

Table 5.46 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKB = PCLKD = 1$ MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLK = 60 MHz)	Permissible signal source impedance (max.) = 1.0 kΩ	0.88 (0.667) *2	—	—	μs	Sampling in 40 states
Analog input capacitance		—	—	30	pF	
Offset error		—	±2.0	±3.5	LSB	
Full-scale error		—	±2.0	±3.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±4.0	±6.0	LSB	
DNL differential nonlinearity error		—	±1.5	±2.5	LSB	
INL integral nonlinearity error		—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.47 A/D Internal Reference Voltage Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKB = PCLKD = 60$ MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.20	1.25	1.30	V	

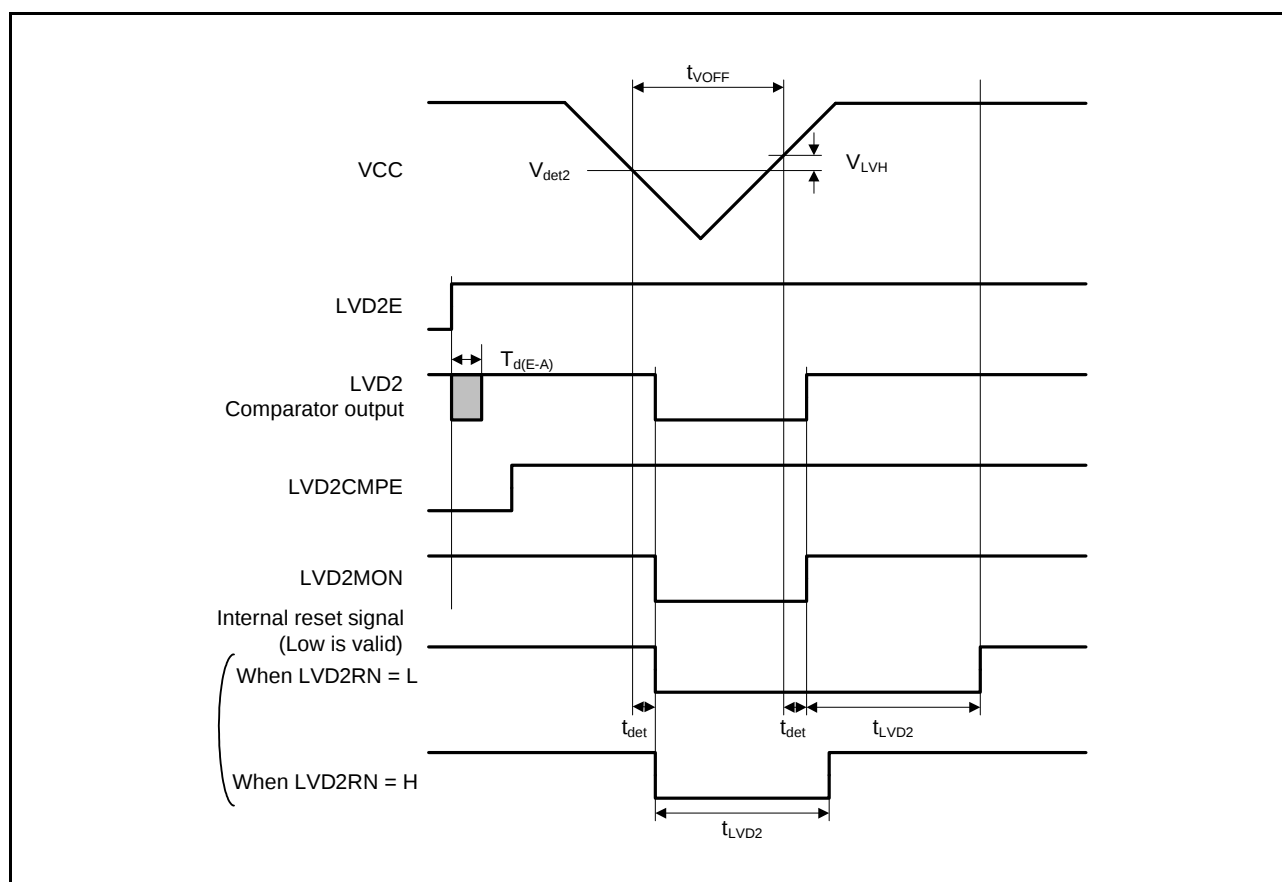


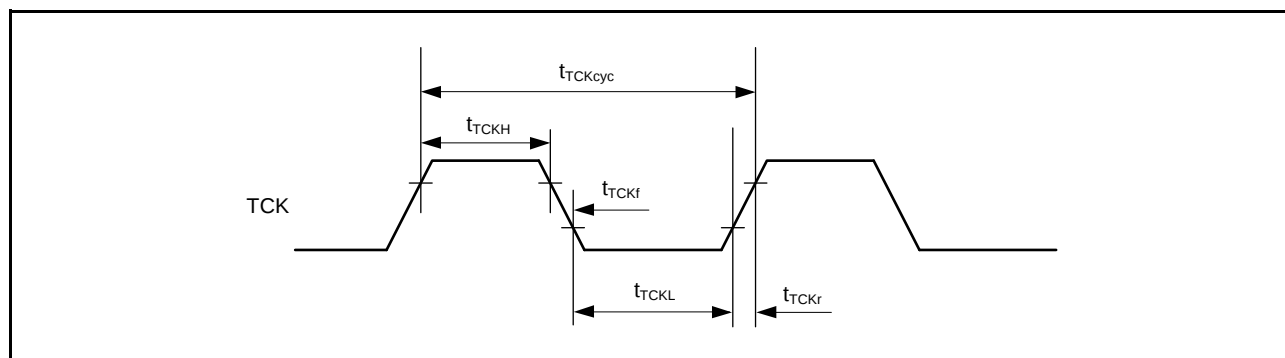
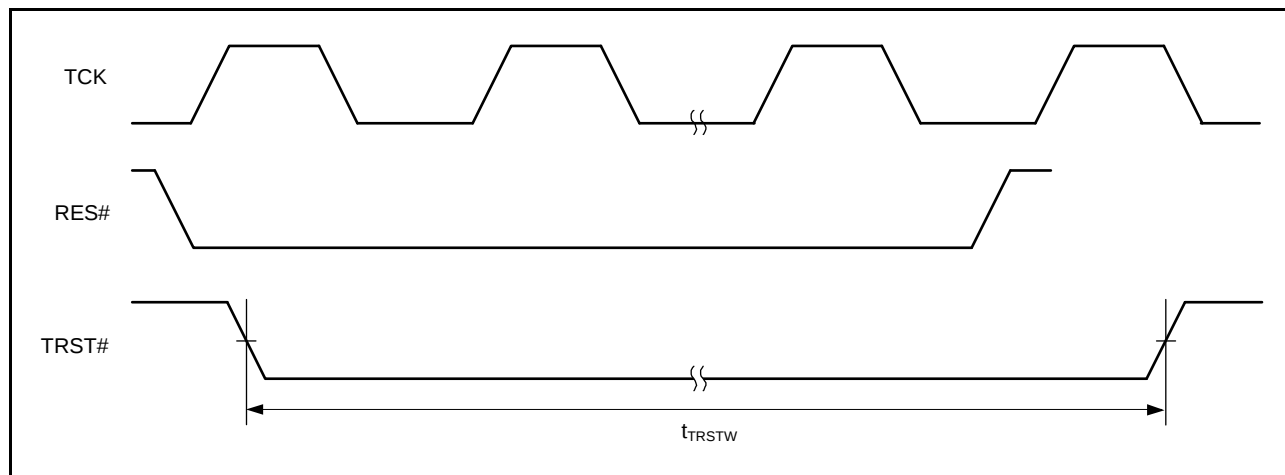
Figure 5.82 Voltage Detection Circuit Timing (V_{det2})

5.12 Boundary Scan

Table 5.55 Boundary Scan Characteristics

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.86
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.87
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.88
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

**Figure 5.86 Boundary Scan TCK Timing****Figure 5.87 Boundary Scan TRST# Timing**

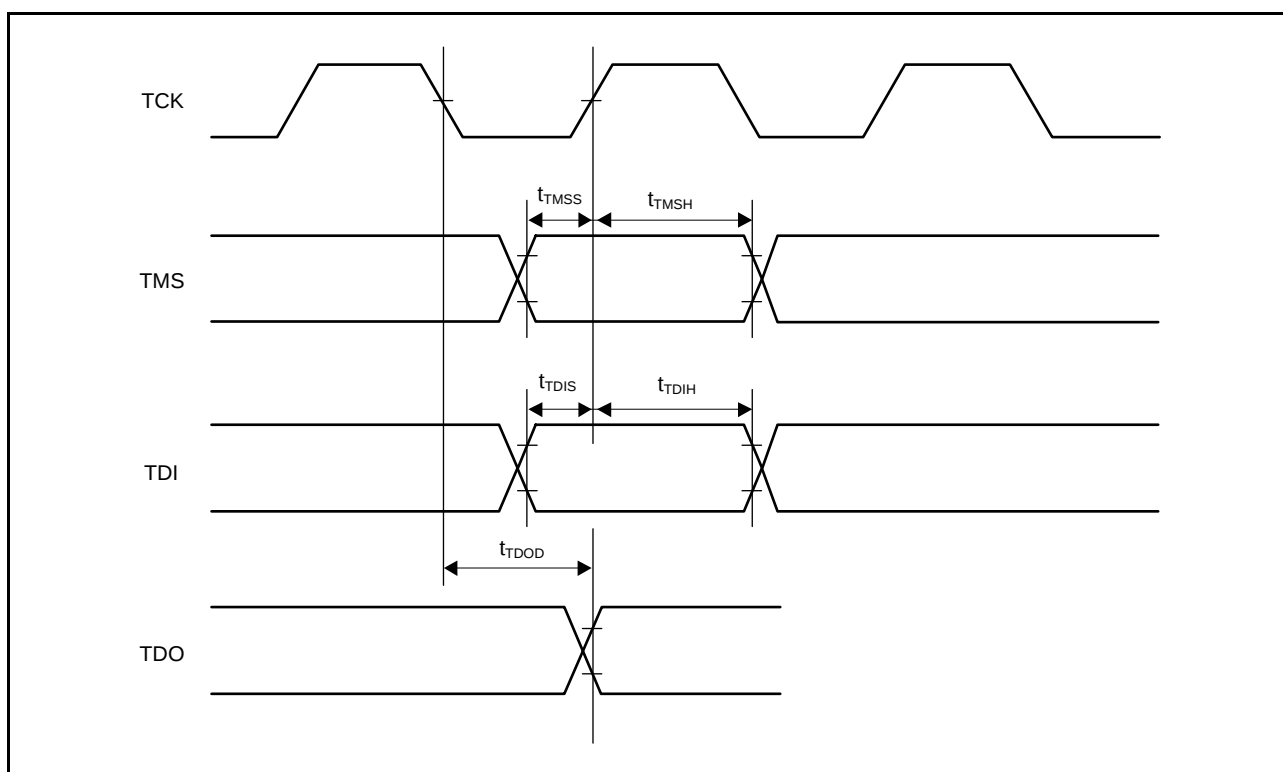


Figure 5.88 Boundary Scan Input/Output Timing