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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mfhdbg-21

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VCC_USB, VCC_USBA	Input	Power supply pins
	VSS_USB, VSS1_USBA, VSS2_USBA	Input	Ground pins
	AVCC_USBA	Input	USBA analog power supply pin
	AVSS_USBA	Input	USBA analog ground pin. Short this pin with the PVSS_USBA pin.
	PVSS_USBA	Input	USBA PLL circuit ground pin. Short this pin with the AVSS_USBA pin.
	USBA_RREF	I/O	USBA reference current supply pin. Connect 2.2 k Ω ($\pm 1\%$) to the AVSS_USBA pin.
	USB0_DP, USBA_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM, USBA_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN, USBA_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID, USBA_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN, USBA_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA, USB0_OVRCURB, USBA_OVRCURA, USBA_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS, USBA_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX0, CRX1-DS, CRX2	Input	Input pins
	CTX0 to CTX2	Output	Output pins
Serial peripheral interface	RSPCKA-A/RSPCKA-B	I/O	Clock input/output pin
	MOSIA-A/MOSIA-B	I/O	Inputs or outputs data output from the master
	MISOA-A/MISOA-B	I/O	Inputs or outputs data output from the slave
	SSLA0-A/SSLA0-B	I/O	Input or output pin for slave selection
	SSLA1-A/SSLA1-B to SSLA3-A/SSLA3-B	Output	Output pin for slave selection
Quad serial peripheral interface	QSPCLK-A/-B	Output	QSPI clock output pin
	QSSL-A/-B	Output	QSPI slave output pin
	QMO-A/-B, QIO0-A/-B	I/O	Master transmit data/data 0
	QMI-A/-B, QIO1-A/-B	I/O	Master input data/data 1
	QIO2-A/-B, QIO3-A/-B	I/O	Data 2, data 3
Serial sound interface	SSISCK0, SSISCK1	I/O	SSI serial bit clock pins
	SSIWS0, SSIWS1	I/O	Word select pins
	SSITXD0, SSITXD1	Output	Serial data output pins
	SSIRXD0, SSIRXD1	Input	Serial data input pins
	SSIDATA0, SSIDATA1	I/O	Serial data input/output pins
	AUDIO_MCLK	Input	Master clock pin for audio

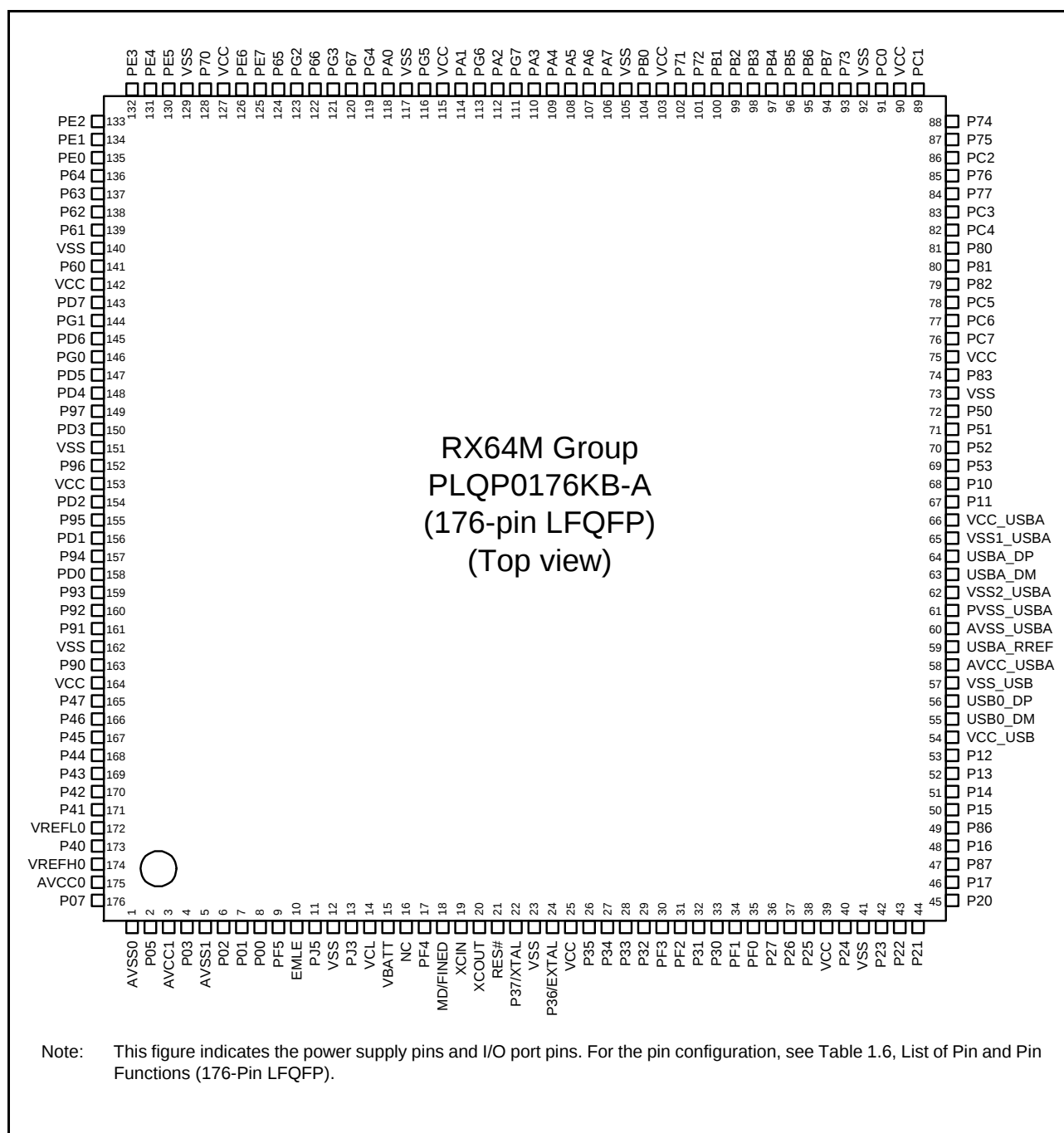


Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 4.1 List of I/O Registers (Address Order) (3 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPRCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPRCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETST	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		Buses
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		Buses
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK		DMACaA
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 201Fh	DMAC0	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 205Fh	DMAC1	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 209Fh	DMAC2	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA

Table 4.1 List of I/O Registers (Address Order) (20 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSE R	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR 0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR 1	16	16	2, 3 PCLKB	2 ICLK	S12ADC

Table 4.1 List of I/O Registers (Address Order) (34 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C0D0h	PORTG	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0D2h	PORTJ	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E5h	PORT5	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0F0h	PORTG	Drive Capacity Control Register	DSCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C100h	MPC	CS Output Enable Register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C102h	MPC	CS Output Pin Select Register 0	PFCS0	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C103h	MPC	CS Output Pin Select Register 1	PFCS1	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C104h	MPC	Address Output Enable Register 0	PFAOE0	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C105h	MPC	Address Output Enable Register 1	PFAOE1	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C106h	MPC	External Bus Control Register 0	PFBCR0	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C107h	MPC	External Bus Control Register 1	PFBCR1	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C10Eh	MPC	Ethernet Control Register	PFENET	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Ah	MPC	P12 Pin Function Control Register	P12PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Bh	MPC	P13 Pin Function Control Register	P13PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2, 3 PCLKB	2 ICLK	MPC

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1854h	CAN1	Time Stamp Register	TSR	16	16	2, 3 PCLKB	2 ICLK	CAN
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2200h to 0009 23FFh	CAN2	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 2400h to 0009 241Fh	CAN2	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2420h	CAN2	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2424h	CAN2	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2428h	CAN2	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 242Ch	CAN2	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2820h to 0009 283Fh	CAN2	Message Control Registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2840h	CAN2	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2842h	CAN2	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2844h	CAN2	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2848h	CAN2	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ah	CAN2	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Bh	CAN2	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ch	CAN2	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Dh	CAN2	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Eh	CAN2	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Fh	CAN2	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2850h	CAN2	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2851h	CAN2	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2852h	CAN2	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2853h	CAN2	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2854h	CAN2	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2856h	CAN2	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2858h	CAN2	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 4200h	CMTW0	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4204h	CMTW0	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4208h	CMTW0	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4210h	CMTW0	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4214h	CMTW0	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4218h	CMTW0	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 421Ch	CMTW0	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4220h	CMTW0	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4224h	CMTW0	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4280h	CMTW1	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4284h	CMTW1	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4288h	CMTW1	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4290h	CMTW1	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4294h	CMTW1	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4298h	CMTW1	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 429Ch	CMTW1	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (48 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0440h	PTPED MAC	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0448h	PTPED MAC	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0450h	PTPED MAC	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0458h	PTPED MAC	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0464h	PTPED MAC	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0468h	PTPED MAC	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0470h	PTPED MAC	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0478h	PTPED MAC	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 047Ch	PTPED MAC	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04C8h	PTPED MAC	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04CCh	PTPED MAC	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D4h	PTPED MAC	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D8h	PTPED MAC	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0500h	EPTPC	PTP Reset Register	PTRSTR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 0504h	EPTPC	STCA Clock Select Register	STCSELR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 1200h	MTU3	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (52 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C85h	MTU5	Timer Control Register 2	TCR2U	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C95h	MTU5	Timer Control Register 2	TCR2V	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA5h	MTU5	Timer Control Register 2	TCR2W	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2002h	GPT	Noise Filter Control Register	NFCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register	GTHSCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Ah	GPT0	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA

Table 4.1 List of I/O Registers (Address Order) (65 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0470h	USBA	Pipe1 Control Register	PIPE1CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0472h	USBA	Pipe2 Control Register	PIPE2CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0474h	USBA	Pipe3 Control Register	PIPE3CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0476h	USBA	Pipe4 Control Register	PIPE4CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0478h	USBA	Pipe5 Control Register	PIPE5CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Ah	USBA	Pipe6 Control Register	PIPE6CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Ch	USBA	Pipe7 Control Register	PIPE7CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Eh	USBA	Pipe8 Control Register	PIPE8CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0480h	USBA	Pipe9 Control Register	PIPE9CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0490h	USBA	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0492h	USBA	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0494h	USBA	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0496h	USBA	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0498h	USBA	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 049Ah	USBA	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA

Table 5.27 MTU3 Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 5.38
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH} , t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 5.39
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc} : PCLKA cycle

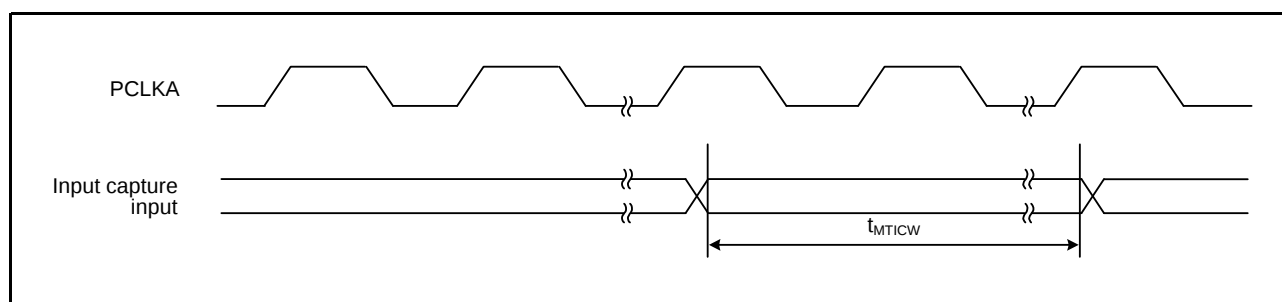
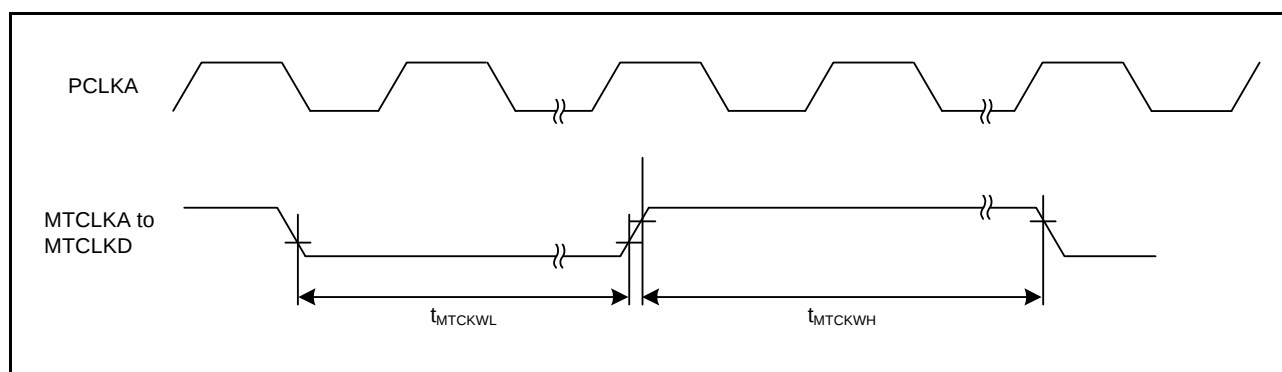
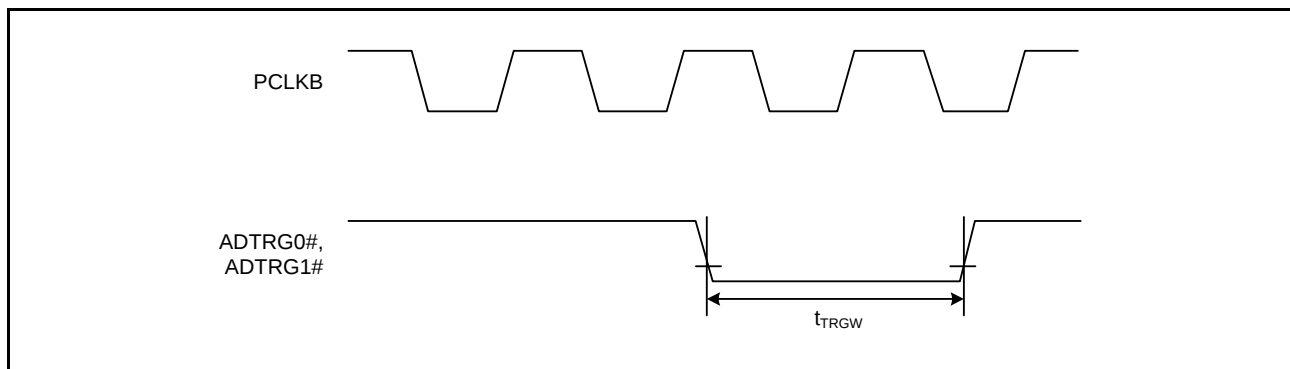
**Figure 5.38 MTU3 Input Capture Input Timing****Figure 5.39 MTU3 Clock Input Timing**

Table 5.30 A/D Converter Trigger Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 5.43

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.43 A/D Converter Trigger Input Timing****Table 5.31 CAC Timing**

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1	Max.	Unit*1	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$	t_{CACREF}	$4.5 t_{cac} + 3 t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{cac}$		$5 t_{cac} + 6.5 t_{PBcyc}$	—		

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. t_{CAC} : CAC count clock source cycle

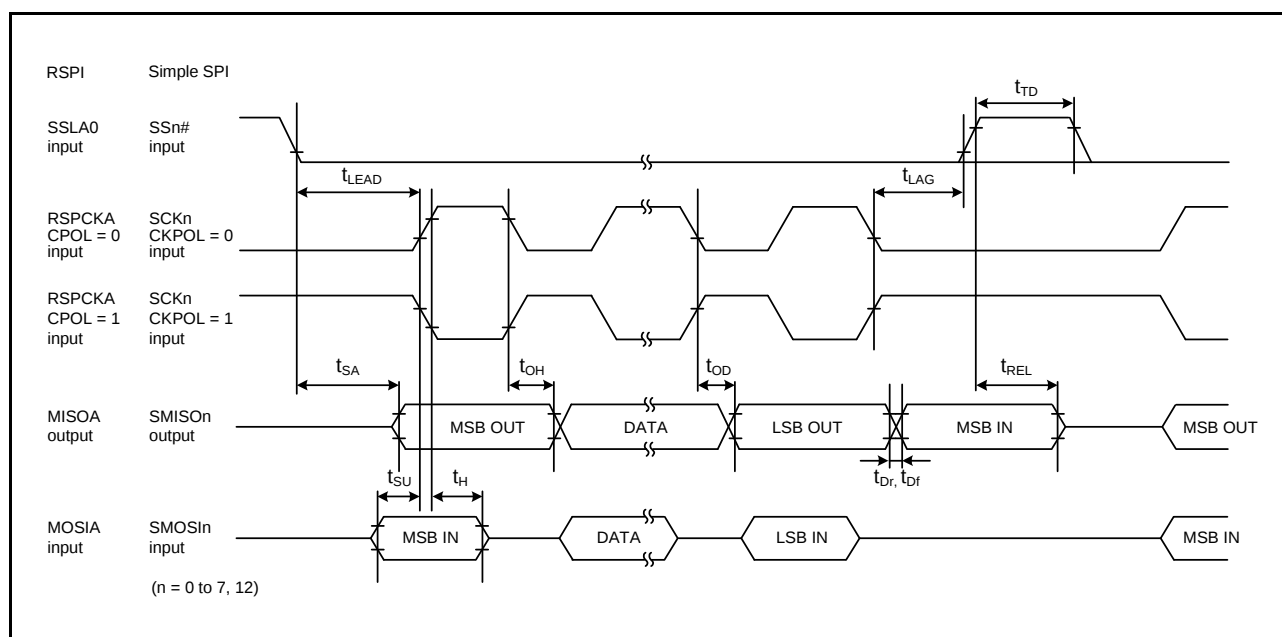


Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

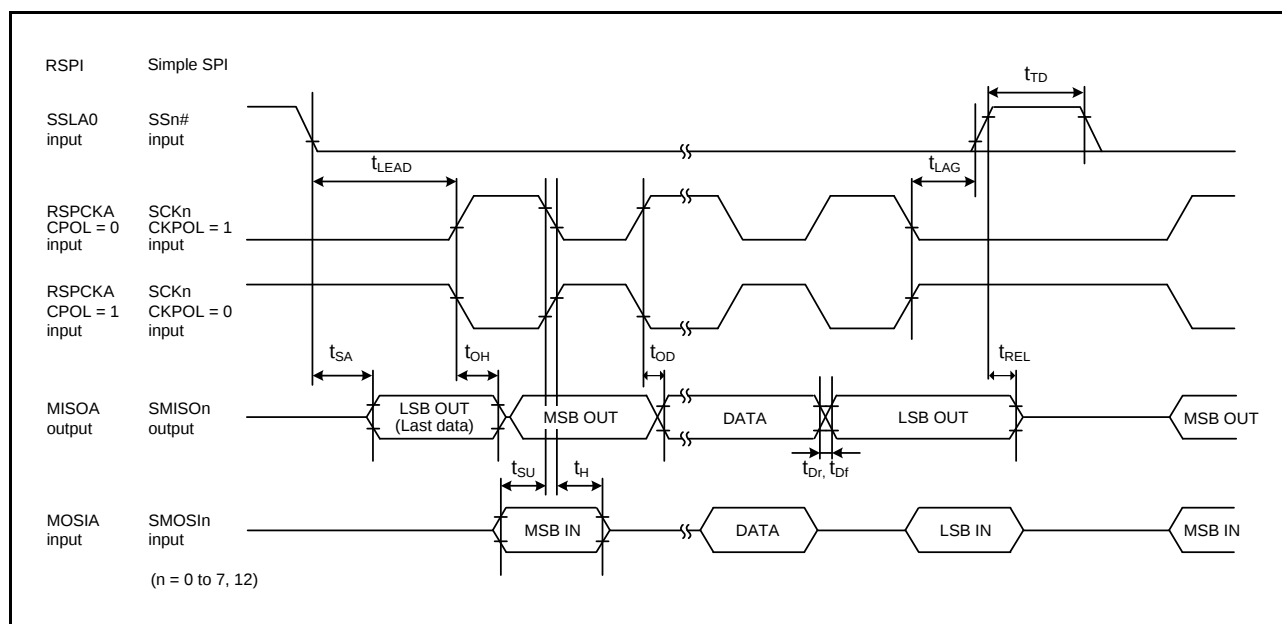


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

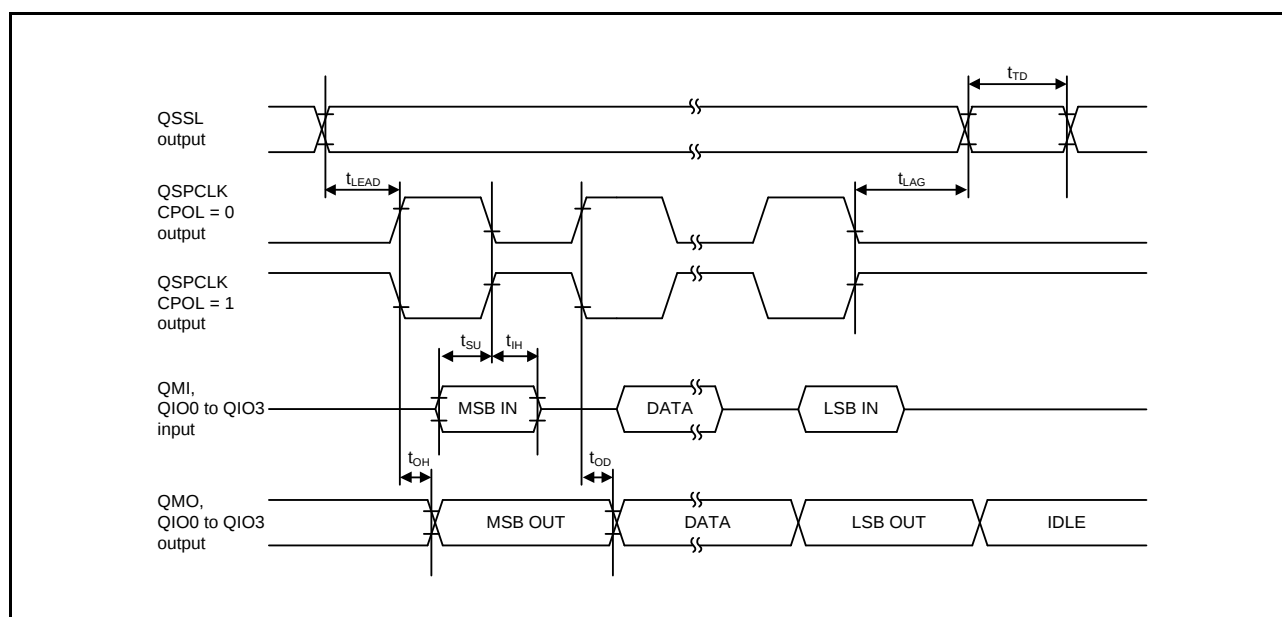


Figure 5.55 Transmit/Receive Timing (CPHA = 1)

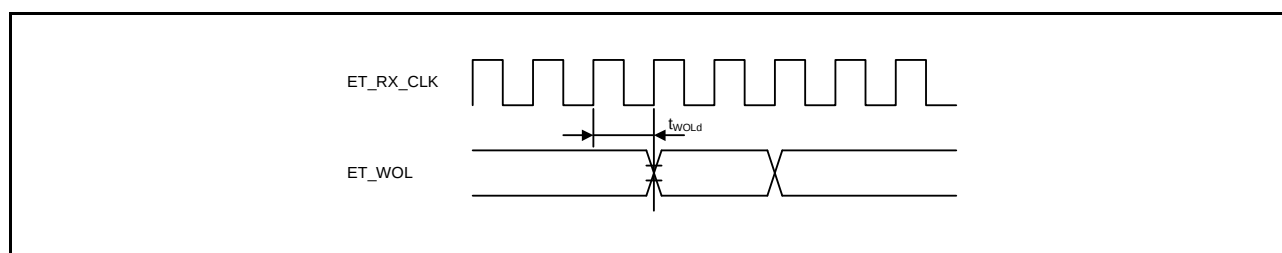
**Figure 5.71 WOL Output Timing (MII)**

Table 5.44 Battery Charge Characteristics (USBA only)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA =$
 $AVSS_USBA = 0$ V, $USBA_RREF = 2.2$ k $\Omega \pm 1\%$, $USBMCLK = 20/24$ MHz, $PCLKA = 8$ to 120 MHz,
 $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
D+ sink current	I_{DP_SINK}	25	175	μA	
D- sink current	I_{DM_SINK}	25	175	μA	
DCD source current	I_{DP_SRC}	7	13	μA	
Data detection voltage	V_{DAT_REF}	0.25	0.4	V	
D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

5.6 D/A Conversion Characteristics

Table 5.48 D/A Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V,
 $2.7 \leq V_{REFH0} \leq AVCC0$, $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Without AMP output	Absolute accuracy	—	—	± 6.0	LSB	2-M Ω resistive load 10-bit conversion
	DNL differential nonlinearity error	—	± 1.0	± 2.0	LSB	2-M Ω resistive load
	RO output resistance	—	7.5	—	k Ω	
	Conversion time	—	—	3.0	μ s	20-pF capacitive load
With AMP output	Resistive load	5	—	—	k Ω	
	Capacitive load	—	—	50	pF	
	Output voltage range	0.2	—	$AVCC1 - 0.2$	V	
	DNL differential nonlinearity error	—	± 1.0	± 2.0	LSB	
	INL integral nonlinearity error	—	± 2.0	± 4.0	LSB	
	Conversion time	—	—	4.0	μ s	

5.7 Temperature Sensor Characteristics

Table 5.49 Temperature Sensor Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	± 1	—	$^{\circ}$ C	
Temperature slope	—	3.8	—	mV/ $^{\circ}$ C	
Output voltage (at 25 $^{\circ}$ C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	μ s	
Sampling time*1	4.15	—	—	μ s	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

5.9 Oscillation Stop Detection Timing

Table 5.51 Oscillation Stop Detection Circuit Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.83

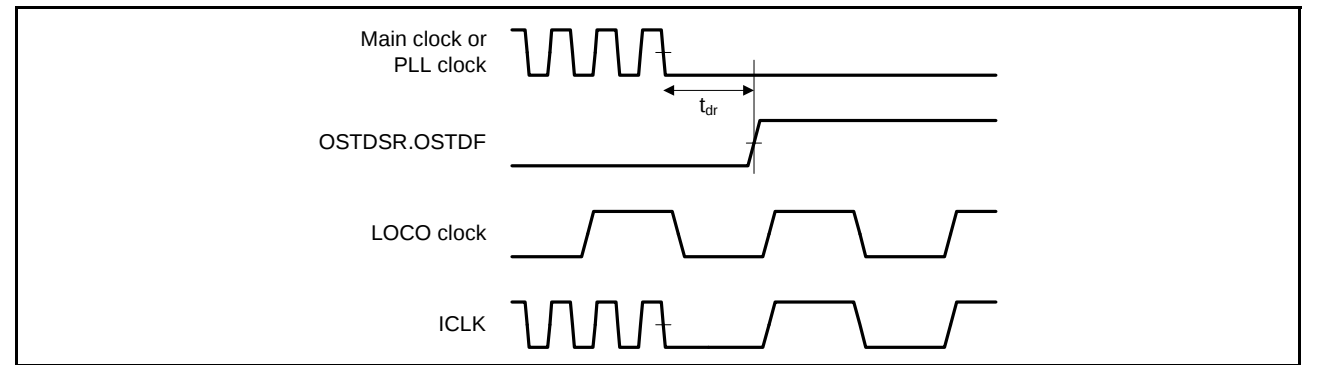


Figure 5.83 Oscillation Stop Detection Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

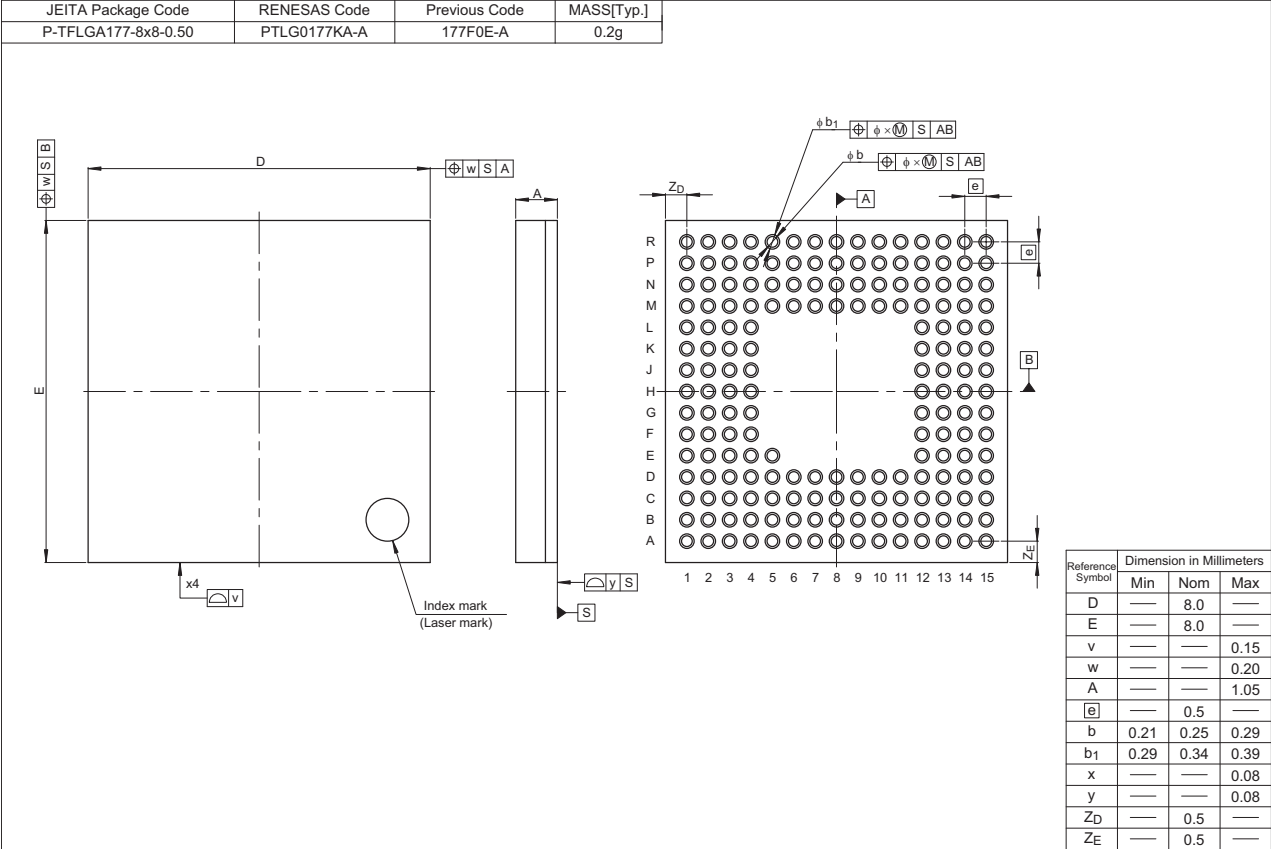


Figure A 177-Pin TFLGA (PTLG0177KA-A)

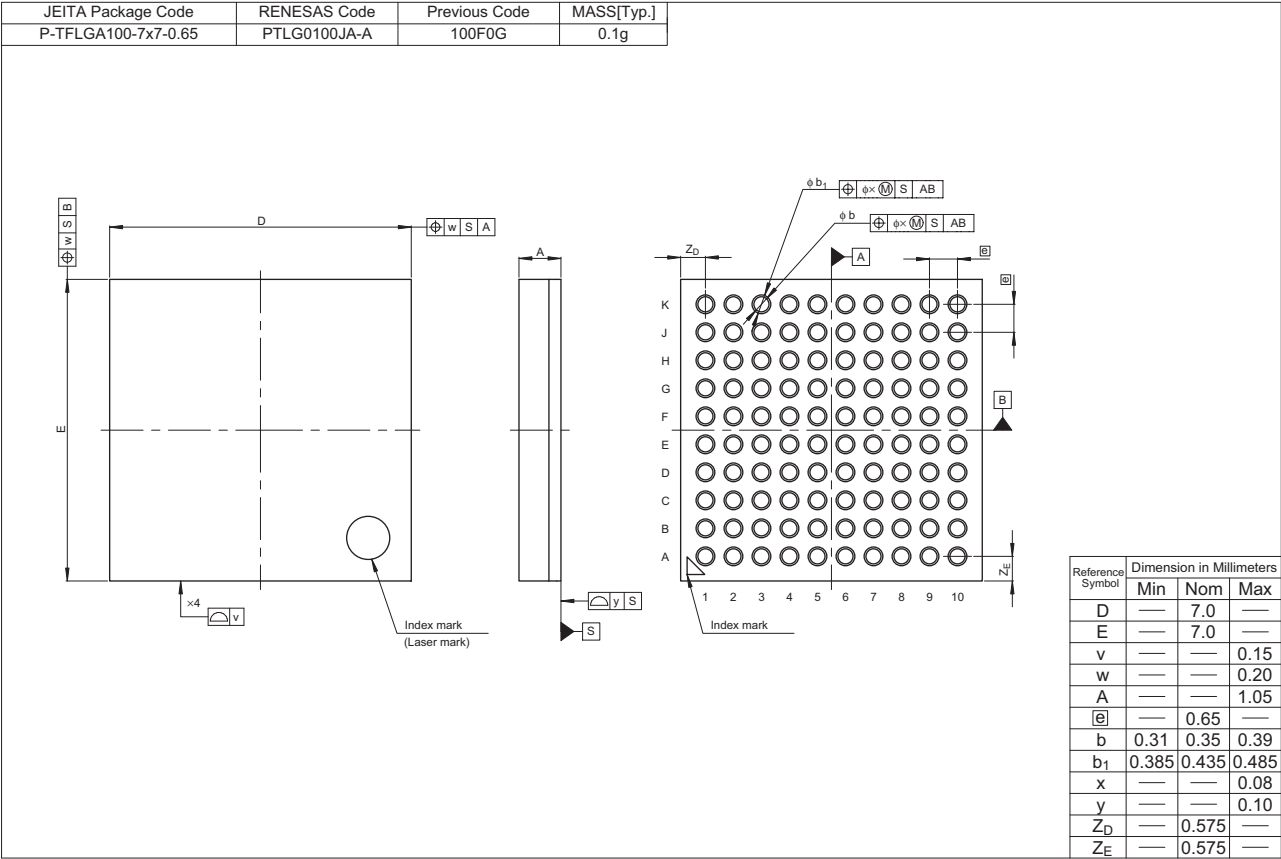


Figure F 100-Pin TFLGA (PTLG0100JA-A)