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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgcdbg-21

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICKL), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICKL): Up to 120 MHz Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt. • Voltage detection circuit 0 - Capable of generating an internal reset - The option-setting memory can be used to select enabling or disabling of the reset. - Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V) • Voltage detection circuits 1 and 2 - Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V) - Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) - Capable of generating an internal reset • Two types of timing are selectable for release from reset - An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable - Voltage detection monitoring - Event linking
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes - Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.

Table 1.1 Outline of Specifications (5/9)

Classification	Module/Function	Description
Timers	General PWM timer (GPTA)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Four clock sources independently selectable for all channels (PCLKA/1, PCLKA/4, PCLKA/8, PCLKA/16) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • Digital filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCd)	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC

Table 1.1 Outline of Specifications (8/9)

Classification	Module/Function	Description
	Parallel data capture unit (PDC)	1 channel - Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals - Setting of the image size when clipping of the output for a one-frame image is required
	12-bit A/D converter (S12ADC)	12 bits × 2 units (unit 0: 8 channels; unit 1: 21 channels) 12-bit resolution (switchable between 8, 10, and 12 bits) - Conversion time 0.48 μs per channel (for 12-bit conversion) 0.45 μs per channel (for 10-bit conversion) 0.42 μs per channel (for 8-bit conversion) - Operating mode - Scan mode (single scan mode, continuous scan mode, or group scan mode) - Group A priority control (only for group scan mode) - Sample-and-hold function - Common sample-and-hold circuit included - In addition, channel-dedicated sample-and-hold function (3ch: in unit 0 only) included - Sampling variable - Sampling time can be set up for each channel. - Digital comparison - Method: Comparison to detect voltages above or below thresholds and window comparison - Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion - Self-diagnostic function - The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) - Double trigger mode (A/D conversion data duplicated) - Detection of analog input disconnection - Three ways to start A/D conversion - Software trigger, timer (MTU3, GPT, TMR, TPU) trigger, external trigger - Event linking by the ELC
	12-bit D/A converter (R12DA)	2 channels 12-bit resolution - Output voltage: 0.2 V to AVCC1 – 0.2 V (amplifier output), 0 V to AVCC1 (direct output) - Output via an amplifier or direct output can be selected. - Event linking by the ELC
	Temperature sensor	1 channel - Relative precision: ±1°C - The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
	Safety	
	Memory protection unit (MPU)	- Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. - Minimum protection unit: 16 bytes - Reading from, writing to, and enabling the execution access can be specified for each area. - An address exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	- Protects against the reading of programs from blocks 8 and 9 of the code flash memory - Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRC)	- CRC code generation for arbitrary amounts of data in 8-bit units - Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ - Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop function	Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDG-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU or GPT in the high impedance state

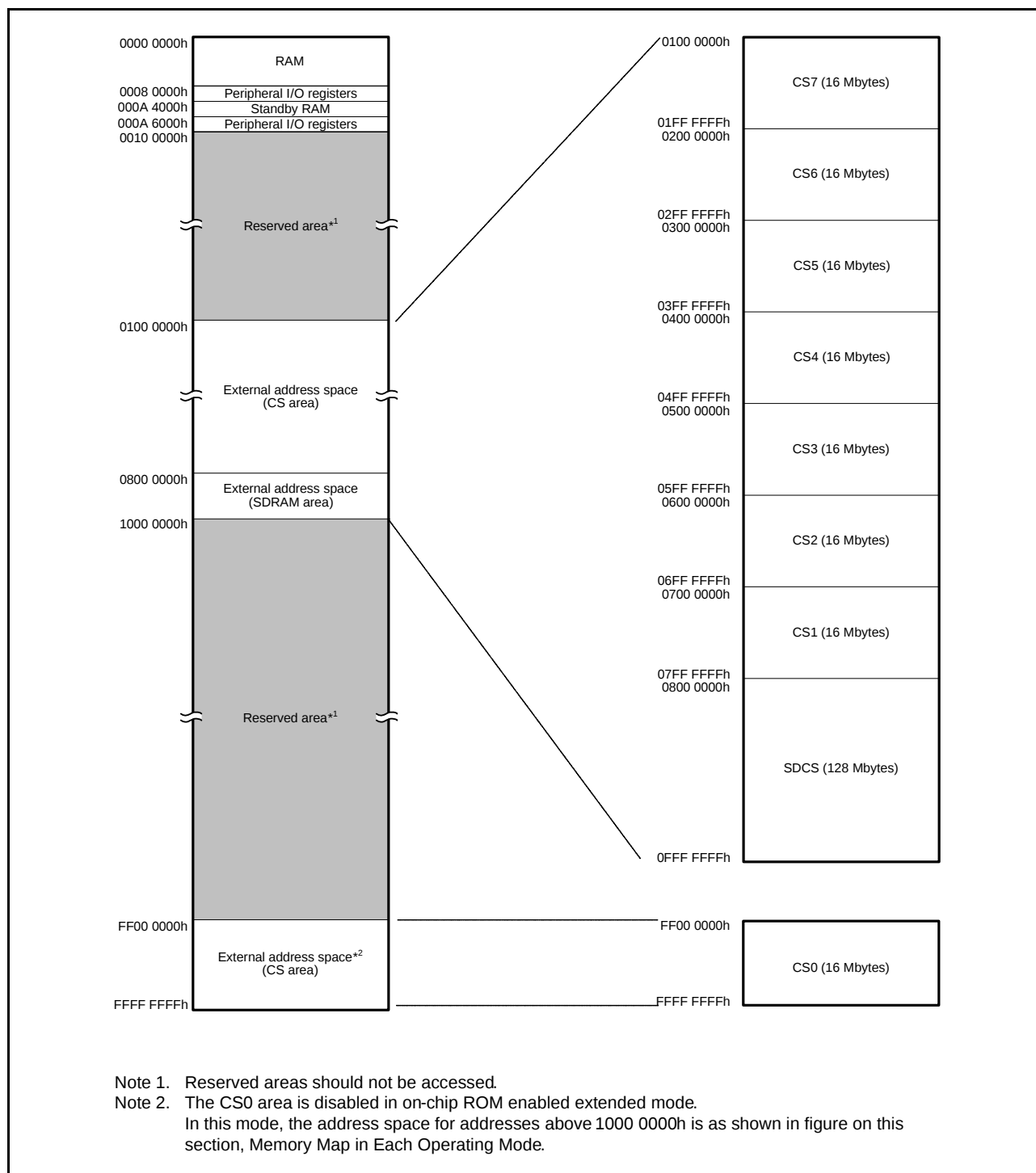
Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2	AVCC0							
A3	VREFL0							
A4		P42					IRQ10-DS	AN002
A5		P46					IRQ14-DS	AN006
A6	VCC							
A7	VSS							
A8		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
A9	VCC							
A10		P97	A23/D23		ET1_ERXD3			
A11		PD6	D6[A6/D6]	MTIOC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A12		P60	CS0#		ET1_TX_EN/ RMII1_TXD_EN			
A13		P63	CS3#/CAS#					
A14		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12	MMC_D5-B		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/ RXDX12	MMC_D6-B	IRQ7-DS	AN100
B1		P05					IRQ13	DA1
B2		P07					IRQ15	ADTRG0#
B3		P40					IRQ8-DS	AN000
B4		P41					IRQ9-DS	AN001
B5		P47					IRQ15-DS	AN007
B6		P91	A17/D17		ET1_COL/SCK7			AN115
B7		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
B8		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
B9		P96	A22/D22		ET1_ERXD2			
B10		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B11		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
B12	VSS							
B13		P64	CS4#/WE#					
B14		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12	MMC_D4-B		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ ET0_ERXD3	MMC_D7-B		AN101
C1	AVSS1							
C2	AVCC1							
C3	VREFH0							

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (7 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK		Buses
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK		Buses
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK		Buses
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK		Buses
0008 3842h	BSC	CS4 Control Register	CS4CR	16	16	1, 2 BCLK		Buses
0008 384Ah	BSC	CS4 Recovery Cycle Register	CS4REC	16	16	1, 2 BCLK		Buses
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU

Table 4.1 List of I/O Registers (Address Order) (16 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR01	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8209h	TMR1	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR01	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Dh	TMR1	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8219h	TMR3	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Dh	TMR3	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	CRC
0008 8300h	RIIC0	I ² C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8301h	RIIC0	I ² C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8302h	RIIC0	I ² C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8303h	RIIC0	I ² C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8304h	RIIC0	I ² C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8305h	RIIC0	I ² C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8306h	RIIC0	I ² C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8307h	RIIC0	I ² C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8308h	RIIC0	I ² C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8309h	RIIC0	I ² C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa

Table 4.1 List of I/O Registers (Address Order) (17 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8310h	RIIC0	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8311h	RIIC0	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8312h	RIIC0	I ² C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8313h	RIIC0	I ² C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I ² C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I ² C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I ² C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I ² C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I ² C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I ² C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I ² C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I ² C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I ² C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I ² C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I ² C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I ² C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8528h	MMCIF	Response Register 1	CERESP1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 852Ch	MMCIF	Response Register 0	CERESP0	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8530h	MMCIF	Automatically Issued CMD12 Response Register	CERESPCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8534h	MMCIF	Data Register	CEDATA	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 853Ch	MMCIF	Boot Operation Setting Register	CEBOOT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8540h	MMCIF	Interrupt status Flag Register	CEINT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8544h	MMCIF	Interrupt request Enable Register	CEINTEN	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8548h	MMCIF	Status Register 1	CEHOSTSTS1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 854Ch	MMCIF	Status Register 2	CEHOSTSTS2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8570h	MMCIF	MMC Detection and Port Control Register	CEDETECT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8574h	MMCIF	Special Mode Setting Register	CEADDMODE	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (20 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSE R	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR 0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR 1	16	16	2, 3 PCLKB	2 ICLK	S12ADC

Table 4.1 List of I/O Registers (Address Order) (42 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 42A0h	CMTW1	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 42A4h	CMTW1	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 8000h to 0009 D6BFh	SRC	Filter Coefficient Table	SRCFCTR0 to 5551	32	32	4, 5 PCLKB	2, 3 ICLK	SRC
0009 DFF0h	SRC	Input Data Register	SRCID	32	32	5, 6 PCLKB	2, 3 ICLK	SRC
0009 DFF4h	SRC	Output Data Register	SRCOD	32	32	5, 6 PCLKB	2, 3 ICLK	SRC
0009 DFF8h	SRC	Input Data Control Register	SRCIDCTRL	16	16	4, 5 PCLKB	2, 3 ICLK	SRC
0009 DFFAh	SRC	Output Data Control Register	SRCODCTRL	16	16	4, 5 PCLKB	2, 3 ICLK	SRC
0009 DFFCh	SRC	Control Register	SRCCTRL	16	16	4, 5 PCLKB	2, 3 ICLK	SRC
0009 DFFEh	SRC	Status Register	SRCSTAT	16	16	4, 5 PCLKB	2, 3 ICLK	SRC
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	8, 16	3, 4 PCLKB	2 ICLK	USBb
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	USBb
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb
000A 004Eh	USB0	Device State Change Register	DVCHGR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBb

Table 4.1 List of I/O Registers (Address Order) (44 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a

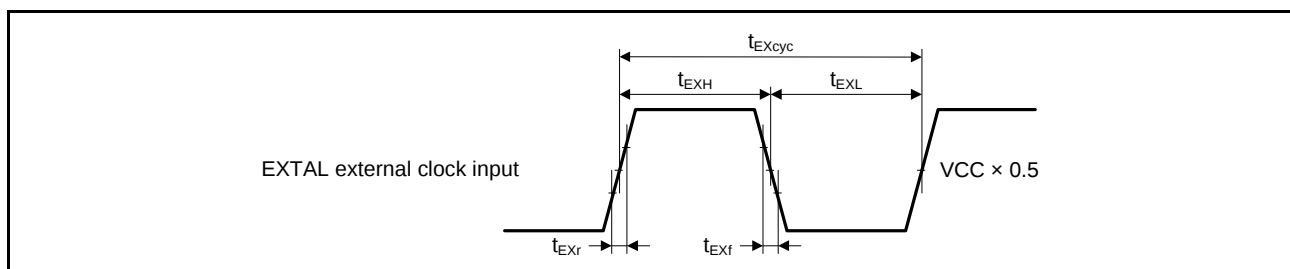
Table 4.1 List of I/O Registers (Address Order) (65 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 0470h	USBA	Pipe1 Control Register	PIPE1CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0472h	USBA	Pipe2 Control Register	PIPE2CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0474h	USBA	Pipe3 Control Register	PIPE3CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0476h	USBA	Pipe4 Control Register	PIPE4CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0478h	USBA	Pipe5 Control Register	PIPE5CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Ah	USBA	Pipe6 Control Register	PIPE6CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Ch	USBA	Pipe7 Control Register	PIPE7CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 047Eh	USBA	Pipe8 Control Register	PIPE8CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0480h	USBA	Pipe9 Control Register	PIPE9CTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0490h	USBA	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0492h	USBA	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0494h	USBA	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0496h	USBA	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 0498h	USBA	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA
000D 049Ah	USBA	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than $1 + (3 + \text{BUSWAIT}) \times (\text{frequency ratio of ICLK/PCLKB})^5$	USBA

Table 5.12 EXTAL Clock Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.13 Main Clock Timing**

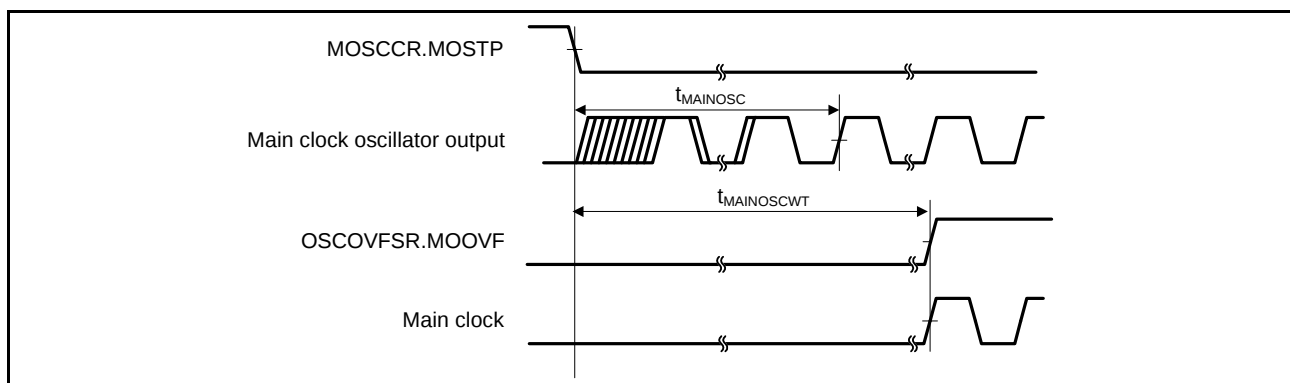
Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 5.5
Main clock oscillator stabilization wait time (crystal)	$t_{MAINSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINSCWT} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 5.5 Main Clock Oscillation Start Timing**

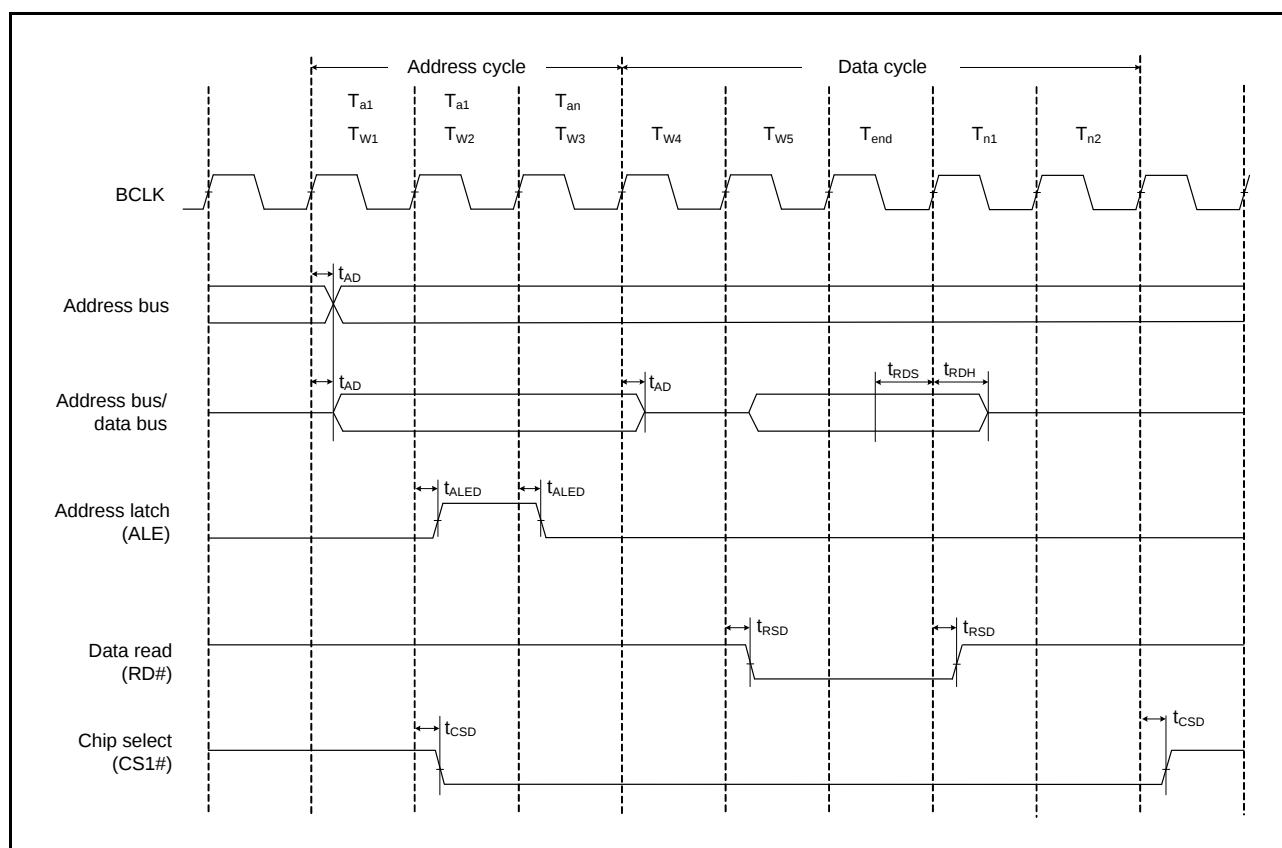


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

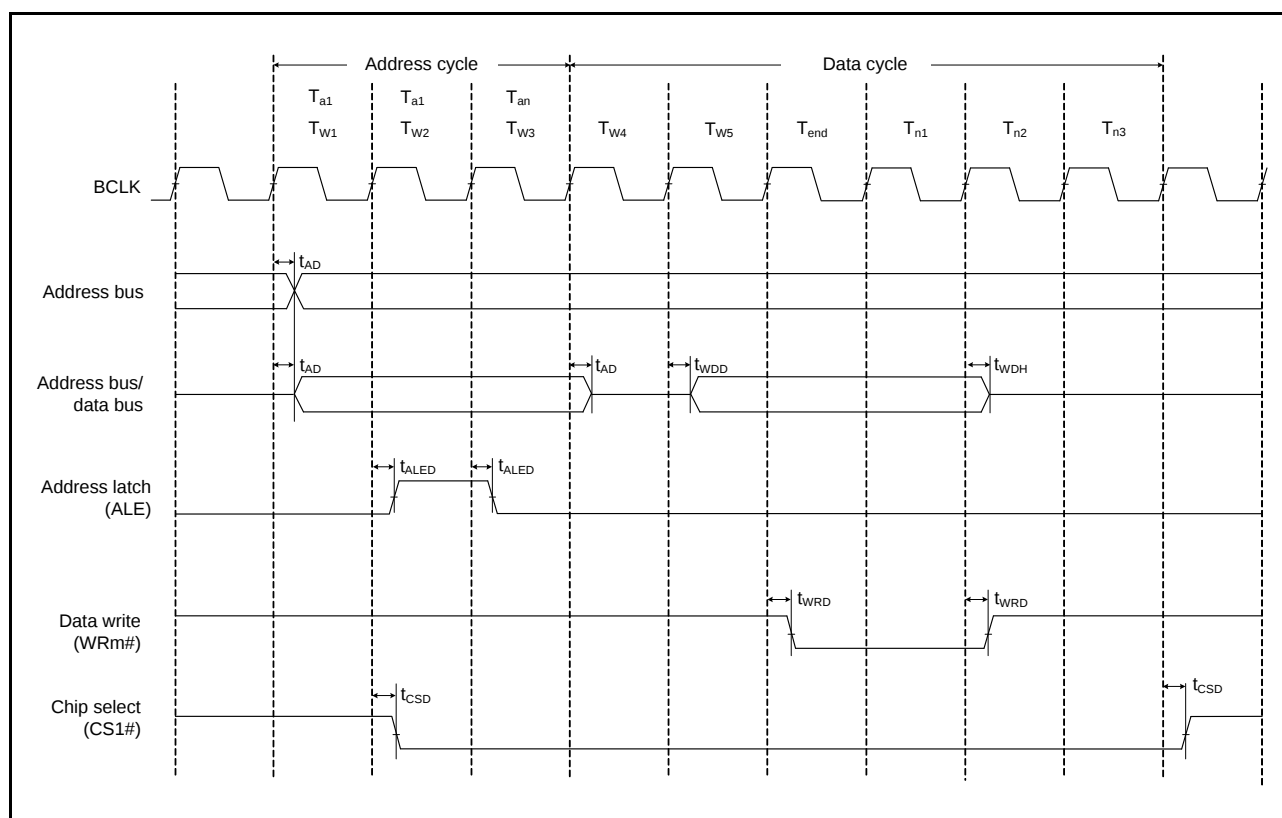


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing

5.3.7 Timing of On-Chip Peripheral Modules

Table 5.23 I/O Port Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 5.33

Note 1. t_{PBcyc} : PCLKB cycle

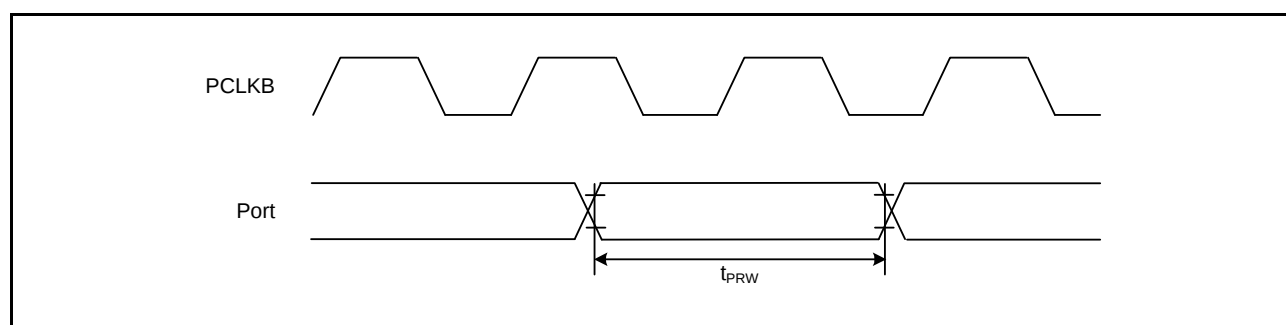
**Figure 5.33 I/O Port Input Timing**

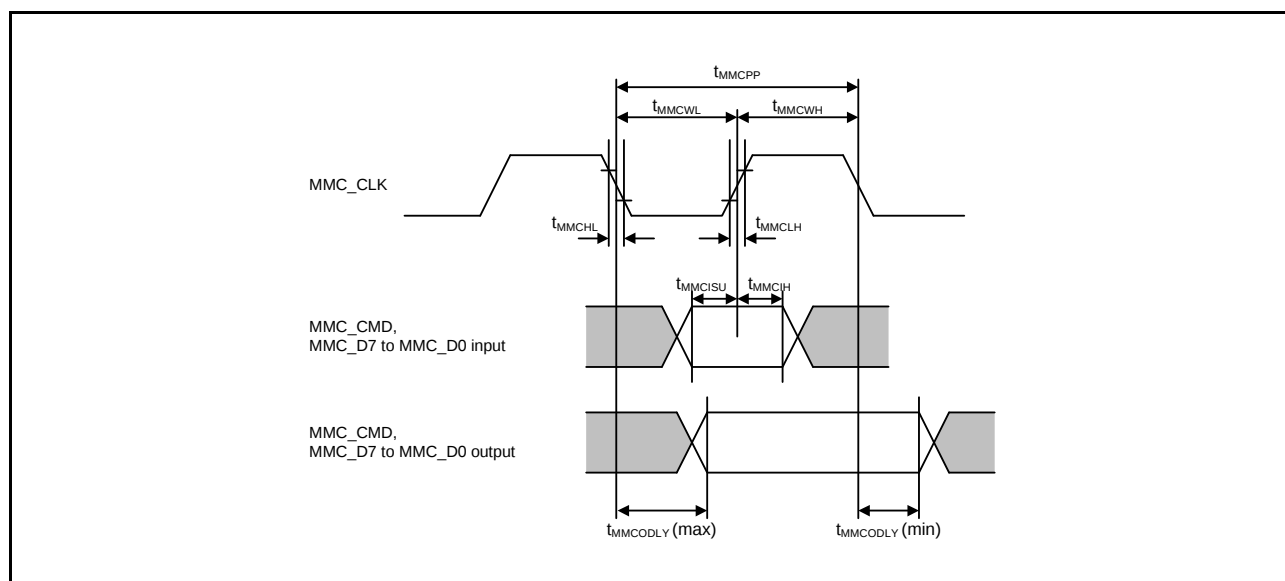
Table 5.39 MMC Host Interface Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.*1	Max.	Unit	Test Conditions*2
MMCIF	MMC_CLK clock cycle	$2 \times t_{PBcyc}$	—	ns	Figure 5.61
	MMC_CLK clock high level width	6.5	—	ns	
	MMC_CLK clock low level width	6.5	—	ns	
	MMC_CLK clock rising time	—	5	ns	
	MMC_CLK clock falling time	—	5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode)	-6.5	6.5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data setup	8	—	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data hold	2	—	ns	

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups.
For the MMC interface, the AC portion of the electrical characteristics is measured for each group.

**Figure 5.61 MMC Interface**

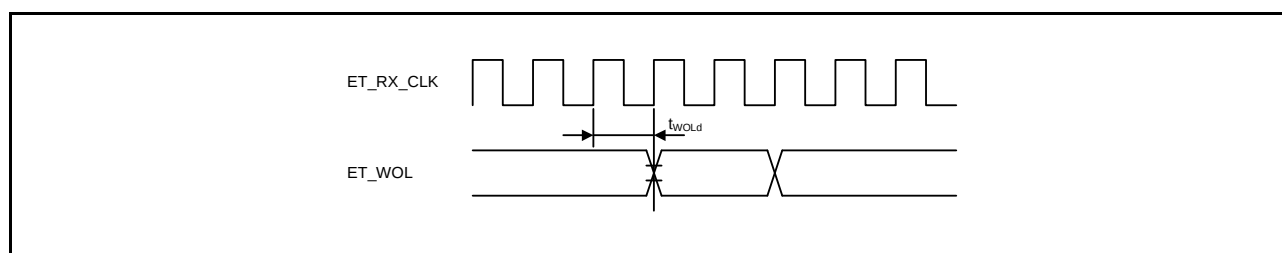
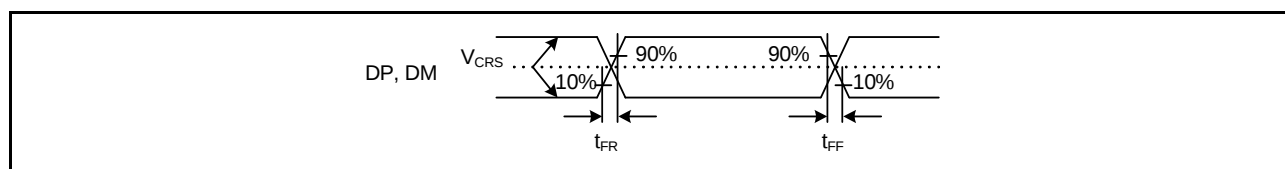
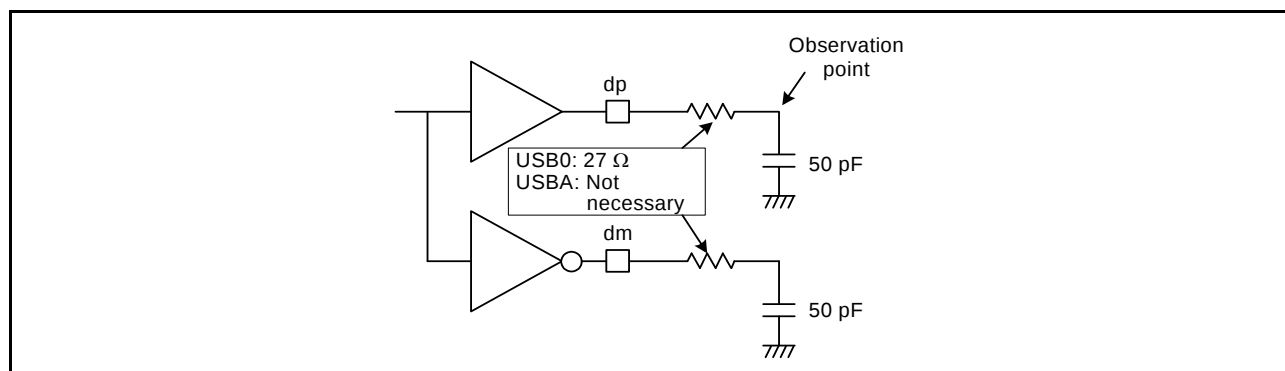
**Figure 5.71 WOL Output Timing (MII)**

Table 5.43 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $USBA_RREF = 2.2$ k $\Omega \pm 1\%$, $USBMCLK = 20/24$ MHz, $UCLK = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V
	Input low level voltage	V_{IL}	—	—	0.8	V
	Differential input sensitivity	V_{DI}	0.2	—	—	V DP – DM
	Differential common mode range	V_{CM}	0.8	—	2.5	V
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V $I_{OH} = -200$ μ A
	Output low level voltage	V_{OL}	0.0	—	0.3	V $I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V Figure 5.77
	Rise time	t_{FR}	4	—	20	ns
	Fall time	t_{FF}	4	—	20	ns
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	% t_{FR} / t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω USBFS: $R_s = 27$ Ω included
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	k Ω Idle state
		R_{pu}	1.425	—	3.090	k Ω At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω

**Figure 5.77 DP and DM Output Timing (Full-Speed)****Figure 5.78 Test Circuit (Full-Speed)**

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