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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgcdfc-v1

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
Timers	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) • 14 of the signals are available for channel 0, 12 are available for channel 2, 11 are available for channels 1, 3, 4, 6 to 8, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode • Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode • Outputs non-overlapping waveforms for controlling 3-phase inverters • Automatic specification of dead times • PWM duty cycle: Selectable as any value from 0% to 100% • Delay can be applied to requests for A/D conversion. • Non-generation of interrupt requests at peak or trough values of counters can be selected. • Double buffer configuration • Reset synchronous PWM mode • Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU3/GPT's waveform output pins • 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
P2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOC0B/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
P3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOC0B5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
P5					USB0_DP			
P6	AVSS_ USBA							
P7					USBA_DM			
P8		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
P9		P52	RD#		RXD2/SMISO2/ SSCL2			
P10		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
P13		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV/	MMC_CD-A/ SDHI_D3-A		
P14		P75	CS5#	PO20	SCK11/RTS11/ ET0_ERXD0/ RMII0_RXD0/	MMC_RES#-A/ SDHI_D2-A		
P15	VCC							
R1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOC0B3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOC0B1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
R4		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
R5					USB0_DM			
R6	PVSS_ USBA							
R7					USBA_DP			
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN			
R9		P53*2	BCLK					
R10	VSS							

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
85		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
86		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
87		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
88		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
89		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
90	VCC							
91		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
92	VSS							
93		P73	CS3#	PO16	ET0_WOL			
94		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
95		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
97		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
99		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/ RTS4#/ SS4#/ SS6#/ ET0_RX_CLK/ REF50CK0			
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC			
102		P71	A18/CS1#		ET0_MDIO			
103	VCC							
104		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
105	VSS							
106		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
107		PA6	A6	MTIC5V/MTCLKB/ GTETR-G/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/ RTS5#/ SS5#/ MOSIA-B/ ET0_EXOUT			
108		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	

Table 4.1 List of I/O Registers (Address Order) (24 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A068h	SCI3	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A069h	SCI3	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Ah	SCI3	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Bh	SCI3	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Ch	SCI3	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Dh	SCI3	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Eh	SCI3	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Fh	SCI3	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A06Eh	SCI3	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A070h	SCI3	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A071h	SCI3	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A070h	SCI3	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A072h	SCI3	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A080h	SCI4	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A081h	SCI4	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A082h	SCI4	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A083h	SCI4	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A084h	SCI4	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A085h	SCI4	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A086h	SMCI4	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A087h	SCI4	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A088h	SCI4	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A089h	SCI4	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ah	SCI4	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Bh	SCI4	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Ch	SCI4	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Dh	SCI4	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Fh	SCI4	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h
0008 A08Eh	SCI4	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SC1h
0008 A090h	SCI4	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SC1h

Table 4.1 List of I/O Registers (Address Order) (28 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2, 3 PCLKB	2 ICLK	CAC
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2, 3 PCLKB	2 ICLK	CAC
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2, 3 PCLKB	2 ICLK	DOC
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2, 3 PCLKB	2 ICLK	DOC
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B101h	ELC	Event Link Setting Register 0	ELSR0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Ch	ELC	Event Link Setting Register 11	ELSR11	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B10Eh	ELC	Event Link Setting Register 13	ELSR13	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B131h	ELC	Event Link Setting Register 33	ELSR33	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B133h	ELC	Event Link Setting Register 35	ELSR35	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B134h	ELC	Event Link Setting Register 36	ELSR36	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B135h	ELC	Event Link Setting Register 37	ELSR37	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B136h	ELC	Event Link Setting Register 38	ELSR38	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B139h	ELC	Event Link Setting Register 41	ELSR41	8	8	2, 3 PCLKB	2 ICLK	ELC

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1854h	CAN1	Time Stamp Register	TSR	16	16	2, 3 PCLKB	2 ICLK	CAN
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2200h to 0009 23FFh	CAN2	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 2400h to 0009 241Fh	CAN2	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2420h	CAN2	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2424h	CAN2	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2428h	CAN2	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 242Ch	CAN2	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2820h to 0009 283Fh	CAN2	Message Control Registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2840h	CAN2	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2842h	CAN2	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2844h	CAN2	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2848h	CAN2	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ah	CAN2	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Bh	CAN2	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ch	CAN2	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Dh	CAN2	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Eh	CAN2	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Fh	CAN2	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2850h	CAN2	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2851h	CAN2	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2852h	CAN2	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2853h	CAN2	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2854h	CAN2	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2856h	CAN2	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2858h	CAN2	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 4200h	CMTW0	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4204h	CMTW0	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4208h	CMTW0	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4210h	CMTW0	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4214h	CMTW0	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4218h	CMTW0	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 421Ch	CMTW0	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4220h	CMTW0	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4224h	CMTW0	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4280h	CMTW1	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4284h	CMTW1	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4288h	CMTW1	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4290h	CMTW1	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4294h	CMTW1	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4298h	CMTW1	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 429Ch	CMTW1	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW

Table 4.1 List of I/O Registers (Address Order) (45 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLKA	ICLK < PCLKA	
000C 0050h	EDMAC 0	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0058h	EDMAC 0	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0064h	EDMAC 0	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0068h	EDMAC 0	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 006Ch	EDMAC 0	Independent Output Signal Setting Register	IOSR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0070h	EDMAC 0	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0078h	EDMAC 0	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 007Ch	EDMAC 0	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 00C8h	EDMAC 0	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 00CCh	EDMAC 0	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 00D4h	EDMAC 0	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 00D8h	EDMAC 0	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0100h	ETHER C0	ETHERC Mode Register	ECMR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0108h	ETHER C0	Receive Frame Maximum Length Register	RFLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0110h	ETHER C0	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0118h	ETHER C0	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0120h	ETHER C0	PHY Interface Register	PIR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0128h	ETHER C0	PHY Status Register	PSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0140h	ETHER C0	Random Number Generation Counter Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0150h	ETHER C0	Interpacket Gap Register	IPGR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0154h	ETHER C0	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0158h	ETHER C0	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0160h	ETHER C0	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0164h	ETHER C0	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 0168h	ETHER C0	PAUSE Frame Retransmit Counter	TPAUSECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 016Ch	ETHER C0	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 01C0h	ETHER C0	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 01C8h	ETHER C0	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 01D0h	ETHER C0	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 01D4h	ETHER C0	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C
000C 01D8h	ETHER C0	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHER C

Table 4.1 List of I/O Registers (Address Order) (49 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 122Ah	MTU4	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 122Ch	MTU3	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 122Dh	MTU4	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1230h	MTU	Timer Interrupt Skipping Set Register 1A	TITCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1231h	MTU	Timer Interrupt Skipping Counter 1A	TITCNT1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1232h	MTU	Timer Buffer Transfer Set Register A	TBTERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1234h	MTU	Timer Dead Time Enable Register A	TDERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1236h	MTU	Timer Output Level Buffer Register A	TOLBRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1238h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1239h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Ah	MTU	Timer Interrupt Skipping Mode Register A	TITMRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Bh	MTU	Timer Interrupt Skipping Set Register 2A	TITCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 123Ch	MTU	Timer Interrupt Skipping Counter 2A	TITCNT2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1240h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1244h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1246h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1248h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Ch	MTU3	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 124Dh	MTU4	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1260h	MTU	Timer Waveform Control Register A	TWCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1270h	MTU	Timer Mode Register 2A	TMDR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1272h	MTU3	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1274h	MTU4	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1276h	MTU4	Timer General Register F	TGRF	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1280h	MTU	Timer Start Register A	TSTRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1281h	MTU	Timer Synchronous Register A	TSYRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1282h	MTU	Timer Counter Synchronous Start Register	TCSYSTR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1284h	MTU	Timer Read/Write Enable Register A	TRWERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1290h	MTU0	Noise Filter Control Register 0	NFCR0	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1291h	MTU1	Noise Filter Control Register 1	NFCR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1292h	MTU2	Noise Filter Control Register 2	NFCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1293h	MTU3	Noise Filter Control Register 3	NFCR3	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1294h	MTU4	Noise Filter Control Register 4	NFCR4	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1298h	MTU8	Noise Filter Control Register 8	NFCR8	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1299h	MTU0	Noise Filter Control Register C	NFCRC	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1300h	MTU0	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1301h	MTU0	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1302h	MTU0	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1303h	MTU0	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1304h	MTU0	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1306h	MTU0	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1308h	MTU0	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 130Ah	MTU0	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 130Ch	MTU0	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 130Eh	MTU0	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1320h	MTU0	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (51 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A10h	MTU6	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A14h	MTU	Timer Cycle Data Register B	TCDRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRBB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A20h	MTU	Timer Subcounter B	TCNTSB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A22h	MTU	Timer Cycle Buffer Register B	TCBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A31h	MTU	Timer Interrupt Skipping Counter 1B	TITCNT1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A3Ch	MTU	Timer Interrupt Skipping Counter 2B	TITCNT2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Ch	MTU6	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (57 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLKA	ICLK < PCLKA	
000C 4810h	EPTPC 0	SYNFP MAC Address Register	SYMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4814h	EPTPC 0	SYNFP MAC Address Register	SYMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 481Ch	EPTPC 0	SYNFP Local IP Address Register	SYIPADDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4840h	EPTPC 0	SYNFP Specification Version Setting Register	SYSPVRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4844h	EPTPC 0	SYNFP Domain Number Setting Register	SYDOMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4850h	EPTPC 0	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4854h	EPTPC 0	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4858h	EPTPC 0	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 485Ch	EPTPC 0	Delay_Resp Message Flag Field Setting Register	DYRPFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4860h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4864h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4868h	EPTPC 0	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4880h	EPTPC 0	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC

Table 5.15 HOCO Clock Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	$-20^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	$-40^{\circ}\text{C} \leq T_a < -20^{\circ}\text{C}$
		17.46	18	18.54	MHz	
		19.40	20	20.60	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	μs	Figure 5.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	μs	Figure 5.9

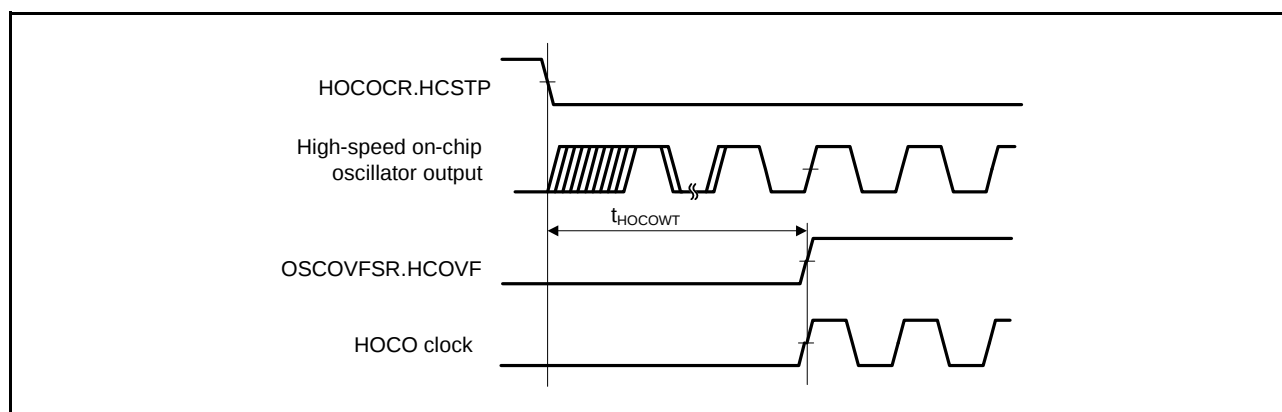
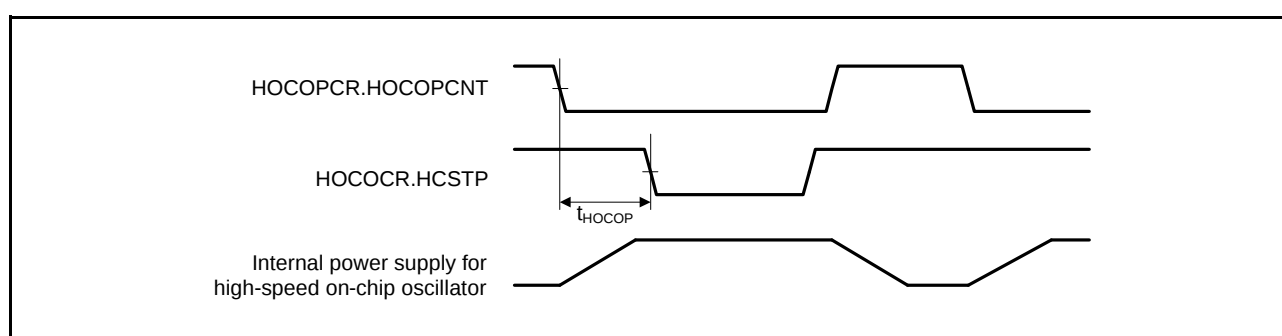
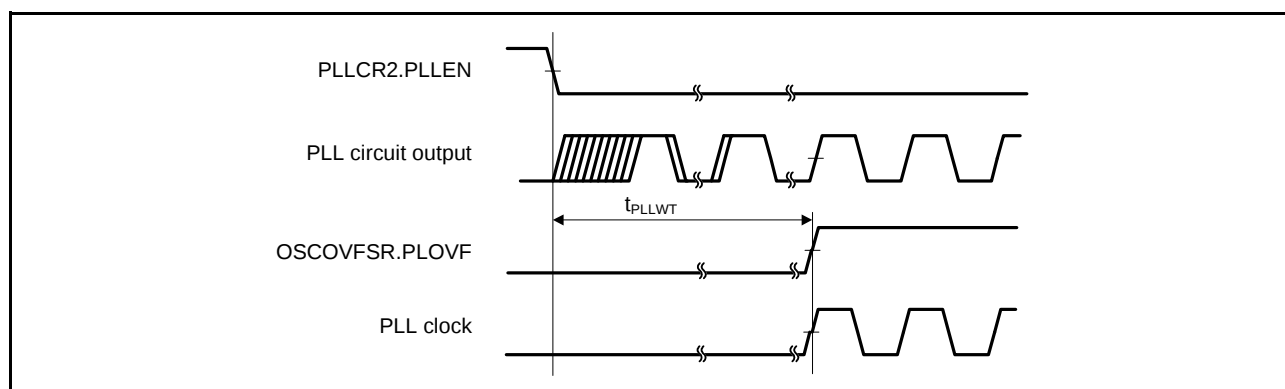
**Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)****Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing**

Table 5.16 PLL Clock Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization wait time	t_{PLLWT}	—	259	320	μ s	Figure 5.10

**Figure 5.10 PLL Clock Oscillation Start Timing****Table 5.17 Sub-Clock Timing**

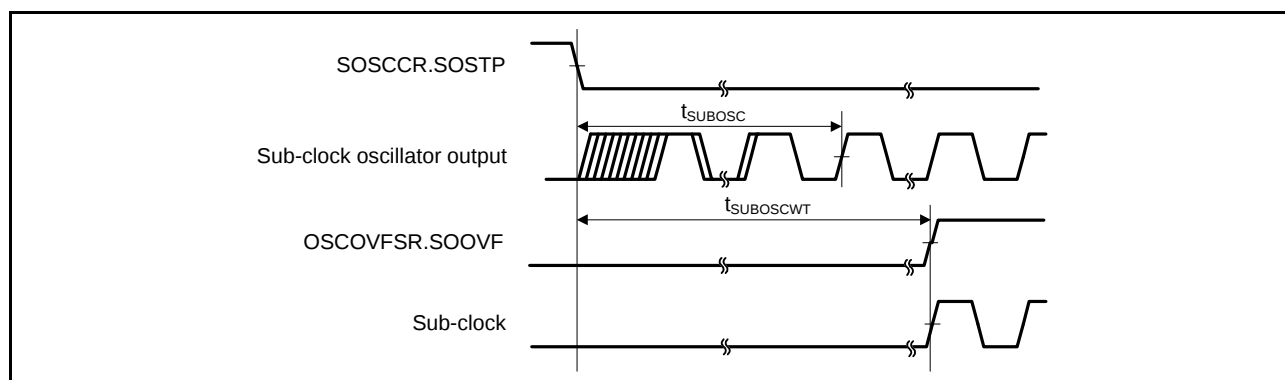
Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $V_{BATT} = 2.0$ to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 5.11
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the $SOSCWTCR.SSTS[7:0]$ bits determines the sub-clock oscillation stabilization wait time in accord with the formula below.

$$t_{SUBOSCWT} = [(SSTS[7:0] \text{ bits} \times 16384) + 10] / f_{LOCO}$$

**Figure 5.11 Sub-Clock Oscillation Start Timing**

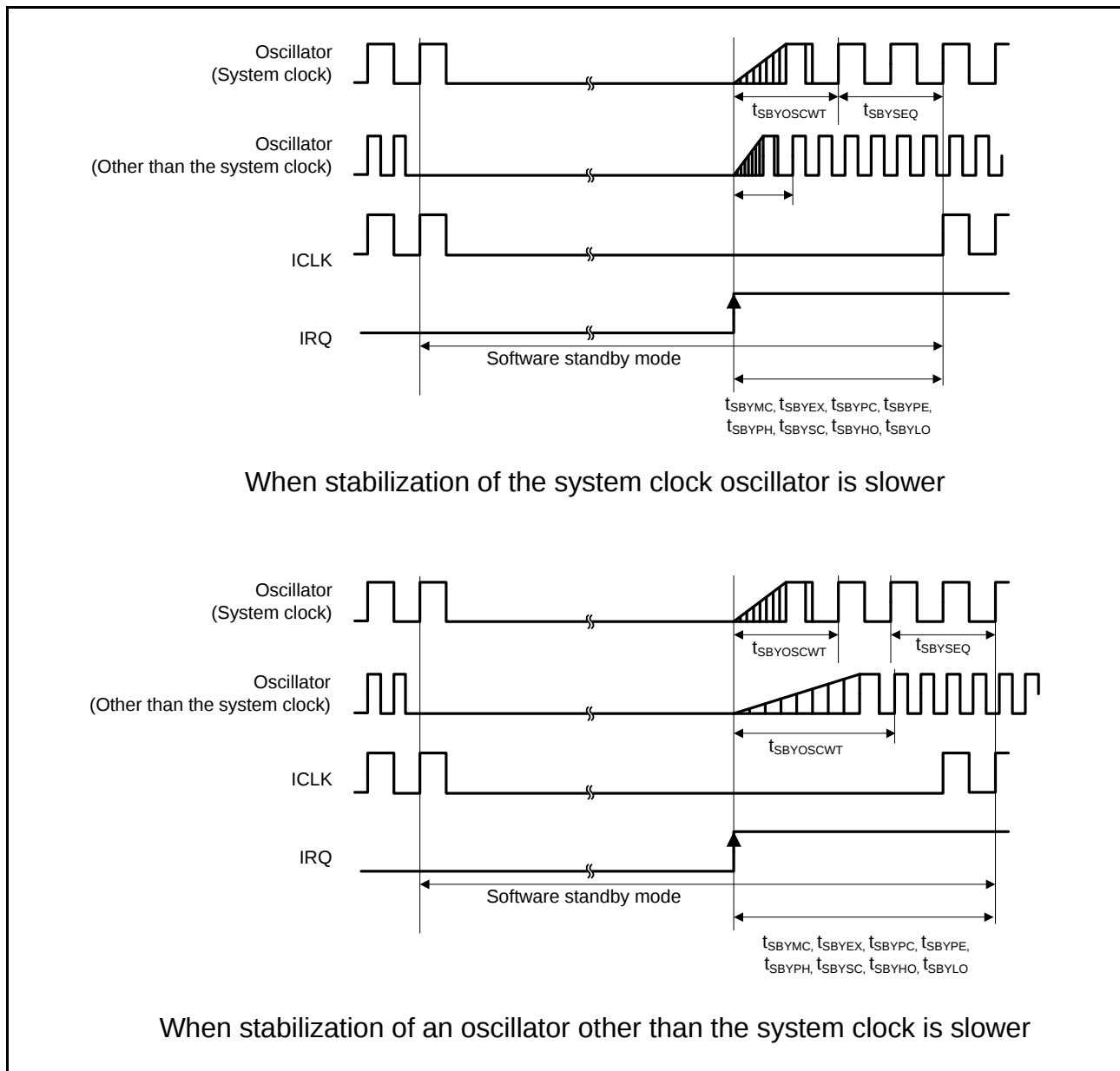


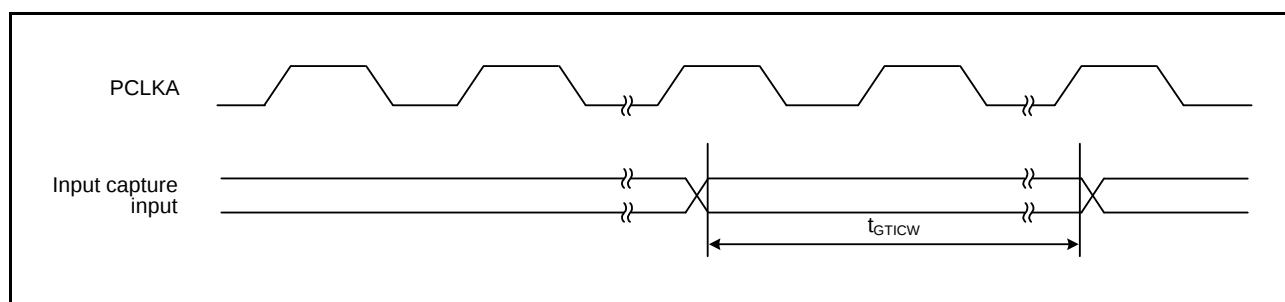
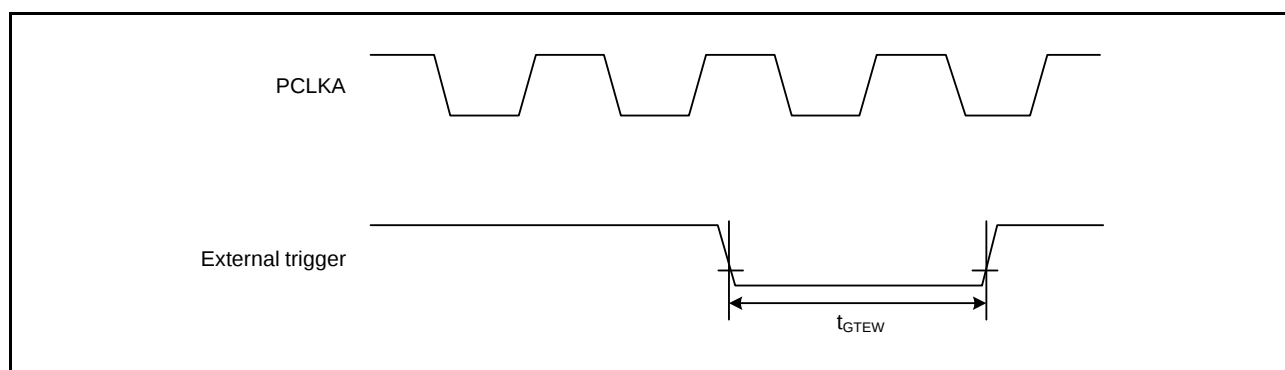
Figure 5.12 Software Standby Mode Cancellation Timing

Table 5.29 GPT Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PACyc}	Figure 5.41
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t_{OTETW}	1.5	—	t_{PACyc}	Figure 5.42
		Both-edge setting		2.5	—		

Note 1. t_{PACyc} : PCLKA cycle

**Figure 5.41 GPT Input Capture Input Timing****Figure 5.42 GPT External Trigger Input Timing**

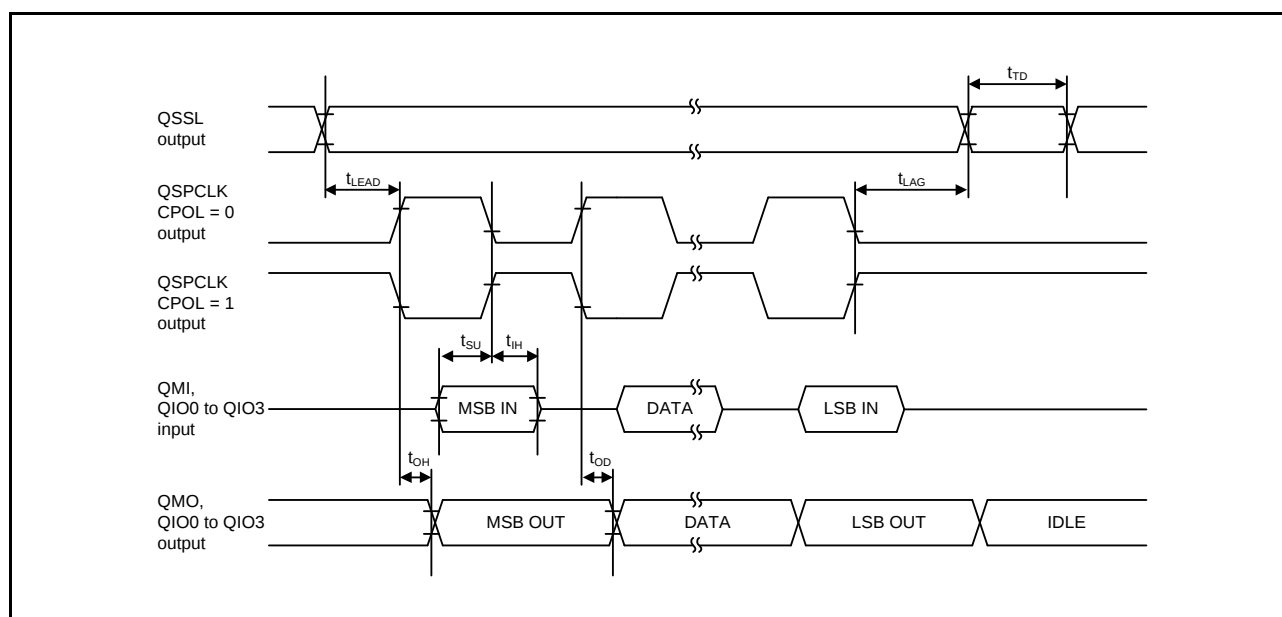


Figure 5.55 Transmit/Receive Timing (CPHA = 1)

Table 5.36 RIIC Timing (1)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 1300$	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 600$	—	ns	
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	SCL, SDA input rise time	t_{Sr}	$20 \times (\text{External pull-up voltage}/5.5V)$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 \times (\text{External pull-up voltage}/5.5V)$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 300$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 300$	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

Table 5.39 MMC Host Interface Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.*1	Max.	Unit	Test Conditions*2
MMCIF	MMC_CLK clock cycle	$2 \times t_{PBcyc}$	—	ns	Figure 5.61
	MMC_CLK clock high level width	6.5	—	ns	
	MMC_CLK clock low level width	6.5	—	ns	
	MMC_CLK clock rising time	—	5	ns	
	MMC_CLK clock falling time	—	5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 output data delay (data transfer mode)	-6.5	6.5	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data setup	8	—	ns	
	MMC_CMD, MMC_D7 to MMC_D0 input data hold	2	—	ns	

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups.
For the MMC interface, the AC portion of the electrical characteristics is measured for each group.

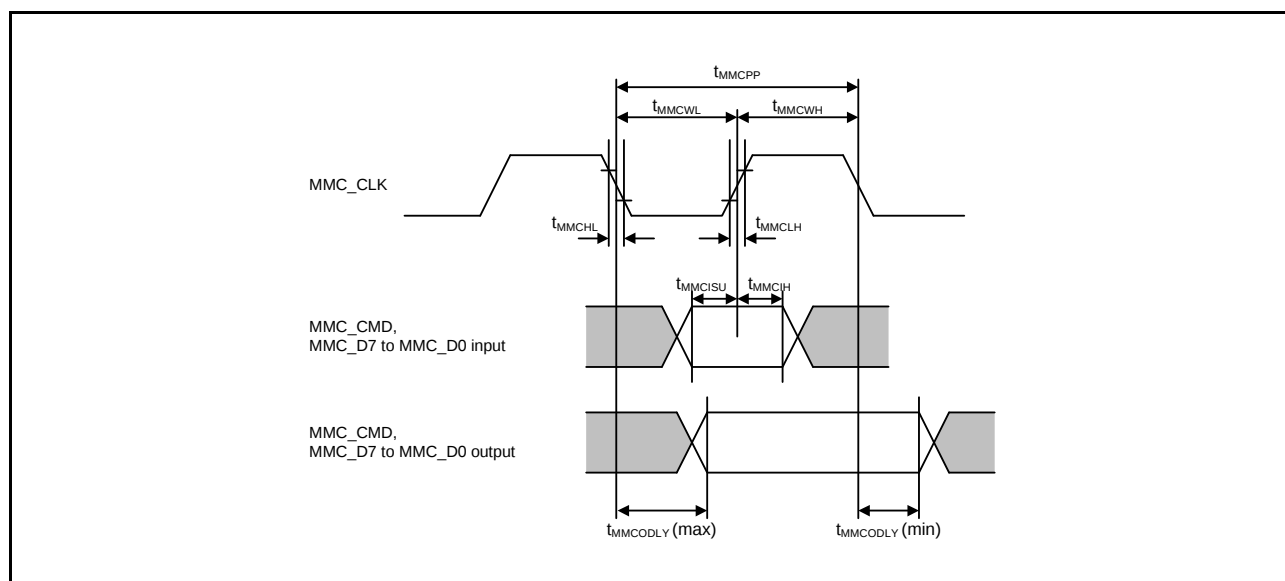
**Figure 5.61 MMC Interface**

Table 5.40 ETHERC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.62 to Figure 5.64
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_XXXX*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII_XXXX*2 setup time	T_{su}	3	—	ns	
	RMII_XXXX*2 hold time	T_{hd}	1	—	ns	
	RMII_XXXX*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.66
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TEND}	1	20	ns	Figure 5.67
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRs setup time	t_{CRSs}	10	—	ns	
	ET_CRs hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.68
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.69
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.70
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.71

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0

Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

5.5 A/D Conversion Characteristics

Table 5.45 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKB = PCLKC = 1$ MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.06 (0.40 + 0.25) *2	—	—	μs	- Sampling of channel-dedicated sample-and-hold circuits in 24 states - Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	μs	
	Dynamic range	0.25	—	VREFH 0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	0.48 (0.267) *2	—	—	μs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.0	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

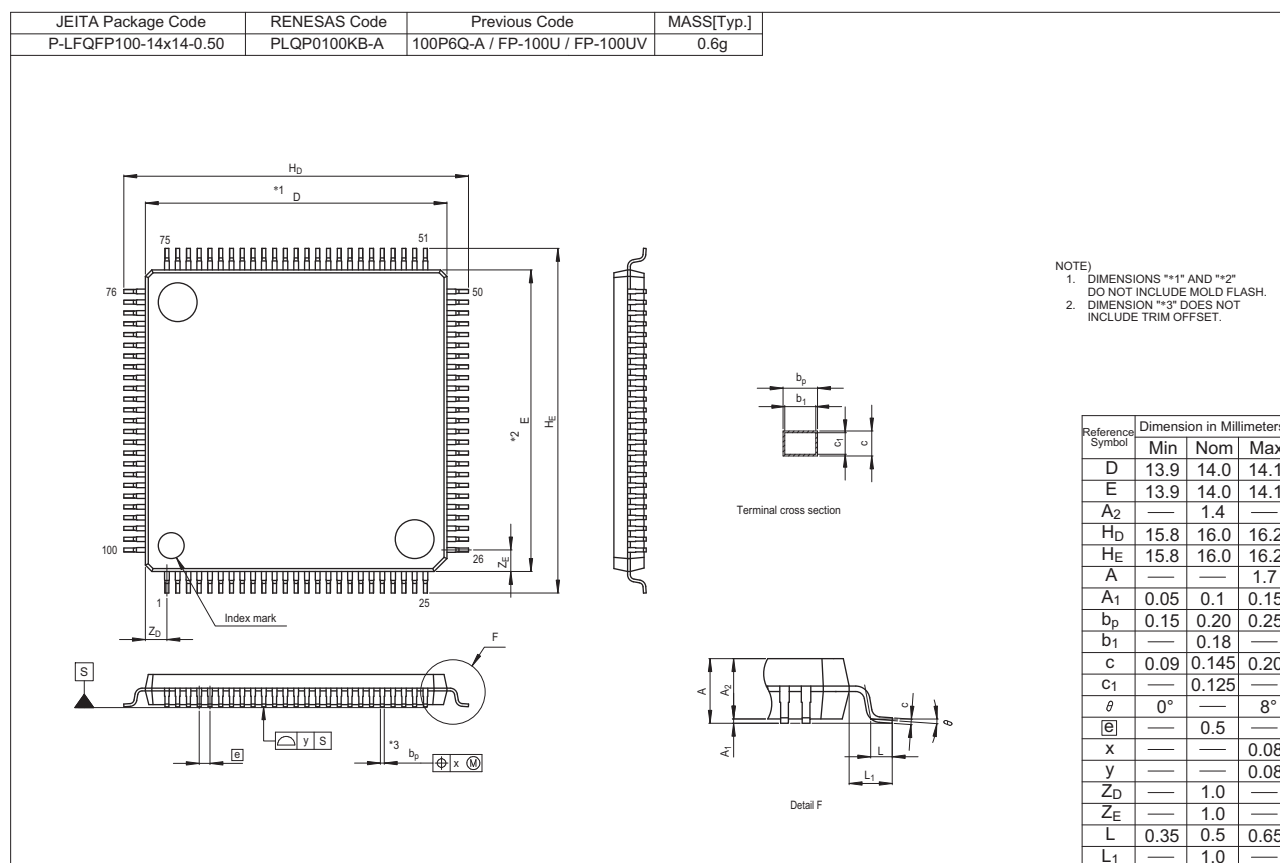


Figure G 100-Pin LFQFP (PLQP0100KB-A)