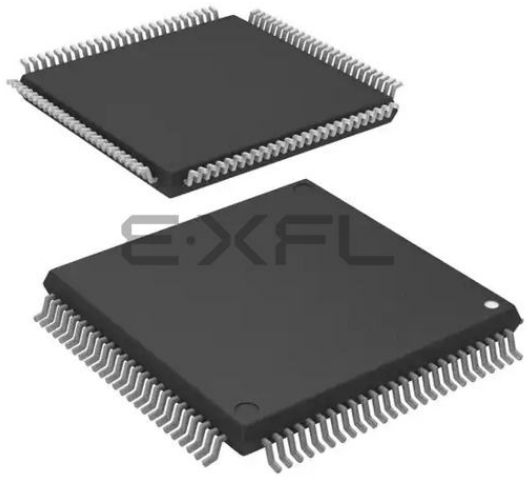
# Renesas Electronics America Inc - R5F564MGCDFP#31 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 2.5MB (2.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 552K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LFQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgcdfp-31 |

**Table 1.1 Outline of Specifications (2/9)**

| Classification | Module/Function | Description |
|---|---|---|
| Clock | Clock generation circuit | • Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator<br>• The peripheral module clocks can be set to frequencies above that of the system clock.<br>• Main-clock oscillation stoppage detection<br>• Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz<br>Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz.<br>Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz<br>ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz<br>ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz<br>Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz<br>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz<br>• Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit |
| Reset | | Nine types of reset<br>• RES# pin reset: Generated when the RES# pin is driven low.<br>• Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises.<br>• Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby.<br>• Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs.<br>• Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs.<br>• Software reset: Generated by register setting. |
| Power-on reset | | If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled. |
| Voltage detection circuit (LVDA) | | Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt.<br>• Voltage detection circuit 0<br>Capable of generating an internal reset<br>The option-setting memory can be used to select enabling or disabling of the reset.<br>Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V)<br>• Voltage detection circuits 1 and 2<br>Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V)<br>Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency)<br>Capable of generating an internal reset<br>• Two types of timing are selectable for release from reset<br>An internal interrupt can be requested.<br>• Detection of voltage rising above and falling below thresholds is selectable.<br>• Maskable or non-maskable interrupt is selectable<br>Voltage detection monitoring<br>Event linking |
| Low power consumption | Low power consumption facilities | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| | Battery backup function | • When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating. |

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1/3)**

| Group | Part No. | Package | Code Flash Memory Capacity | RAM Capacity | Data Flash Memory Capacity | Operating Frequency (Max.) | Encryption Module | SDHI |
|---|---|---|---|---|---|---|---|---|
| RX64M | R5F564MLCDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MFCDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MFDDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MFGDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MFHDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MLCDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MFCDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MFDDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MFGDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MFHDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MLCDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |

**Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/7)**

| Pin Number 177-Pin TFLGA 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| C4 | | P43 | | | | | IRQ11-DS | AN003 |
| C5 | | P45 | | | | | IRQ13-DS | AN005 |
| C6 | | P90 | A16/D16 | | ET1_RX_DV/ TXD7/SMOSI7/SSDA7 | | | AN114 |
| C7 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| C8 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2_B | IRQ2 | AN110 |
| C9 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| C10 | | PG0 | D24 | | ET1_RX_CLK/ REF50CK1 | | | |
| C11 | VCC | | | | | | | |
| C12 | | P62 | CS2#/RAS# | | | | | |
| C13 | | PE4 | D12[A12/D12] | MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28 | ET0_ERXD2 | | | AN102 |
| C14 | VSS | | | | | | | |
| C15 | | P70 | SDCLK | | | | | |
| D1 | | P01 | | TMCI0 | RXD6/SMISO6/ SSCL6 | | IRQ9 | AN119 |
| D2 | | P02 | | TMCI1 | SCK6 | | IRQ10 | AN120 |
| D3 | | P03 | | | | | IRQ11 | DA0 |
| D4 | | P00 | | TMRI0 | TXD6/SMOSI6/ SSDA6 | | IRQ8 | AN118 |
| D5 | | P44 | | | | | IRQ12-DS | AN004 |
| D6 | | P93 | A19/D19 | POE0# | ET1_LINKSTA/CTS7#/ RTS7#/SS7# | | | AN117 |
| D7 | | P95 | A21/D21 | | ET1_ERXD1/ RMII1_RXD1 | | | |
| D8 | VSS | | | | | | | |
| D9 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| D10 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B | IRQ7 | AN107 |
| D11 | | P61 | CS1#/SDCS# | | | | | |
| D12 | | PE5 | D13[A13/D13] | MTIOC4C/MTIOC2B/ GTIOC0A-A | ET0_RX_CLK/ REF50CK0 | | IRQ5 | AN103 |
| D13 | VCC | | | | | | | |
| D14 | | PE7 | D15[A15/D15] | MTIOC6A/ GTIOC3A-E/TOC1 | | MMC_RES#-B/ SDHI_WP-B | IRQ7 | AN105 |
| D15 | | P65 | CS5#/CKE | | | | | |
| E1 | | PJ5 | | POE8# | CTS2#/RTS2#/SS2# | | | |
| E2 | EMLE | | | | | | | |
| E3 | | PF5 | | | | | IRQ4 | |
| E4 | VSS | | | | | | | |
| E5*1 | | | | | | | | |
| E12 | | PE6 | D14[A14/D14] | MTIOC6C/ GTIOC3B-E/TIC1 | | MMC_CD-B/ SDHI_CD-B | IRQ6 | AN104 |
| E13 | TRDATA0 | PG2 | D26 | | ET1_TX_CLK | | | |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/7)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 85 | | P76 | CS6# | PO22 | RXD11/ET0_RX_CLK/ REF50CK0 | MMC_CMD-A/ SDHI_CMD-A/ QSSL-A | | |
| 86 | | PC2 | A18 | MTIOC4B/ GTIOC2B-D/TCLKA/ PO21 | RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV | MMC_CD-A/ SDHI_D3-A | | |
| 87 | | P75 | CS5# | PO20 | SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0 | MMC_RES#-A/ SDHI_D2-A | | |
| 88 | | P74 | A20/CS4# | PO19 | CTS11#/ET0_ERXD1/ RMII0_RXD1 | | | |
| 89 | | PC1 | A17 | MTIOC3A/TCLKD/ PO18 | SCK5/SSLA2-A/ ET0_ERXD2 | | IRQ12 | |
| 90 | VCC | | | | | | | |
| 91 | | PC0 | A16 | MTIOC3C/TCLKC/ PO17 | CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3 | | IRQ14 | |
| 92 | VSS | | | | | | | |
| 93 | | P73 | CS3# | PO16 | ET0_WOL | | | |
| 94 | | PB7 | A15 | MTIOC3B/TIOCB5/ PO31 | TXD9/ET0_CRS/ RMII0_CRS_DV | | | |
| 95 | | PB6 | A14 | MTIOC3D/TIOCA5/ PO30 | RXD9/ET0_ETXD1/ RMII0_TXD1 | | | |
| 96 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4# | SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0 | | | |
| 97 | | PB4 | A12 | TIOCA4/PO28 | CTS9#/ET0_TX_EN/ RMII0_TXD_EN | | | |
| 98 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11# | SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER | | | |
| 99 | | PB2 | A10 | TIOCC3/TCLKC/ PO26 | CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0 | | | |
| 100 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25 | TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0 | | IRQ4-DS | |
| 101 | | P72 | A19/CS2# | | ET0_MDC | | | |
| 102 | | P71 | A18/CS1# | | ET0_MDIO | | | |
| 103 | VCC | | | | | | | |
| 104 | | PB0 | A8 | MTIC5W/TIOCA3/ PO24 | RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1 | | IRQ12 | |
| 105 | VSS | | | | | | | |
| 106 | | PA7 | A7 | TIOCB2/PO23 | MISOA-B/ ET0_WOL | | | |
| 107 | | PA6 | A6 | MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10# | CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT | | | |
| 108 | | PA5 | A5 | MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21 | RSPCKA-B/ ET0_LINKSTA | | | |
| 109 | | PA4 | A4 | MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20 | TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC | | IRQ5-DS | |
| 110 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/ SSCL5/ ET0_MDIO | | IRQ6-DS | |

**Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (5/5)**

| Pin Number 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| M4 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | | IRQ2 | |
| M5 | VCC_USB | | | | | | | |
| M6 | VSS_USB | | | | | | | |
| M7 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2 | | | |
| M8 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30 | RXD8/MOSIA-A/ ET0_ETXD3 | MMC_D6-A | IRQ13 | |
| M9 | TRDATA1 | P81 | EDACK0 | MTIOC3D/ GTIOC0B-D/PO27 | RXD10/ET0_ETXD0/ RMII0_TXD0 | MMC_D3-A/ SDHI_CD-A/ QIO3-A | | |
| M10 | | P77 | CS7# | PO23 | TXD11/ET0_RX_ER/ RMII0_RX_ER | MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A | | |
| M11 | | PC0 | A16 | MTIOC3C/TCLKC/ PO17 | CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3 | | IRQ14 | |
| M12 | | PC1 | A17 | MTIOC3A/TCLKD/ PO18 | SCK5/SSLA2-A/ ET0_ERXD2 | | IRQ12 | |
| M13 | VCC | | | | | | | |
| N1 | | P21 | | MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0 | PIXD5 | IRQ9 | |
| N2 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0 | PIXD4 | IRQ8 | |
| N3 | | P87 | | MTIOC4C/ GTIOC1B-B/TIOCA2 | TXD10 | PIXD2 | | |
| N4 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15 | CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA | | IRQ4 | |
| N5 | | | | | USB0_DM | | | |
| N6 | | | | | USB0_DP | | | |
| N7 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET0_EXOUT | | IRQ10 | |
| N8 | VSS | | | | | | | |
| N9 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | MMC_D7-A | IRQ14 | |
| N10 | TRSYNC | P82 | EDREQ1 | MTIOC4A/ GTIOC2A-D/PO28 | TXD10/ET0_ETXD1/ RMII0_TXD1 | MMC_D4-A | | |
| N11 | | PC3 | A19 | MTIOC4D/ GTIOC1B-D/TCLKB/ PO24 | TXD5/SMOSI5/ SSDA5/ET0_TX_ER | MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A | | |
| N12 | | P75 | CS5# | PO20 | SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0 | MMC_RES#-A/ SDHI_D2-A | | |
| N13 | | P74 | A20/CS4# | PO19 | CTS11#/ET0_ERXD1/ RMII0_RXD1 | | | |

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

**Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (2/5)**

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 36 | | P21 | | MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1 | RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0 | PIXD5 | IRQ9 | |
| 37 | | P20 | | MTIOC1A/TIOCB3/ TMRI0/PO0 | TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0 | PIXD4 | IRQ8 | |
| 38 | | P17 | | MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8# | SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0 | PIXD3 | IRQ7 | ADTRG1# |
| 39 | | P87 | | MTIOC4C/ GTIOC1B-B/TIOCA2 | TXD10 | PIXD2 | | |
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT | TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | | IRQ6 | ADTRG0# |
| 41 | | P86 | | MTIOC4D/ GTIOC2B-B/TIOCA0 | RXD10 | PIXD1 | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13 | RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1 | PIXD0 | IRQ5 | |
| 43 | | P14 | | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15 | CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA | | IRQ4 | |
| 44 | | P13 | | MTIOC0B/TIOCA5/ TMO3/PO13 | TXD2/SMOSI2/ SSDA2/SDA0[FM+] | | IRQ3 | ADTRG1# |
| 45 | | P12 | | TMCI1 | RXD2/SMISO2/ SSCL2/SCL0[FM+] | | IRQ2 | |
| 46 | VCC_USB | | | | | | | |
| 47 | | | | | USB0_DM | | | |
| 48 | | | | | USB0_DP | | | |
| 49 | VSS_USB | | | | | | | |
| 50 | | P56 | EDACK1 | MTIOC3C/TIOCA1 | | | | |
| 51 | TRDATA3 | P55 | WAIT#/ EDREQ0 | MTIOC4D/TMO3 | CRX1/ET0_EXOUT | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE/EDACK0 | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA | | | |
| 53 | | P53*1 | BCLK | | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/SSCL2 | | | |
| 55 | | P51 | WR1#/BC1#/ WAIT# | | SCK2 | | | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2 | | | |
| 57 | VSS | | | | | | | |
| 58 | TRCLK | P83 | EDACK1 | MTIOC4C/ GTIOC0A-D | CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10 | | | |
| 59 | VCC | | | | | | | |
| 60 | UB | PC7 | A23/CS0# | MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF | TXD8/MISOA-A/ ET0_COL | MMC_D7-A | IRQ14 | |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30 | RXD8/MOSIA-A/ ET0_ETXD3 | MMC_D6-A | IRQ13 | |
| 62 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29 | SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2 | MMC_D5-A | | |

**Table 4.1 List of I/O Registers (Address Order) (6 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 285Dh | EXDMAC1 | EXDMA Software Start Register | EDMREQ | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 285Eh | EXDMAC1 | EXDMA Status Register | EDMSTS | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2860h | EXDMAC1 | EXDMA External Request Sense Mode Register | EDMRMD | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2861h | EXDMAC1 | EXDMA External Request Flag Register | EDMERF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2862h | EXDMAC1 | EXDMA Peripheral Request Flag Register | EDMPRF | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2A00h | EXDMAC | EXDMAC Module Start Register | EDMAST | 8 | 8 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE0h | EXDMAC | Cluster Buffer Register 0 | CLSBR0 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE4h | EXDMAC | Cluster Buffer Register 1 | CLSBR1 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BE8h | EXDMAC | Cluster Buffer Register 2 | CLSBR2 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BECh | EXDMAC | Cluster Buffer Register 3 | CLSBR3 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF0h | EXDMAC | Cluster Buffer Register 4 | CLSBR4 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF4h | EXDMAC | Cluster Buffer Register 5 | CLSBR5 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BF8h | EXDMAC | Cluster Buffer Register 6 | CLSBR6 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 2BFCh | EXDMAC | Cluster Buffer Register 7 | CLSBR7 | 32 | 32 | 1, 2 BCLK | | EXDMACa |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3024h | BSC | CS2 Wait Control Register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3028h | BSC | CS2 Wait Control Register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3032h | BSC | CS3 Mode Register | CS3MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3034h | BSC | CS3 Wait Control Register 1 | CS3WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3038h | BSC | CS3 Wait Control Register 2 | CS3WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3042h | BSC | CS4 Mode Register | CS4MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3044h | BSC | CS4 Wait Control Register 1 | CS4WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3048h | BSC | CS4 Wait Control Register 2 | CS4WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3052h | BSC | CS5 Mode Register | CS5MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3054h | BSC | CS5 Wait Control Register 1 | CS5WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3058h | BSC | CS5 Wait Control Register 2 | CS5WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3062h | BSC | CS6 Mode Register | CS6MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3064h | BSC | CS6 Wait Control Register 1 | CS6WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3068h | BSC | CS6 Wait Control Register 2 | CS6WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3072h | BSC | CS7 Mode Register | CS7MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3074h | BSC | CS7 Wait Control Register 1 | CS7WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3078h | BSC | CS7 Wait Control Register 2 | CS7WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3802h | BSC | CS0 Control Register | CS0CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 380Ah | BSC | CS0 Recovery Cycle Register | CS0REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3812h | BSC | CS1 Control Register | CS1CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 381Ah | BSC | CS1 Recovery Cycle Register | CS1REC | 16 | 16 | 1, 2 BCLK | | Buses |

**Table 4.1 List of I/O Registers (Address Order) (21 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9198h | S12AD1 | A/D Compare Level Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 919Ah | S12AD1 | A/D Compare Level Register 1 | ADCMPLR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 919Ch | S12AD1 | A/D Compare Data Register 0 | ADCMPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 919Eh | S12AD1 | A/D Compare Data Register 1 | ADCMPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 91A0h | S12AD1 | A/D Compare Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 91A2h | S12AD1 | A/D Compare Status Register 1 | ADCMPSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 91A4h | S12AD1 | A/D Compare Status Extended Register | ADCMPSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADC |
| 0008 9E00h | QSPI | QSPI Control Register | SPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E01h | QSPI | QSPI Slave Select Polarity Register | SSLP | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E02h | QSPI | QSPI Pin Control Register | SPPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E03h | QSPI | QSPI Status Register | SPSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E04h | QSPI | QSPI Data Register | SPDR | 32 | 8, 16, 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E08h | QSPI | QSPI Sequence Control Register | SPSCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E09h | QSPI | QSPI Sequence Status Register | SPSSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ah | QSPI | QSPI Bit Rate Register | SPBR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Bh | QSPI | QSPI Data Control Register | SPDCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Ch | QSPI | QSPI Clock Delay Register | SPCKD | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Dh | QSPI | QSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E0Eh | QSPI | QSPI Next-Access Delay Register | SPND | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E10h | QSPI | QSPI Command Register 0 | SPCMD0 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E12h | QSPI | QSPI Command Register 1 | SPCMD1 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E14h | QSPI | QSPI Command Register 2 | SPCMD2 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E16h | QSPI | QSPI Command Register 3 | SPCMD3 | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E18h | QSPI | QSPI Buffer Control Register | SPBFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ah | QSPI | QSPI Buffer Data Count Set Register | SPBDCR | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E1Ch | QSPI | QSPI Transfer Data Length Multiplier Setting Register 0 | SPBMUL0 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E20h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 1 | SPBMUL1 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E24h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 2 | SPBMUL2 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 9E28h | QSPI | QSPI Transfer Data Length Multiplier Setting Register 3 | SPBMUL3 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | QSPI |
| 0008 A000h | SCI0 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A001h | SCI0 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A002h | SCI0 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A003h | SCI0 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A006h | SMCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIg, SCIh |

**Table 4.1 List of I/O Registers (Address Order) (32 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C068h | PORT8 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C069h | PORT9 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ch | PORTC | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Dh | PORTD | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Fh | PORTF | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C070h | PORTG | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C072h | PORTJ | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C080h | PORT0 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C081h | PORT0 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C082h | PORT1 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C083h | PORT1 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C084h | PORT2 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C085h | PORT2 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C086h | PORT3 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C087h | PORT3 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C088h | PORT4 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C089h | PORT4 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ah | PORT5 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Bh | PORT5 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ch | PORT6 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Dh | PORT6 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Eh | PORT7 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Fh | PORT7 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C090h | PORT8 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C091h | PORT8 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C092h | PORT9 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C093h | PORT9 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C094h | PORTA | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

**Table 4.1 List of I/O Registers (Address Order) (42 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 42A0h | CMTW1 | Output Compare Register 0 | CMWOCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 42A4h | CMTW1 | Output Compare Register 1 | CMWOCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | CMTW |
| 0009 8000h to 0009 D6BFh | SRC | Filter Coefficient Table | SRCFCTR0 to 5551 | 32 | 32 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF0h | SRC | Input Data Register | SRCID | 32 | 32 | 5, 6 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF4h | SRC | Output Data Register | SRCOD | 32 | 32 | 5, 6 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFF8h | SRC | Input Data Control Register | SRCIDCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFAh | SRC | Output Data Control Register | SRCODCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFCh | SRC | Control Register | SRCCTRL | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 0009 DFFEh | SRC | Status Register | SRCSTAT | 16 | 16 | 4, 5 PCLKB | 2, 3 ICLK | SRC |
| 000A 0000h | USB0 | System Configuration Control Register | SYSCFG | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0004h | USB0 | System Configuration Status Register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0008h | USB0 | Device State Control Register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0014h | USB0 | CFIFO Port Register | CFIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0018h | USB0 | D0FIFO Port Register | D0FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 001Ch | USB0 | D1FIFO Port Register | D1FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0020h | USB0 | CFIFO Port Select Register | CFIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0022h | USB0 | CFIFO Port Control Register | CFIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0028h | USB0 | D0FIFO Port Select Register | D0FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ah | USB0 | D0FIFO Port Control Register | D0FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ch | USB0 | D1FIFO Port Select Register | D1FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Eh | USB0 | D1FIFO Port Control Register | D1FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0030h | USB0 | Interrupt Enable Register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0032h | USB0 | Interrupt Enable Register 1 | INTENB1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0036h | USB0 | BRDY Interrupt Enable Register | BRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0038h | USB0 | NRDY Interrupt Enable Register | NRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 003Ah | USB0 | BEMP Interrupt Enable Register | BEMPENB | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 003Ch | USB0 | SOF Output Configuration Register | SOFCFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0040h | USB0 | Interrupt Status Register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0042h | USB0 | Interrupt Status Register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0046h | USB0 | BRDY Interrupt Status Register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0048h | USB0 | NRDY Interrupt Status Register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 004Ah | USB0 | BEMP Interrupt Status Register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 004Ch | USB0 | Frame Number Register | FRMNUM | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 004Eh | USB0 | Device State Change Register | DVCHGR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |

**Table 4.1 List of I/O Registers (Address Order) (44 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 009Ah | USB0 | Pipe3 Transaction Counter Register | PIPE3TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 009Ch | USB0 | Pipe4 Transaction Counter Enable Register | PIPE4TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 009Eh | USB0 | Pipe4 Transaction Counter Register | PIPE4TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00A0h | USB0 | Pipe5 Transaction Counter Enable Register | PIPE5TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00A2h | USB0 | Pipe5 Transaction Counter Register | PIPE5TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00D0h | USB0 | Device Address 0 Configuration Register | DEVADD0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00D2h | USB0 | Device Address 1 Configuration Register | DEVADD1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00D4h | USB0 | Device Address 2 Configuration Register | DEVADD2 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00D6h | USB0 | Device Address 3 Configuration Register | DEVADD3 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00D8h | USB0 | Device Address 4 Configuration Register | DEVADD4 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00DAh | USB0 | Device Address 5 Configuration Register | DEVADD5 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 00F0h | USB0 | PHY Cross Point Adjustment Register | PHYSLEW | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0400h | USB | Deep Standby USB Transceiver Control/Pin Monitoring Register | DPUSR0R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0404h | USB | Deep Standby USB Suspend/Resume Interrupt Register | DPUSR1R | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5 | USBb |
| 000A 0500h | PDC | PDC Control Register 0 | PCCR0 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0504h | PDC | PDC Control Register 1 | PCCR1 | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0508h | PDC | PDC Status Register | PCSR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 050Ch | PDC | PDC Pin Monitor Register | PCMONR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0510h | PDC | PDC Receive Data Register | PCDR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0514h | PDC | Vertical Capture Register | VCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000A 0518h | PDC | Horizontal Capture Register | HCR | 32 | 32 | 2, 3 PCLKB | 2 ICLK | PDC |
| 000C 0000h | EDMAC 0 | EDMAC Mode Register | EDMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0008h | EDMAC 0 | EDMAC Transmit Request Register | EDTRR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0010h | EDMAC 0 | EDMAC Receive Request Register | EDRRR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0018h | EDMAC 0 | Transmit Descriptor List Start Address Register | TDLAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0020h | EDMAC 0 | Receive Descriptor List Start Address Register | RDLAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0028h | EDMAC 0 | ETHERC/EDMAC Status Register | EESR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0030h | EDMAC 0 | ETHERC/EDMAC Status Interrupt Enable Register | EESIPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0038h | EDMAC 0 | ETHERC/EDMAC Transmit/Receive Status Copy Enable Register | TRSCER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0040h | EDMAC 0 | Missed-Frame Counter Register | RMFCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |
| 000C 0048h | EDMAC 0 | Transmit FIFO Threshold Register | TFTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMAC a |

**Table 4.1 List of I/O Registers (Address Order) (50 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1406h | MTU2 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1408h | MTU2 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 140Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 140Ch | MTU2 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1600h | MTU8 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1601h | MTU8 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1602h | MTU8 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1603h | MTU8 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1604h | MTU8 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1606h | MTU8 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1608h | MTU8 | Timer Counter | TCNT | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 160Ch | MTU8 | Timer General Register A | TGRA | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1610h | MTU8 | Timer General Register B | TGRB | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1614h | MTU8 | Timer General Register C | TGRC | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1618h | MTU8 | Timer General Register D | TGRD | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A00h | MTU6 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A01h | MTU7 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A02h | MTU6 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A03h | MTU7 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A04h | MTU6 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A05h | MTU6 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A06h | MTU7 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A07h | MTU7 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A08h | MTU6 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A09h | MTU7 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A0Ah | MTU | Timer Output Master Enable Register B | TOERB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A0Eh | MTU | Timer Output Control Register 1B | TOCR1B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (51 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1A0Fh | MTU | Timer Output Control Register 2B | TOCR2B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A10h | MTU6 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A12h | MTU7 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A14h | MTU | Timer Cycle Data Register B | TCDRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A16h | MTU | Timer Dead Time Data Register B | TDDRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A18h | MTU6 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A1Ah | MTU6 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A1Ch | MTU7 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A1Eh | MTU7 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A20h | MTU | Timer Subcounter B | TCNTSB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A22h | MTU | Timer Cycle Buffer Register B | TCBRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A24h | MTU6 | Timer General Register C | TGRC | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A26h | MTU6 | Timer General Register D | TGRD | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A28h | MTU7 | Timer General Register C | TGRC | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A2Ah | MTU7 | Timer General Register D | TGRD | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A2Ch | MTU6 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A2Dh | MTU7 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A30h | MTU | Timer Interrupt Skipping Set Register 1B | TITCR1B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A31h | MTU | Timer Interrupt Skipping Counter 1B | TITCNT1B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A32h | MTU | Timer Buffer Transfer Set Register B | TBTERB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A34h | MTU | Timer Dead Time Enable Register B | TDERB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A36h | MTU | Timer Output Level Buffer Register B | TOLBRB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counter 2B | TITCNT2B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (66 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 049Ch | USBA | Pipe4 Transaction Counter Enable Register | PIPE4TRE | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 049Eh | USBA | Pipe4 Transaction Counter Register | PIPE4TRN | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04A0h | USBA | Pipe5 Transaction Counter Enable Register | PIPE5TRE | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04A2h | USBA | Pipe5 Transaction Counter Register | PIPE5TRN | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04D0h | USBA | Device Address 0 Configuration Register | DEVADD0 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04D2h | USBA | Device Address 1 Configuration Register | DEVADD1 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04D4h | USBA | Device Address 2 Configuration Register | DEVADD2 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04D6h | USBA | Device Address 3 Configuration Register | DEVADD3 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04D8h | USBA | Device Address 4 Configuration Register | DEVADD4 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 04DAh | USBA | Device Address 5 Configuration Register | DEVADD5 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 0500h | USBA | Low Power Control Register | LPCTRL | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 0502h | USBA | Low Power Status Register | LPSTS | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 0540h | USBA | Battery Charging Control Register | BCCTRL | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 0544h | USBA | Function L1 Control Register 1 | PL1CTRL1 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |
| 000D 0546h | USBA | Function L1 Control Register 2 | PL1CTRL2 | 16 | 16 | (3 + BUSWAIT) PCLKA or more | Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5 | USBA |

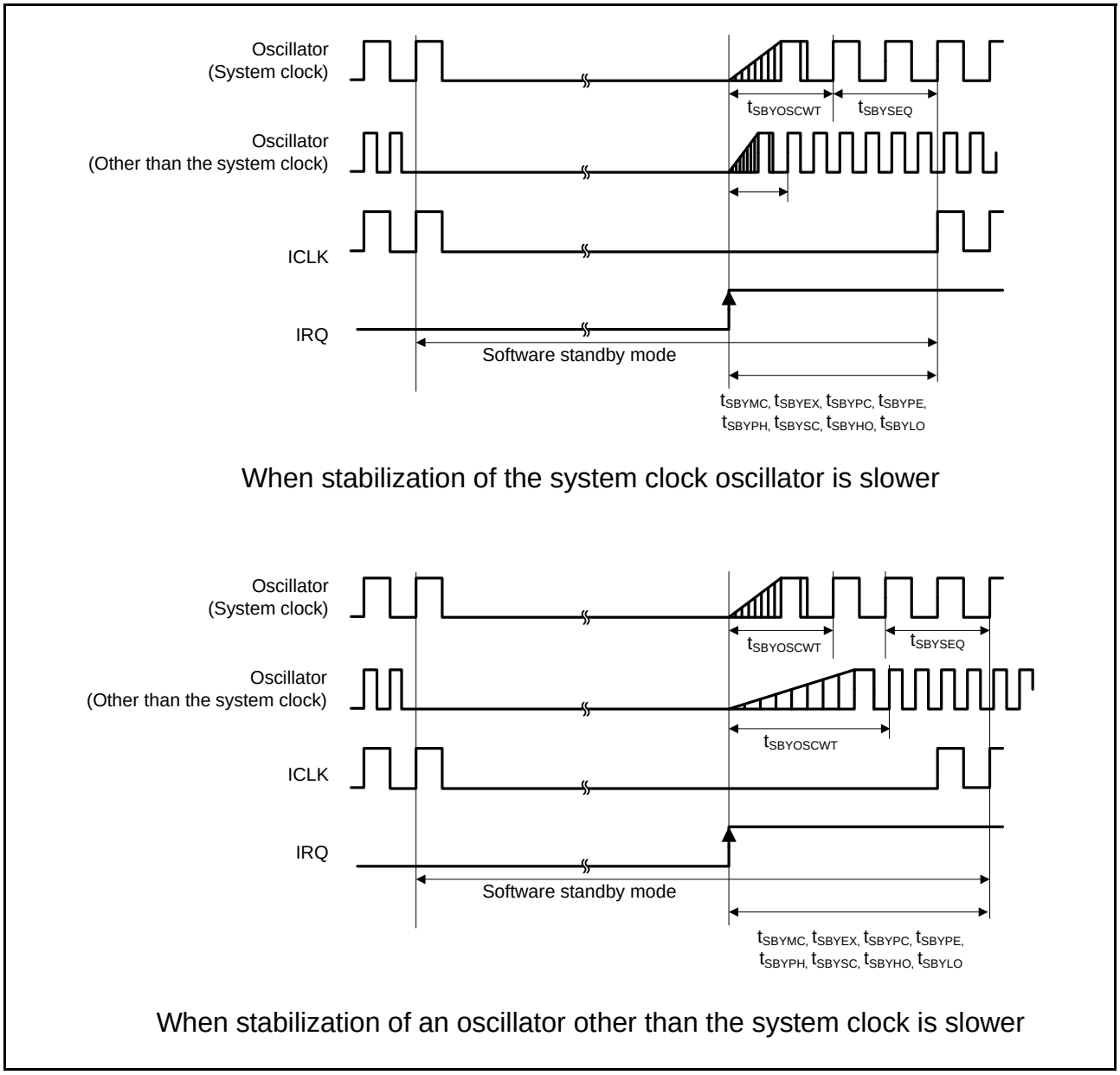


**Figure 5.12 Software Standby Mode Cancellation Timing**

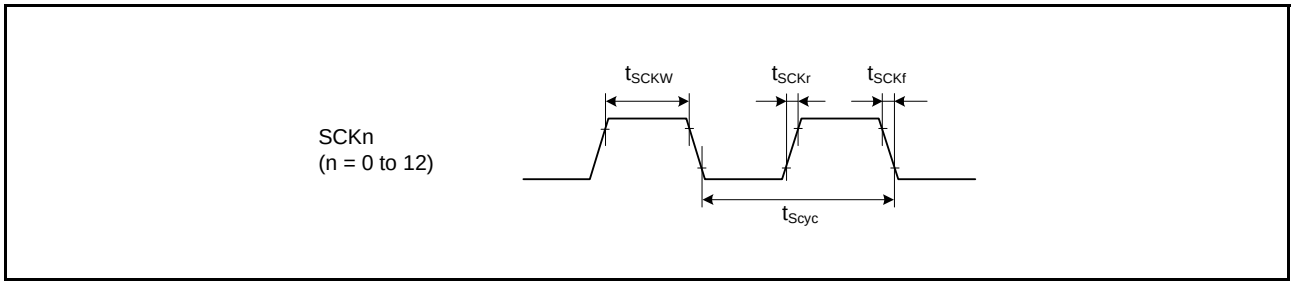


**Figure 5.44 SCK Clock Input Timing**

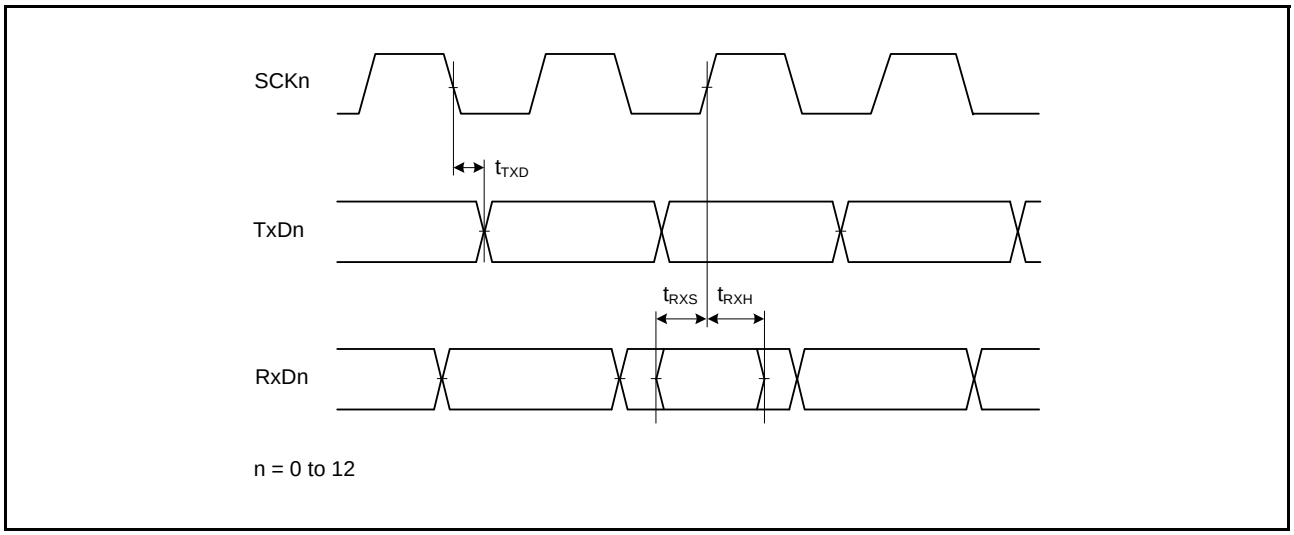


**Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode**

### Table 5.34 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|
| Simple SPI | SCK clock cycle output (master) | $t_{SPcyc}$ | 4 | 65536 | $t_{PBcyc}$ | Figure 5.46 |
| | SCK clock cycle input (slave) | | 8 | 65536 | | |
| | SCK clock high pulse width | $t_{SPCKWH}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock low pulse width | $t_{SPCKWL}$ | 0.4 | 0.6 | $t_{SPcyc}$ | |
| | SCK clock rise/fall time | $t_{SPCKr}$, $t_{SPCKf}$ | — | 20 | ns | |
| | Data input setup time | $t_{SU}$ | 33.3 | — | ns | Figure 5.47 to Figure 5.52 |
| | Data input hold time | $t_H$ | 33.3 | — | ns | |
| | SS input setup time | $t_{LEAD}$ | 1 | — | $t_{SPcyc}$ | |
| | SS input hold time | $t_{LAG}$ | 1 | — | $t_{SPcyc}$ | |
| | Data output delay time | $t_{OD}$ | — | 33.3 | ns | |
| | Data output hold time | $t_{OH}$ | –10 | — | ns | |
| | Data rise/fall time | $t_{Dr}$, $t_{Df}$ | — | 16.6 | ns | |
| | SS input rise/fall time | $t_{SSLr}$, $t_{SSLf}$ | — | 16.6 | ns | |
| | Slave access time | $t_{SA}$ | — | 5 | $t_{PBcyc}$ | Figure 5.51, Figure 5.52 |
| | Slave output release time | $t_{REL}$ | — | 5 | $t_{PBcyc}$ | |

Note 1. $t_{PBcyc}$: PCLKB cycle

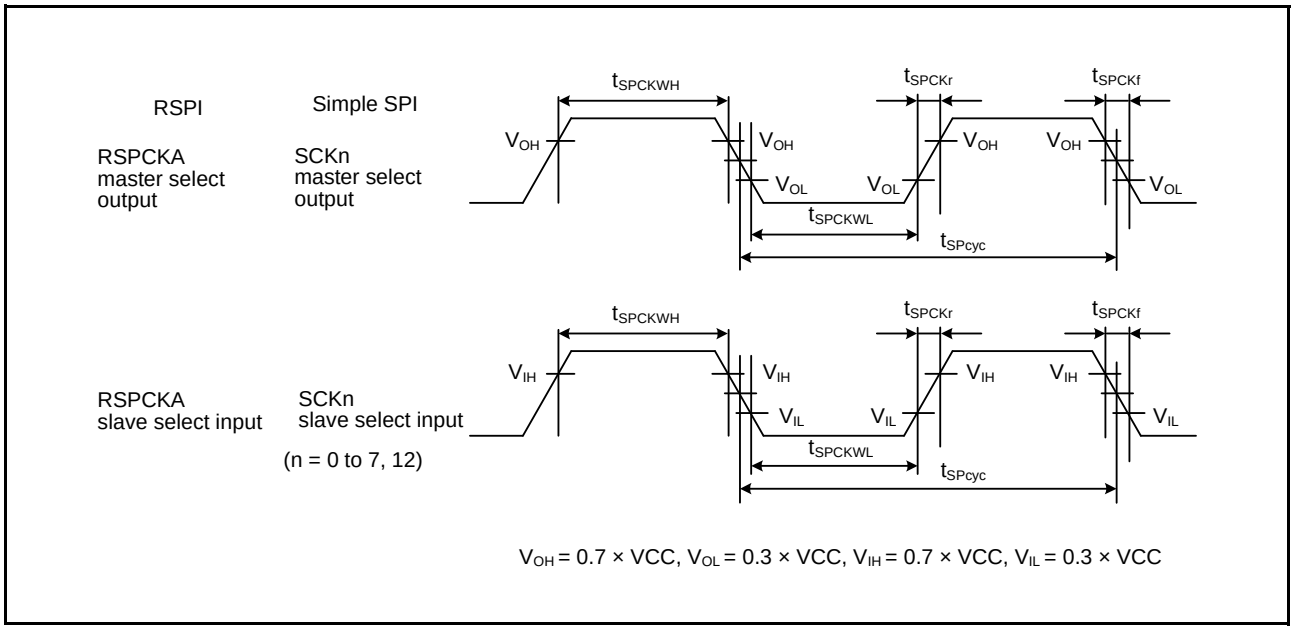


**Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing**

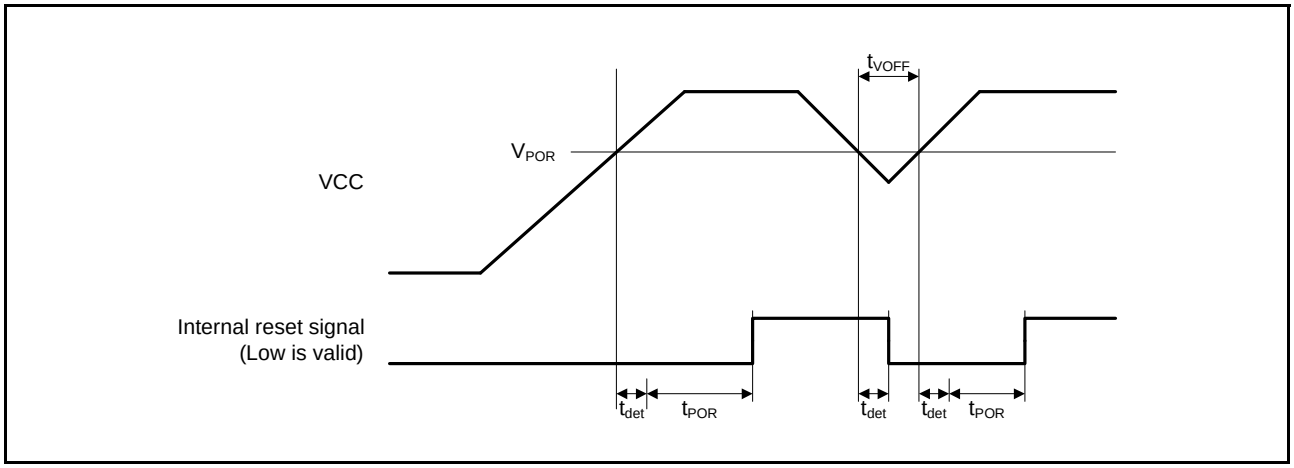


**Figure 5.79 Power-on Reset Timing**

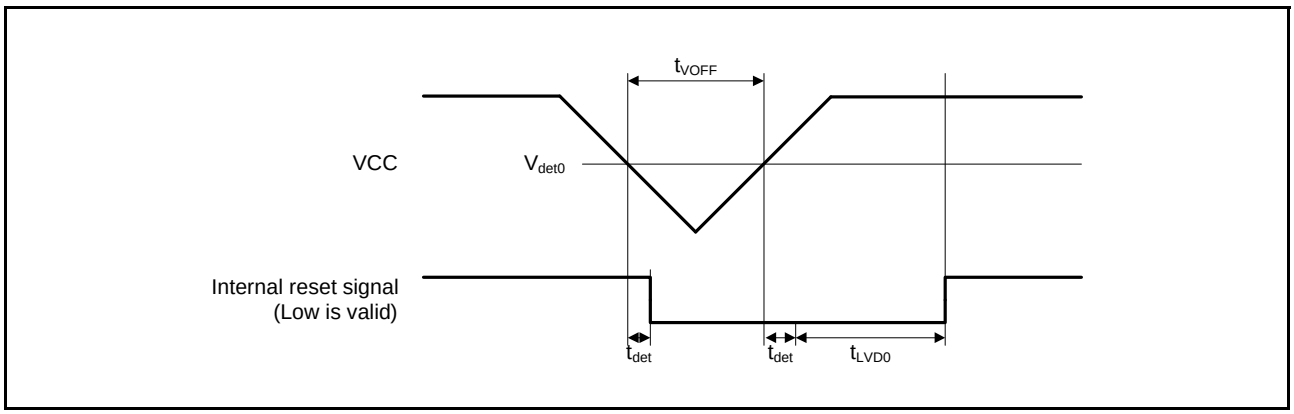


**Figure 5.80 Voltage Detection Circuit Timing ($V_{det0}$)**

## 5.11 Flash Memory Characteristics

### Table 5.53 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V
Temperature range for programming/erasure: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time $N_{PEC}$ ≤ 100 times | 256 bytes | $t_{P256}$ | — | 0.9 | 13.2 | — | 0.4 | 6 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 29 | 176 | — | 13 | 80 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 116 | 704 | — | 52 | 320 | ms |
| Programming time $N_{PEC}$ > 100 times | 256 bytes | $t_{P256}$ | — | 1.1 | 15.8 | — | 0.5 | 7.2 | ms |
| | 8 Kbytes | $t_{P8K}$ | — | 35 | 212 | — | 16 | 96 | ms |
| | 32 Kbytes | $t_{P32K}$ | — | 140 | 848 | — | 64 | 384 | ms |
| Erasure time $N_{PEC}$ ≤ 100 times | 8 Kbytes | $t_{E8K}$ | — | 71 | 216 | — | 39 | 120 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 254 | 864 | — | 141 | 480 | ms |
| Erasure time $N_{PEC}$ > 100 times | 8 Kbytes | $t_{E8K}$ | — | 85 | 260 | — | 47 | 144 | ms |
| | 32 Kbytes | $t_{E32K}$ | — | 304 | 1040 | — | 169 | 576 | ms |
| Reprogramming/erasure cycle*1 | | $N_{PEC}$ | 1000*2 | — | — | 1000*2 | — | — | Times |
| Suspend delay time during programming | | $t_{SPD}$ | — | — | 264 | — | — | 120 | µs |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 216 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | — | — | 1.7 | ms |
| Suspend delay time during erasure (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | — | — | 1.7 | ms |
| Forced stop command | | $t_{FD}$ | — | — | 32 | — | — | 20 | µs |
| Data hold time*3 | | $t_{DRP}$ | 10 | — | — | 10 | — | — | Year |
| FCU reset time | | $t_{FCUR}$ | 35 | — | — | 35 | — | — | µs |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).
Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

| REVISION HISTORY | RX64M Group Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.90 | Feb 28, 2014 | — | First edition, issued |
| 1.00 | Jul 31, 2014 | Summary | |
| | | 1 | ■ Data transfer, changed |
| | | 1. Overview | |
| | | — | FINEC (Pin), deleted |
| | | 2 | Table 1.1 Outline of Specifications (1/9), changed |
| | | 3 | Table 1.1 Outline of Specifications (2/9), changed |
| | | 6 | Table 1.1 Outline of Specifications (5/9), changed |
| | | 7 | Table 1.1 Outline of Specifications (6/9), changed |
| | | 8 | Table 1.1 Outline of Specifications (7/9), changed |
| | | 9 | Table 1.1 Outline of Specifications (8/9), changed |
| | | 10 | Table 1.1 Outline of Specifications (9/9), changed |
| | | 16 | Figure 1.1 How to Read the Product Part Number, changed |
| | | 19 | Table 1.4 Pin Functions (2/8), changed |
| | | 20 | Table 1.4 Pin Functions (3/8), changed |
| | | 25 | Table 1.4 Pin Functions (8/8), note added |
| | | 2. CPU, added | |
| | | 3. Address Space, added | |
| | | 4. I/O Registers, added | |
| | | 5. Electrical Characteristics, added | |
| | | Appendix 1. Package Dimensions, added | |

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.10 | Oct 24, 2016 | All | Terms unified:<br>GPTa → GPTA<br>LQFP → LFQFP | |
| | | Features | | |
| | | 1 | AES key lengths, changed | TN-RX*-A122A/E |
| | | 1. Overview | | |
| | | 2 | Table 1.1 Outline of Specifications (1/9), changed | TN-RX*-A127A/E |
| | | 5 | Table 1.1 Outline of Specifications (4/9), changed | |
| | | 10 | Table 1.1 Outline of Specifications (9/9), changed | TN-RX*-A122A/E |
| | | 28 | Figure 1.5 Pin Assignment (176-Pin LFQFP), changed | |
| | | 48 | Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5), changed | |
| | | 49 | Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5), changed | |
| | | 52 | Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/5), changed | |
| | | 55 | Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/5), changed | |
| | | 58 | Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4), changed | |
| | | 59 | Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4), changed | |
| | | 63 | Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/4), changed | |
| | | 4. I/O Registers | | |
| | | 71 | (4) Notes on Sleep Mode and Mode Transitions, added | |
| | | 73 | Table 4.1 List of I/O Registers (Address Order) (2 / 67)<br>0008 1200h, 0008 1201h, 0008 1204h, 0008 1208h, added | TN-RX*-A127A/E |