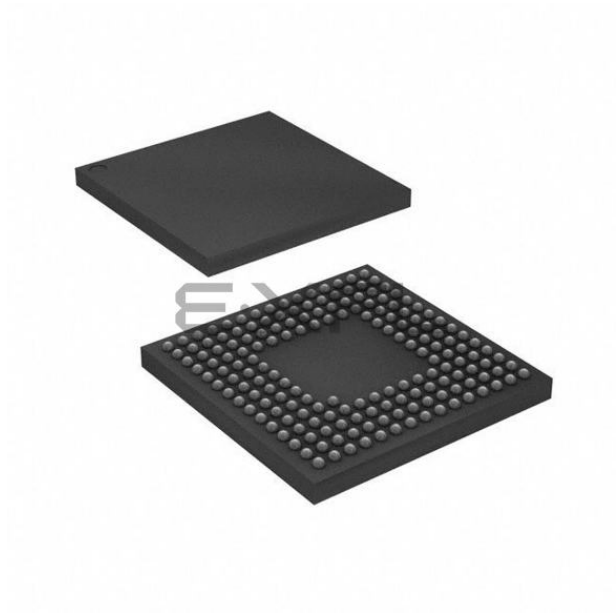
Renesas Electronics America Inc - R5F564MGCDLC#21 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgcdlc-21

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Communication function	I²C bus interface (RIICa)	• 2 channels (only channel 0 can be used in fast-mode plus) Communication formats I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPIa)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Quad serial peripheral interface (QSPI)	• 1 channel • Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) • Programmable bit length and selectable active sense and phase of the clock signal • Sequential execution of transfer • LSB or MSB first is selectable.
Serial sound interface (SSI)		• 2 channels • Full-duplex transfer is possible (only on channel 0). • Support for multiple audio formats • Support for master or slave operation • Bit clock frequency is selectable from four different types (16 fs, 32 fs, 48 fs, and 64 fs). • Support for 8-/16-/18-/20-/22-/24 bit data formats • Internal 8-stage FIFO for transmission and reception • Stopping SSIWS when data transfer is stopped is selectable.
Sampling rate converter (SRC)		• 1 channel • Data formats: 32-bit stereo (16 bits for the left, 16 bits for the right) and 16-bit monaural. • Input sampling rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz • Output sampling rates: 32, 44.1, 48, 8*2 or 16 kHz*2
SD host interface (SDHI)*4		• 1 channel • Transfer speed: Supports high-speed mode (15 MB/s) and default speed mode (10 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
MMC host interface (MMCIF)		• 1 channel • Transfer speed: Supports high-speed mode (30 MB/s) and Backward-compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)

Table 1.2 Comparison of Functions for Different Packages (1/2)

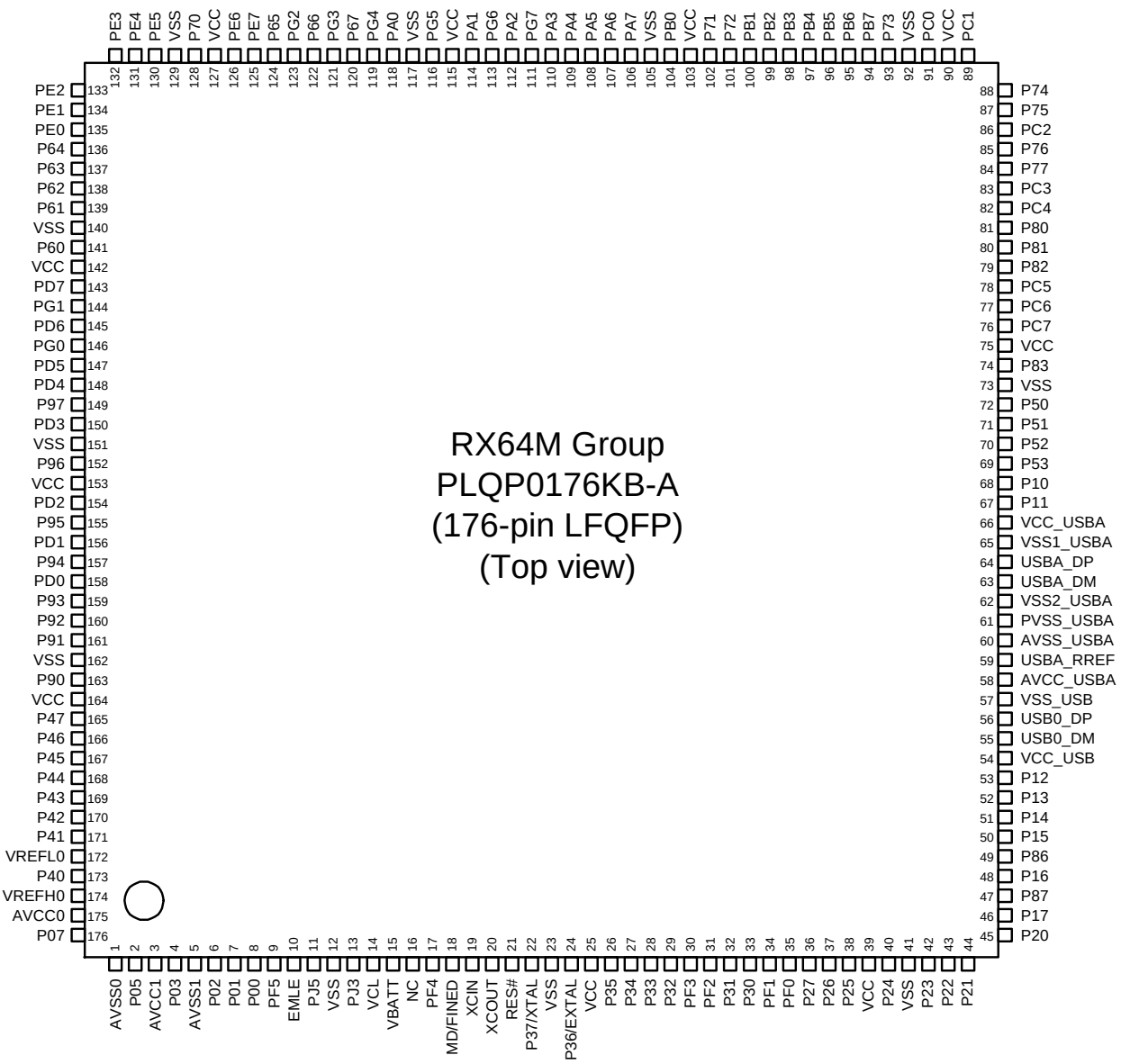
Functions		RX64M Group		
Package		**177 Pins, 176 Pins**	**145 Pins, 144 Pins**	**100 Pins**
External bus	External bus width	32 bits	16 bits	
	SDRAM area controller	Available		Not supported
DMA	DMA controller	Ch. 0 to 7		
	Data transfer controller	Available		
	EXDMA controller	Ch. 0 and 1		
Timers	16-bit timer pulse unit	Ch. 0 to 5		
	Multi-function timer pulse unit 3	Ch. 0 to 8		
	General-purpose PWM timer	Ch. 0 to 3		
	Port output enable 3	Available		
	Programmable pulse generator	Ch. 0 and 1		
	8-bit timers	Ch. 0 to 3		
	Compare match timer	Ch. 0 to 3		
	Compare match timer W	Ch. 0 and 1		
	Realtime clock	Available		
	Watchdog timer	Available		
	Independent watchdog timer	Available		
Communication function	Ethernet controller	Ch. 0 and 1	Ch. 0	
	PTP controller for ethernet controller	Available		
	DMAC controller for ethernet	Ch. 0 and 1 (ETHERC) Ch. 2 (EPTPC)	Ch. 0 (ETHERC) and 2 (EPTPC)	
	USB 2.0 FS host/function module	Ch. 0		
	USB 2.0 FS host/function module with battery charging	Available	Not supported	
	Serial communications interfaces (SCIg)	Ch. 0 to 7		Ch. 0 to 3, 5 and 6
	Serial communications interfaces (SCIh)	Ch. 12		
	Serial communications interfaces with FIFO	Ch. 8 to 11		Ch. 8 and 9
	I^2C bus interfaces	Ch. 0 and 2		
	Serial peripheral interface	Ch. 0		
	CAN module	Ch. 0 to 2		Ch. 0 and 1
	Quad serial peripheral interface	Ch. 0		
	Serial sound interfaces	Ch. 0 and 1		
	Sampling rate converter	Available		
	SD host interface	Ch. 0		
	MMC host interface	Ch. 0		
	Parallel data capture unit	Available		Not supported
12-bit A/D converter		AN000 to 007 (unit 0: 8 channels) AN100 to 120 (unit 1: 21 channels)		AN000 to 007 (unit 0: 8 channels) AN100 to 113 (unit 1: 14 channels)
12-bit D/A converter		Ch. 0 and 1		Ch. 1
Temperature sensor		Available		
CRC calculator		Available		
Data operation circuit		Available		
Clock frequency accuracy measurement circuit		Available		
AES		Available		

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode or user boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LFQFP).

Figure 1.5 Pin Assignment (176-Pin LFQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (6/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
143		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
144		PG1	D25		ET1_RX_ER/ RMII1_RX_ER			
145		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
146		PG0	D24		ET1_RX_CLK/ REF50CK1			
147		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
148		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
149		P97	A23/D23		ET1_ERXD3			
150		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
151	VSS							
152		P96	A22/D22		ET1_ERXD2			
153	VCC							
154		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2_B	IRQ2	AN110
155		P95	A21/D21		ET1_ERXD1/ RMII1_RXD1			
156		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
157		P94	A20/D20		ET1_ERXD0/ RMII1_RXD0			
158		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
159		P93	A19/D19	POE0#	ET1_LINKSTA/CTS7#/ RTS7#/SS7#			AN117
160		P92	A18/D18	POE4#	ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7			AN116
161		P91	A17/D17		ET1_COL/SCK7			AN115
162	VSS							
163		P90	A16/D16		ET1_RX_DV/ TXD7/SMOSI7/SSDA7			AN114
164	VCC							
165		P47					IRQ15-DS	AN007
166		P46					IRQ14-DS	AN006
167		P45					IRQ13-DS	AN005
168		P44					IRQ12-DS	AN004
169		P43					IRQ11-DS	AN003
170		P42					IRQ10-DS	AN002
171		P41					IRQ9-DS	AN001
172	VREFL0							

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
C10		P63	CS3#/CAS#					
C11		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12	MMC_D4-B		ANEX0
C12		P70	SDCLK					
C13	VSS							
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
D2		PF5					IRQ4	
D3		P03					IRQ11	DA0
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
D5	VCC							
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D8		P60	CS0#					
D9		P64	CS4#/WE#					
D10		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1		MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D11	VCC							
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0		IRQ5	AN103
D13		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E1	VSS							
E2	VCL							
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E4	EMLE							
E5		P44					IRQ12-DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E11		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
E12		P65	CS5#/CKE					
E13		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	XCIN							
F2	XCOUT							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
F4	VBATT							
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F11	VSS							
F12		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4)

Pin Number 100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C8		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
C9		PE5	D13[A13/ D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0		IRQ5	AN103
C10		PE4	D12[A12/ D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2			AN102
D1	XCIN							
D2	XCOUT							
D3	MD/FINED							
D4	VBATT							
D5		P45					IRQ13-DS	AN005
D6		P46					IRQ14-DS	AN006
D7		PE6	D14[A14/ D14]	MTIOC6C/GTIOC3B-E/TIC1		MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
D8		PE7	D15[A15/ D15]	MTIOC6A/GTIOC3A-E/TOC1		MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D9		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/GTIOC2A-C/TIOCB0/PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
E5		P41					IRQ9-DS	AN001
E6		PA2	A2	MTIOC7A/GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
E7		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
E8		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
E9		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
E10		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35					NMI	
F4		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	

Table 4.1 List of I/O Registers (Address Order) (4 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACAa
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACAa
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2 ICLK		DMACAa
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACAa
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACAa
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACAa
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACAa
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACAa
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACAa
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACAa
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACAa

Table 4.1 List of I/O Registers (Address Order) (12 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7908h	ICU	Software Configurable Interrupt A Request Register 8	PIAR8	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7909h	ICU	Software Configurable Interrupt A Request Register 9	PIAR9	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Ah	ICU	Software Configurable Interrupt A Request Register A	PIARA	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D0h	ICU	Software Configurable Interrupt A Source Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D1h	ICU	Software Configurable Interrupt A Source Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D2h	ICU	Software Configurable Interrupt A Source Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D3h	ICU	Software Configurable Interrupt A Source Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D4h	ICU	Software Configurable Interrupt A Source Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D5h	ICU	Software Configurable Interrupt A Source Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D6h	ICU	Software Configurable Interrupt A Source Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D7h	ICU	Software Configurable Interrupt A Source Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D8h	ICU	Software Configurable Interrupt A Source Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D9h	ICU	Software Configurable Interrupt A Source Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DAh	ICU	Software Configurable Interrupt A Source Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DBh	ICU	Software Configurable Interrupt A Source Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DCh	ICU	Software Configurable Interrupt A Source Select Register 220	SLIAR220	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DDh	ICU	Software Configurable Interrupt A Source Select Register 221	SLIAR221	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DEh	ICU	Software Configurable Interrupt A Source Select Register 222	SLIAR222	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DFh	ICU	Software Configurable Interrupt A Source Select Register 223	SLIAR223	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E0h	ICU	Software Configurable Interrupt A Source Select Register 224	SLIAR224	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E1h	ICU	Software Configurable Interrupt A Source Select Register 225	SLIAR225	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E2h	ICU	Software Configurable Interrupt A Source Select Register 226	SLIAR226	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E3h	ICU	Software Configurable Interrupt A Source Select Register 227	SLIAR227	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E4h	ICU	Software Configurable Interrupt A Source Select Register 228	SLIAR228	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E5h	ICU	Software Configurable Interrupt A Source Select Register 229	SLIAR229	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E6h	ICU	Software Configurable Interrupt A Source Select Register 230	SLIAR230	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E7h	ICU	Software Configurable Interrupt A Source Select Register 231	SLIAR231	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E8h	ICU	Software Configurable Interrupt A Source Select Register 232	SLIAR232	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E9h	ICU	Software Configurable Interrupt A Source Select Register 233	SLIAR233	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79EAh	ICU	Software Configurable Interrupt A Source Select Register 234	SLIAR234	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79EBh	ICU	Software Configurable Interrupt A Source Select Register 235	SLIAR235	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (15 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2, 3 PCLKB	2 ICLK	TPUa
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81E6h	PPG0	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E8h	PPG0	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E9h	PPG0	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EAh	PPG0	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EBh	PPG0	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81ECh	PPG0	Next Data Registers H*1	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EDh	PPG0	Next Data Registers L*2	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EEh	PPG0	Next Data Registers H*1	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81EFh	PPG0	Next Data Registers L*2	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F0h	PPG1	PPG Trigger Select Register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F6h	PPG1	PPG Output Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F7h	PPG1	PPG Output Mode Register	PMR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F8h	PPG1	Next Data Enable Registers H	NDERH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81F9h	PPG1	Next Data Enable Registers L	NDERL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FAh	PPG1	Output Data Registers H	PODRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FBh	PPG1	Output Data Registers L	PODRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FCh	PPG1	Next Data Registers H*3	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh	PPG1	Next Data Registers L*4	NDRL	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FEh	PPG1	Next Data Registers H*3	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FFh	PPG1	Next Data Registers L*4	NDRL2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR

Table 4.1 List of I/O Registers (Address Order) (23 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A046h	SMCI2	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A049h	SCI2	I^2C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Ah	SCI2	I^2C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Bh	SCI2	I^2C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Ch	SCI2	I^2C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Eh	SCI2	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Fh	SCI2	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A04Eh	SCI2	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 A050h	SCI2	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A051h	SCI2	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A050h	SCI2	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIg, SCIh
0008 A052h	SCI2	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A060h	SCI3	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A061h	SCI3	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A062h	SCI3	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A063h	SCI3	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A064h	SCI3	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A065h	SCI3	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A066h	SMCI3	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh
0008 A067h	SCI3	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIg, SCIh

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB)*5	USBb

Table 5.6 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	–3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	min	typ	max	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 5.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

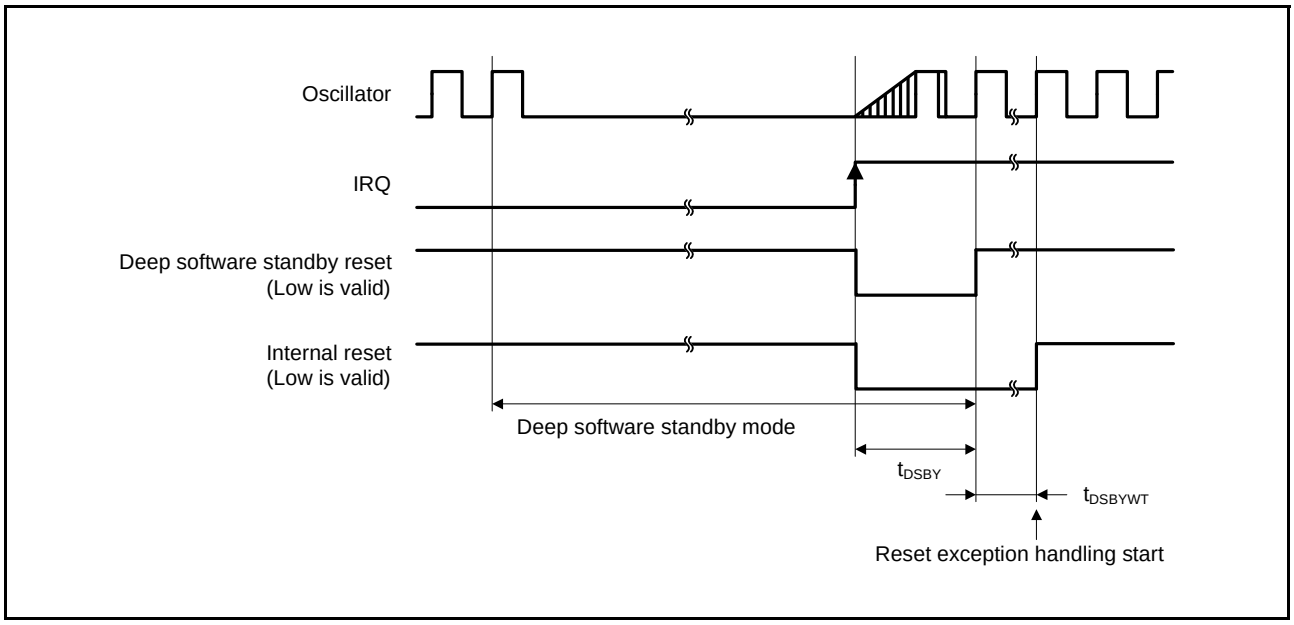


Figure 5.13 Deep Software Standby Mode Cancellation Timing

Table 5.36 RIIC Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

Table 5.43 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 5.77
	Rise time	t_{FR}	4	—	20	ns	
	Fall time	t_{FF}	4	—	20	ns	
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
			40.5	—	49.5	Ω	USBA: Rs not necessary (PHYSET.REPSEL[1:0] = 01b and PHYSET.HSEB = 0)
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	kΩ	Idle state
			1.425	—	3.090	kΩ	At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

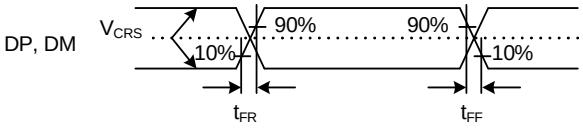


Figure 5.77 DP and DM Output Timing (Full-Speed)

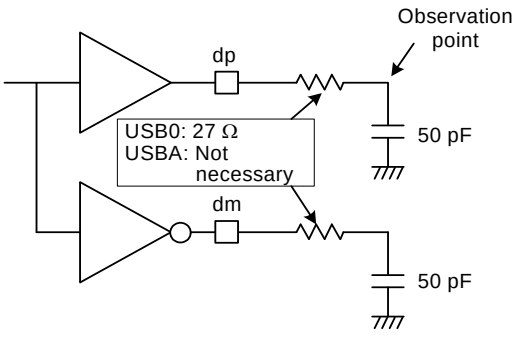


Figure 5.78 Test Circuit (Full-Speed)

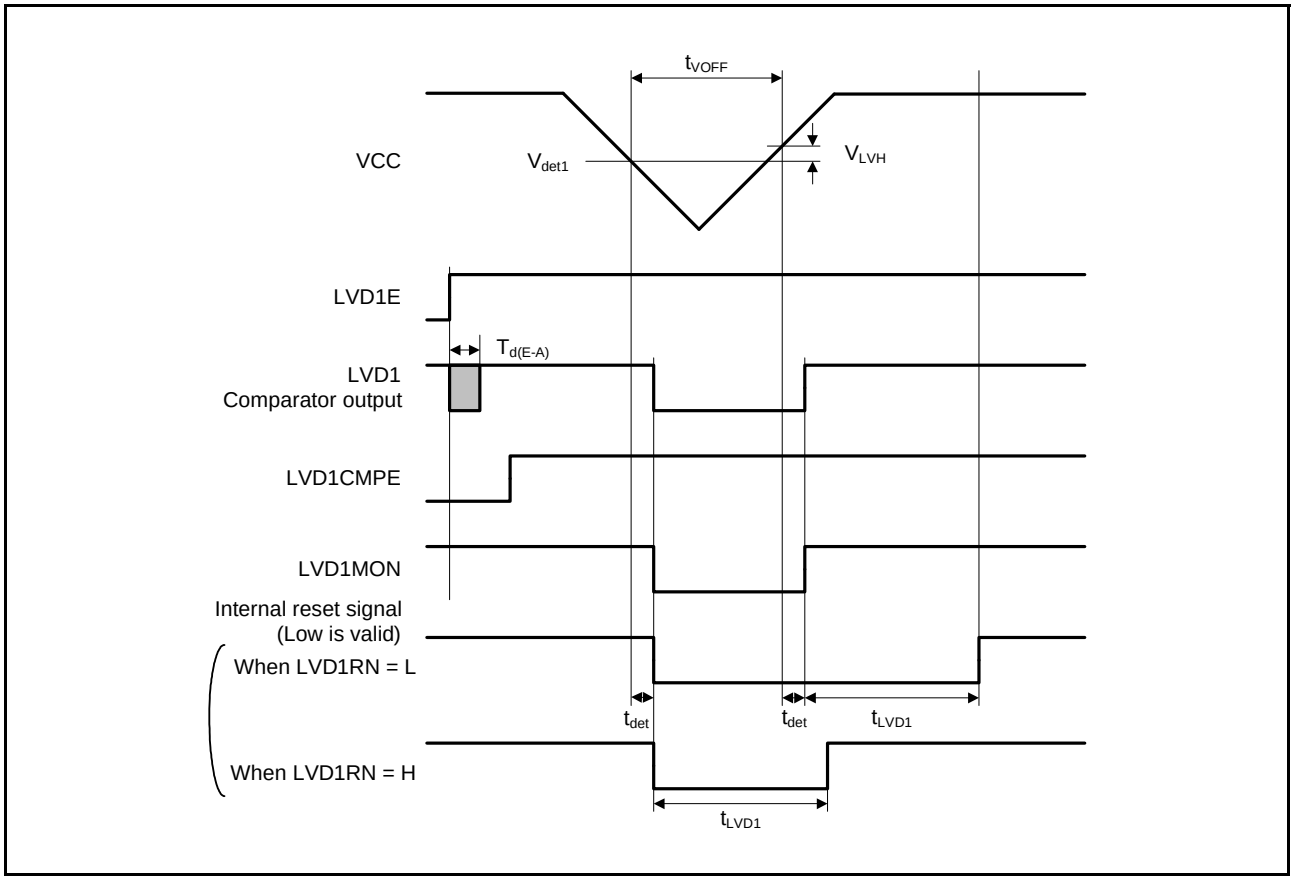


Figure 5.81 Voltage Detection Circuit Timing (V_{det1})

5.11 Flash Memory Characteristics

Table 5.53 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms
	8 Kbytes	t_{P8K}	—	29	176	—	13	80	ms
	32 Kbytes	t_{P32K}	—	116	704	—	52	320	ms
Programming time N_{PEC} > 100 times	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2	ms
	8 Kbytes	t_{P8K}	—	35	212	—	16	96	ms
	32 Kbytes	t_{P32K}	—	140	848	—	64	384	ms
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	71	216	—	39	120	ms
	32 Kbytes	t_{E32K}	—	254	864	—	141	480	ms
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	85	260	—	47	144	ms
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576	ms
Reprogramming/erasure cycle*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Times
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
Forced stop command		t_{FD}	—	—	32	—	—	20	µs
Data hold time*3		t_{DRP}	10	—	—	10	—	—	Year
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).
Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

REVISION HISTORY	RX64M Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.90	Feb 28, 2014	—	First edition, issued
1.00	Jul 31, 2014	Summary	
		1	■ Data transfer, changed
		1. Overview	
		—	FINEC (Pin), deleted
		2	Table 1.1 Outline of Specifications (1/9), changed
		3	Table 1.1 Outline of Specifications (2/9), changed
		6	Table 1.1 Outline of Specifications (5/9), changed
		7	Table 1.1 Outline of Specifications (6/9), changed
		8	Table 1.1 Outline of Specifications (7/9), changed
		9	Table 1.1 Outline of Specifications (8/9), changed
		10	Table 1.1 Outline of Specifications (9/9), changed
		16	Figure 1.1 How to Read the Product Part Number, changed
		19	Table 1.4 Pin Functions (2/8), changed
		20	Table 1.4 Pin Functions (3/8), changed
		25	Table 1.4 Pin Functions (8/8), note added
		2. CPU, added	
		3. Address Space, added	
		4. I/O Registers, added	
		5. Electrical Characteristics, added	
		Appendix 1. Package Dimensions, added	

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 24, 2016	All	Terms unified: GPTa → GPTA LQFP → LFQFP	
		Features		
		1	AES key lengths, changed	TN-RX*-A122A/E
		1. Overview		
		2	Table 1.1 Outline of Specifications (1/9), changed	TN-RX*-A127A/E
		5	Table 1.1 Outline of Specifications (4/9), changed	
		10	Table 1.1 Outline of Specifications (9/9), changed	TN-RX*-A122A/E
		28	Figure 1.5 Pin Assignment (176-Pin LFQFP), changed	
		48	Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5), changed	
		49	Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5), changed	
		52	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/5), changed	
		55	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/5), changed	
		58	Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4), changed	
		59	Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4), changed	
		63	Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/4), changed	
		4. I/O Registers		
		71	(4) Notes on Sleep Mode and Mode Transitions, added	
		73	Table 4.1 List of I/O Registers (Address Order) (2 / 67) 0008 1200h, 0008 1201h, 0008 1204h, 0008 1208h, added	TN-RX*-A127A/E

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