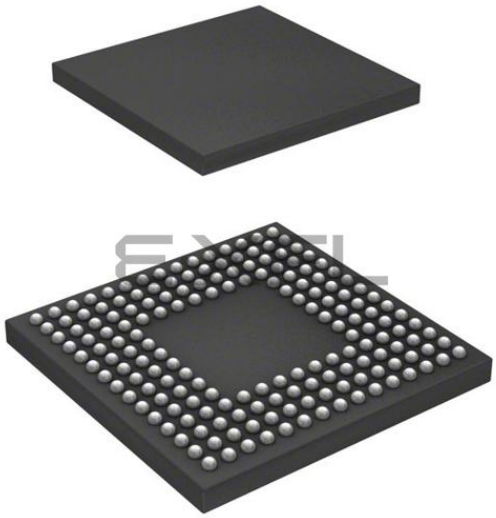

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgddbg-21

Table 1.1 Outline of Specifications (2/9)

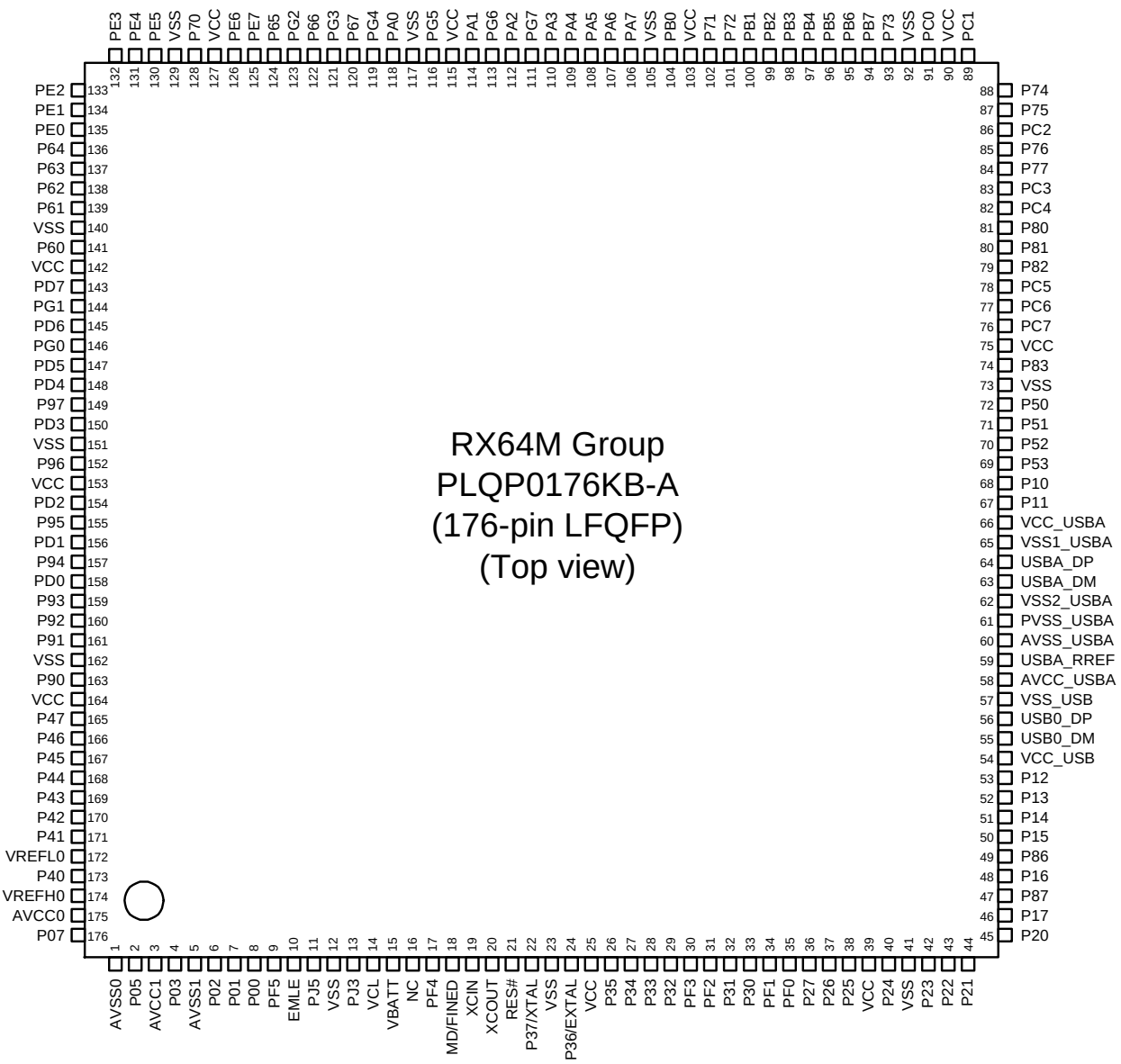
Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.

Table 1.1 Outline of Specifications (3/9)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICUA)	• Peripheral function interrupts: 293 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 7 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 156 sources.)
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACAa)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller (EXDMACa)	• 2 channels Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDACKn signal • Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	• I/O ports for the 177-pin TFLGA, 176-pin LFBGA, and 176-pin LFQFP I/O pins: 127 Input pin: 1 Pull-up resistors: 127 Open-drain outputs: 127 5-V tolerance: 19 • I/O ports for the 145-pin TFLGA and 144-pin LFQFP I/O pins: 111 Input pin: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 18 • I/O ports for the 100-pin TFLGA and 100-pin LFQFP I/O pins: 78 Input pin: 1 Pull-up resistors: 78 Open-drain outputs: 78 5-V tolerance: 17
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 119 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.

Table 1.1 Outline of Specifications (7/9)

Classification	Module/Function	Description
Communication function	I²C bus interface (RIICa)	• 2 channels (only channel 0 can be used in fast-mode plus) Communication formats I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPIa)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC
	Quad serial peripheral interface (QSPI)	• 1 channel • Connectable with serial flash memory equipped with multiple input and output lines (i.e. for single, dual, or quad operation) • Programmable bit length and selectable active sense and phase of the clock signal • Sequential execution of transfer • LSB or MSB first is selectable.
Serial sound interface (SSI)		• 2 channels • Full-duplex transfer is possible (only on channel 0). • Support for multiple audio formats • Support for master or slave operation • Bit clock frequency is selectable from four different types (16 fs, 32 fs, 48 fs, and 64 fs). • Support for 8-/16-/18-/20-/22-/24 bit data formats • Internal 8-stage FIFO for transmission and reception • Stopping SSIWS when data transfer is stopped is selectable.
Sampling rate converter (SRC)		• 1 channel • Data formats: 32-bit stereo (16 bits for the left, 16 bits for the right) and 16-bit monaural. • Input sampling rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz • Output sampling rates: 32, 44.1, 48, 8*2 or 16 kHz*2
SD host interface (SDHI)*4		• 1 channel • Transfer speed: Supports high-speed mode (15 MB/s) and default speed mode (10 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
MMC host interface (MMCIF)		• 1 channel • Transfer speed: Supports high-speed mode (30 MB/s) and Backward-compatible mode (25 MB/s) • Compliant with JEDEC STANDARD JESD84-A441 (DDR is not supported) • Interface for Multimedia Cards (MMCs) • Device buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card detection interrupt, error/timeout interrupt, normal operation interrupt • DMA transfer requests: CE_DATA write and CE_DATA read • Support for card detection, boot operation, high priority interrupt (HPI)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LFQFP).

Figure 1.5 Pin Assignment (176-Pin LFQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
85		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
86		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
87		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
88		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
89		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
90	VCC							
91		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
92	VSS							
93		P73	CS3#	PO16	ET0_WOL			
94		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
95		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
97		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
99		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC			
102		P71	A18/CS1#		ET0_MDIO			
103	VCC							
104		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
105	VSS							
106		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
107		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
108		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	MD/FINED							
17	XCIN							
18	XCOUT							
19	RES							
20	XTAL	P37						
21	VSS							
22	EXTAL	P36						
23	VCC							
24		P35					NMI	
25	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
26		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
27		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#		IRQ1-DS	
29	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/SSCL1		IRQ0-DS	
30	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1			
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1			
32		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
33		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
34		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0	PIXD7		
35		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		

Table 4.1 List of I/O Registers (Address Order) (7 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 3822h	BSC	CS2 Control Register	CS2CR	16	16	1, 2 BCLK		Buses
0008 382Ah	BSC	CS2 Recovery Cycle Register	CS2REC	16	16	1, 2 BCLK		Buses
0008 3832h	BSC	CS3 Control Register	CS3CR	16	16	1, 2 BCLK		Buses
0008 383Ah	BSC	CS3 Recovery Cycle Register	CS3REC	16	16	1, 2 BCLK		Buses
0008 3842h	BSC	CS4 Control Register	CS4CR	16	16	1, 2 BCLK		Buses
0008 384Ah	BSC	CS4 Recovery Cycle Register	CS4REC	16	16	1, 2 BCLK		Buses
0008 3852h	BSC	CS5 Control Register	CS5CR	16	16	1, 2 BCLK		Buses
0008 385Ah	BSC	CS5 Recovery Cycle Register	CS5REC	16	16	1, 2 BCLK		Buses
0008 3862h	BSC	CS6 Control Register	CS6CR	16	16	1, 2 BCLK		Buses
0008 386Ah	BSC	CS6 Recovery Cycle Register	CS6REC	16	16	1, 2 BCLK		Buses
0008 3872h	BSC	CS7 Control Register	CS7CR	16	16	1, 2 BCLK		Buses
0008 387Ah	BSC	CS7 Recovery Cycle Register	CS7REC	16	16	1, 2 BCLK		Buses
0008 3880h	BSC	CS Recovery Cycle Insertion Enable Register	CSRECEN	16	16	1, 2 BCLK		Buses
0008 3C00h	BSC	SDC Control Register	SDCCR	8	8	1, 2 BCLK		Buses
0008 3C01h	BSC	SDC Mode Register	SDCMOD	8	8	1, 2 BCLK		Buses
0008 3C02h	BSC	SDRAM Access Mode Register	SDAMOD	8	8	1, 2 BCLK		Buses
0008 3C10h	BSC	SDRAM Self-Refresh Control Register	SDSELF	8	8	1, 2 BCLK		Buses
0008 3C14h	BSC	SDRAM Refresh Control Register	SDRFCR	16	16	1, 2 BCLK		Buses
0008 3C16h	BSC	SDRAM Auto-Refresh Control Register	SDRFEN	8	8	1, 2 BCLK		Buses
0008 3C20h	BSC	SDRAM Initialization Sequence Control Register	SDICR	8	8	1, 2 BCLK		Buses
0008 3C24h	BSC	SDRAM Initialization Register	SDIR	16	16	1, 2 BCLK		Buses
0008 3C40h	BSC	SDRAM Address Register	SDADR	8	8	1, 2 BCLK		Buses
0008 3C44h	BSC	SDRAM Timing Register	SDTR	32	32	1, 2 BCLK		Buses
0008 3C48h	BSC	SDRAM Mode Register	SDMOD	16	16	1, 2 BCLK		Buses
0008 3C50h	BSC	SDRAM Status Register	SDSR	8	8	1, 2 BCLK		Buses
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK		MPU
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK		MPU
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK		MPU
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK		MPU
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK		MPU
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK		MPU
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK		MPU
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK		MPU
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK		MPU
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK		MPU
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK		MPU
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK		MPU
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK		MPU
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK		MPU
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK		MPU
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK		MPU
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK		MPU
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK		MPU
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK		MPU
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK		MPU
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK		MPU
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK		MPU
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK		MPU
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK		MPU

Table 4.1 List of I/O Registers (Address Order) (17 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8310h	RIIC0	I2C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8311h	RIIC0	I2C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8312h	RIIC0	I2C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8313h	RIIC0	I2C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I2C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I2C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I2C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I2C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I2C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I2C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I2C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I2C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I2C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I2C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I2C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I2C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I2C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I2C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8528h	MMCIF	Response Register 1	CERESP1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 852Ch	MMCIF	Response Register 0	CERESP0	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8530h	MMCIF	Automatically Issued CMD12 Response Register	CERESPCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8534h	MMCIF	Data Register	CEDATA	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 853Ch	MMCIF	Boot Operation Setting Register	CEBOOT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8540h	MMCIF	Interrupt status Flag Register	CEINT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8544h	MMCIF	Interrupt request Enable Register	CEINTEN	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8548h	MMCIF	Status Register 1	CEHOSTSTS1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 854Ch	MMCIF	Status Register 2	CEHOSTSTS2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8570h	MMCIF	MMC Detection and Port Control Register	CEDETECT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8574h	MMCIF	Special Mode Setting Register	CEADDMODE	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (47 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0310h	ETHERC1	ETHERC Status Register	ECSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0318h	ETHERC1	ETHERC Interrupt Enable Register	ECSIPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0320h	ETHERC1	PHY Interface Register	PIR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0328h	ETHERC1	PHY Status Register	PSR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0340h	ETHERC1	Random Number Generation Counter Upper Limit Setting Register	RDMLR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0350h	ETHERC1	Interpacket Gap Register	IPGR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0354h	ETHERC1	Automatic PAUSE Frame Register	APR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0358h	ETHERC1	Manual PAUSE Frame Register	MPR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0360h	ETHERC1	Received PAUSE Frame Counter	RFCF	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0364h	ETHERC1	PAUSE Frame Retransmit Count Setting Register	TPAUSER	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0368h	ETHERC1	PAUSE Frame Retransmit Counter Register	TPAUSECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 036Ch	ETHERC1	Broadcast Frame Receive Count Setting Register	BCFRR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03C0h	ETHERC1	MAC Address Upper Bit Register	MAHR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03C8h	ETHERC1	MAC Address Lower Bit Register	MALR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03D0h	ETHERC1	Transmit Retry Over Counter Register	TROCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03D4h	ETHERC1	Late Collision Detect Counter Register	CDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03D8h	ETHERC1	Lost Carrier Counter Register	LCCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03DCh	ETHERC1	Carrier Not Detect Counter Register	CNDCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03E4h	ETHERC1	CRC Error Frame Receive Counter Register	CEFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03E8h	ETHERC1	Frame Receive Error Counter Register	FRECR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03ECh	ETHERC1	Too-Short Frame Receive Counter Register	TSFRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F0h	ETHERC1	Too-Long Frame Receive Counter Register	TLFRCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F4h	ETHERC1	Received Alignment Error Frame Counter Register	RFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 03F8h	ETHERC1	Multicast Address Frame Receive Counter Register	MAFCR	32	32	13, 14 PCLKA	2 to 7 ICLK	ETHERC
000C 0400h	PTPEDMAC	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0408h	PTPEDMAC	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0410h	PTPEDMAC	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0418h	PTPEDMAC	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0420h	PTPEDMAC	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0428h	PTPEDMAC	PTP/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0430h	PTPEDMAC	PTP/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a

Table 4.1 List of I/O Registers (Address Order) (50 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1322h	MTU0	Timer General Register F	TGRF	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1324h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1326h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1328h	MTU0	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1380h	MTU1	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1381h	MTU1	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1382h	MTU1	Timer I/O Control Register	TIOR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1384h	MTU1	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1385h	MTU1	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1386h	MTU1	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1388h	MTU1	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 138Ah	MTU1	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1390h	MTU1	Timer Input Capture Control Register	TICCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1391h	MTU1	Timer Mode Register 3	TMDR3	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1394h	MTU1	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 13A0h	MTU1	Timer Longword Counter	TCNTLW	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 13A4h	MTU1	Timer Longword General Register	TGRALW	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 13A8h	MTU1	Timer Longword General Register	TGRBLW	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1400h	MTU2	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1401h	MTU2	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1402h	MTU2	Timer I/O Control Register	TIOR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1404h	MTU2	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1405h	MTU2	Timer Status Register	TSR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1406h	MTU2	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1408h	MTU2	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ah	MTU2	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 140Ch	MTU2	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1600h	MTU8	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1601h	MTU8	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1602h	MTU8	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1603h	MTU8	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1604h	MTU8	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1606h	MTU8	Timer Control Register 2	TCR2	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1608h	MTU8	Timer Counter	TCNT	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 160Ch	MTU8	Timer General Register A	TGRA	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1610h	MTU8	Timer General Register B	TGRB	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1614h	MTU8	Timer General Register C	TGRC	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1618h	MTU8	Timer General Register D	TGRD	32	32	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A00h	MTU6	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (60 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4D20h	EPTPC1	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D24h	EPTPC1	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D28h	EPTPC1	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D2Ch	EPTPC1	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D30h	EPTPC1	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D34h	EPTPC1	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D38h	EPTPC1	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D3Ch	EPTPC1	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D40h	EPTPC1	Frame Reception Filter Setting Register	FFLTR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D60h	EPTPC1	Frame Reception Filter MAC Address 0 Setting Registers	FMAC0RU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D64h	EPTPC1	Frame Reception Filter MAC Address 0 Setting Registers	FMAC0RL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D68h	EPTPC1	Frame Reception Filter MAC Address 1 Setting Registers	FMAC1RU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D6Ch	EPTPC1	Frame Reception Filter MAC Address 1 Setting Registers	FMAC1RL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC0h	EPTPC1	Asymmetric Delay Setting Register	DASYMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC4h	EPTPC1	Asymmetric Delay Setting Register	DASYMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC8h	EPTPC1	Timestamp Latency Setting Register	TSLATR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DCCh	EPTPC1	SYNFP Operation Setting Register	SYCONFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DD0h	EPTPC1	SYNFP Frame Format Setting Register	SYFORMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DD4h	EPTPC1	Response Message Reception Timeout Register	RSTOUTR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000D 0000h	SCIFA8	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0004h	SCIFA8	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0006h	SCIFA8	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0008h	SCIFA8	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ah	SCIFA8	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ch	SCIFA8	FIFO Control Register	FCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Eh	SCIFA8	FIFO Data Count Register	FDR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0010h	SCIFA8	Serial Port Register	SPTR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0012h	SCIFA8	Line Status Register	LSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0014h	SCIFA8	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0016h	SCIFA8	FIFO Trigger Control Register	FTCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0020h	SCIFA9	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0024h	SCIFA9	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0026h	SCIFA9	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0028h	SCIFA9	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 002Ah	SCIFA9	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA

Table 5.6 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}	—	—	3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}	—	—	7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	–3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

5.3.1 Reset Timing

Table 5.10 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 5.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 5.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	62	—	63	t_{Lcyc}	Figure 5.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	108	—	116	t_{Lcyc}	

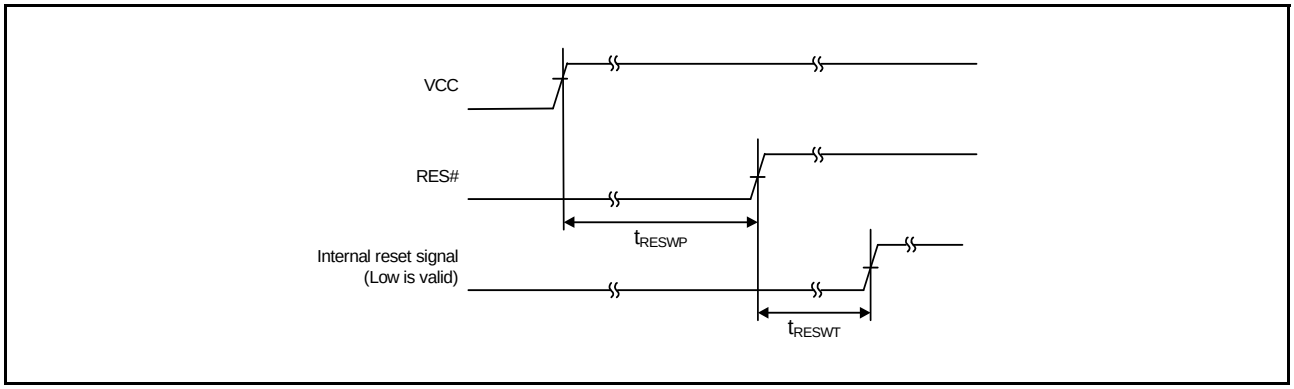


Figure 5.1 Reset Input Timing at Power-On

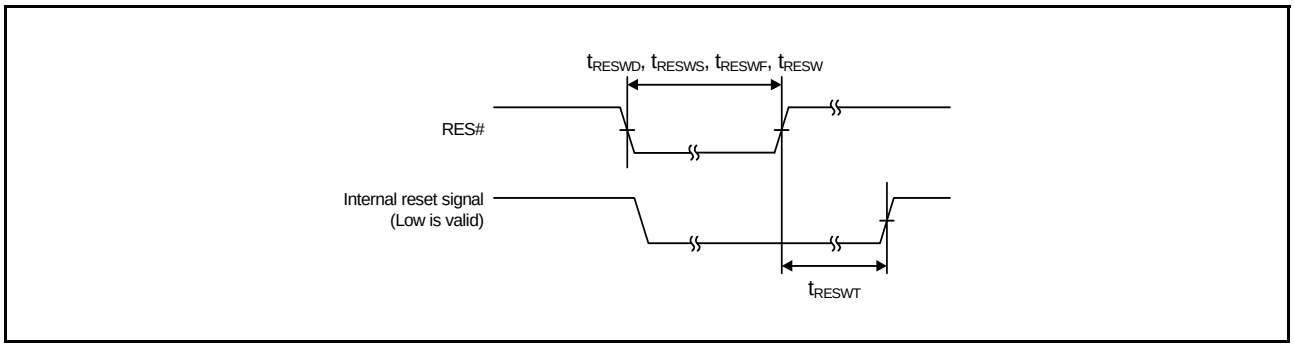


Figure 5.2 Reset Input Timing

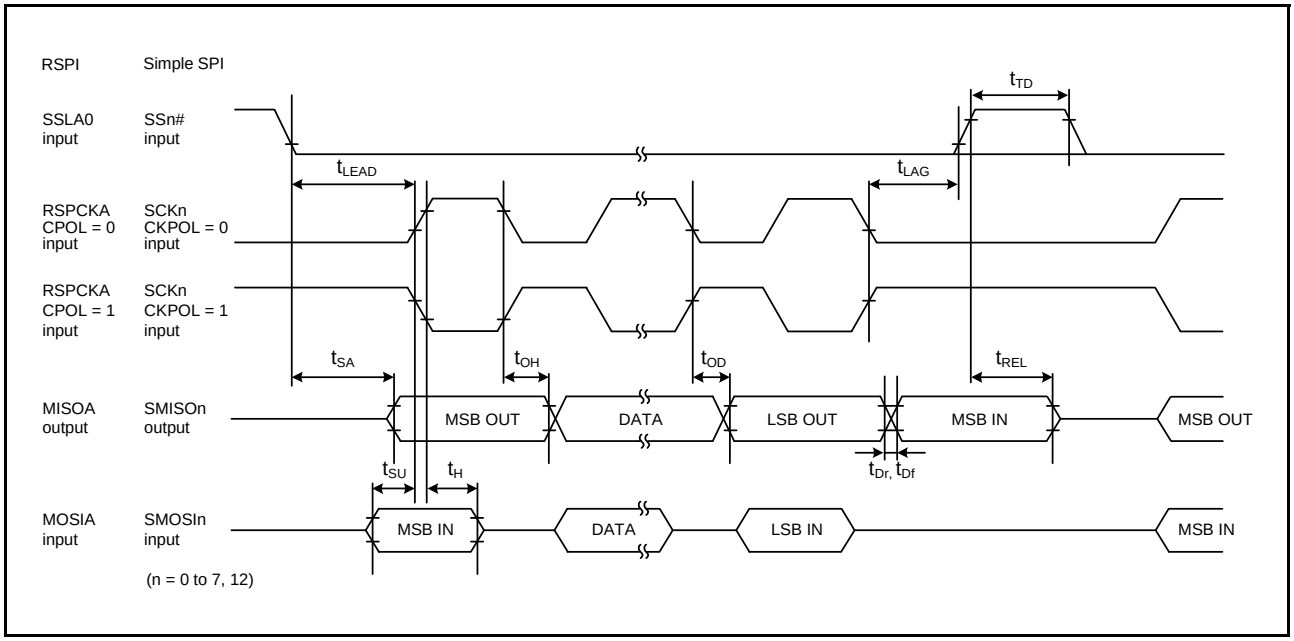


Figure 5.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

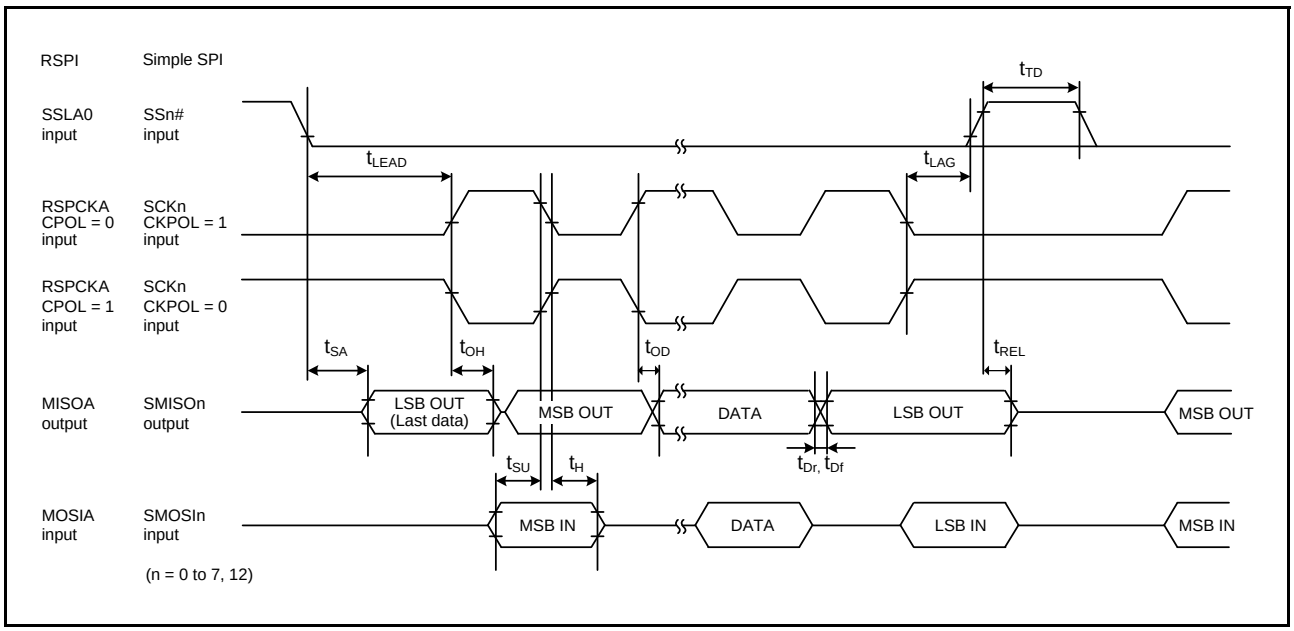


Figure 5.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

5.4 USB Characteristics

Table 5.42 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 5.75
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

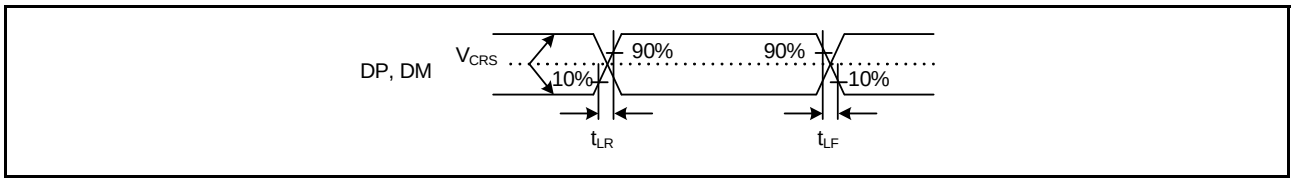


Figure 5.75 DP and DM Output Timing (Low Speed)

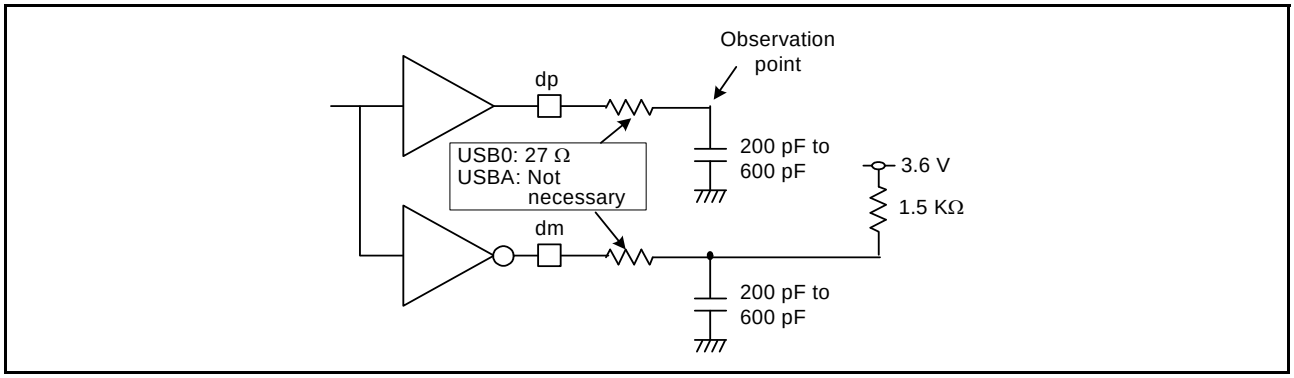


Figure 5.76 Test Circuit (Low Speed)

5.5 A/D Conversion Characteristics

Table 5.45 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.06 (0.40 + 0.25) *2	—	—	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	μs	
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	0.48 (0.267) *2	—	—	μs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.0	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

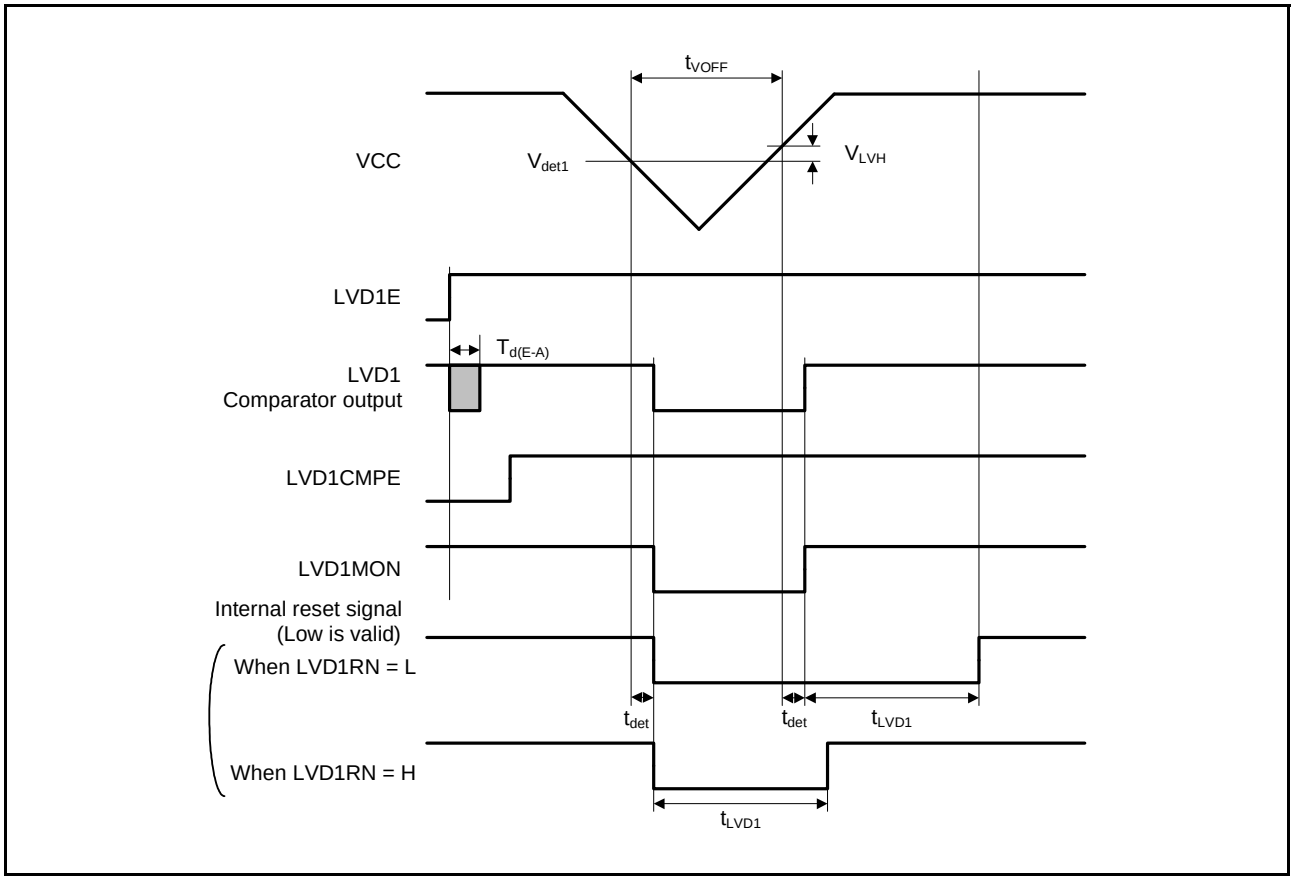


Figure 5.81 Voltage Detection Circuit Timing (V_{det1})

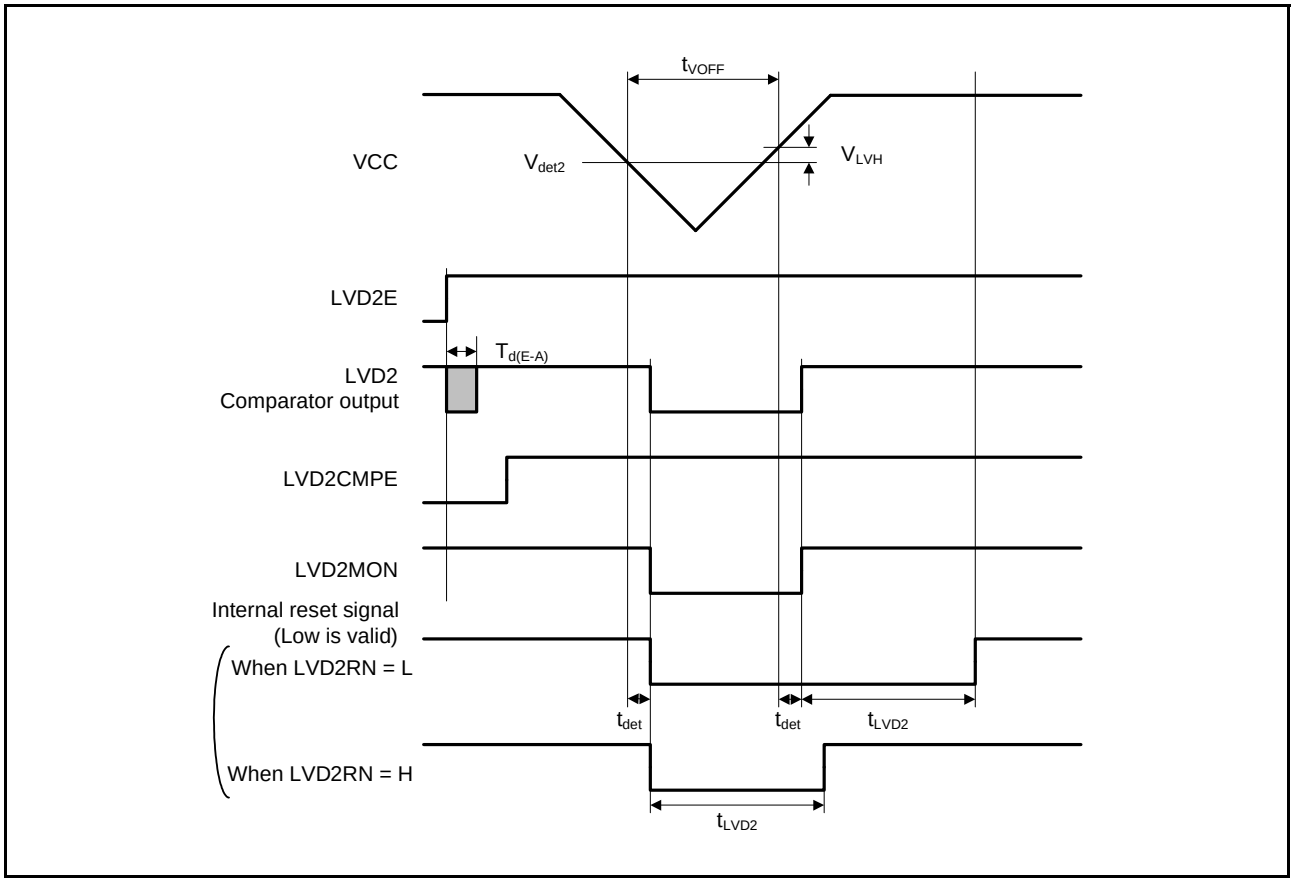


Figure 5.82 Voltage Detection Circuit Timing (V_{det2})

5.11 Flash Memory Characteristics

Table 5.53 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms
	8 Kbytes	t_{P8K}	—	29	176	—	13	80	ms
	32 Kbytes	t_{P32K}	—	116	704	—	52	320	ms
Programming time N_{PEC} > 100 times	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2	ms
	8 Kbytes	t_{P8K}	—	35	212	—	16	96	ms
	32 Kbytes	t_{P32K}	—	140	848	—	64	384	ms
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	71	216	—	39	120	ms
	32 Kbytes	t_{E32K}	—	254	864	—	141	480	ms
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	85	260	—	47	144	ms
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576	ms
Reprogramming/erasure cycle*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Times
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
Forced stop command		t_{FD}	—	—	32	—	—	20	µs
Data hold time*3		t_{DRP}	10	—	—	10	—	—	Year
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).
Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

5.12 Boundary Scan

Table 5.55 Boundary Scan Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.86
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.87
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.88
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

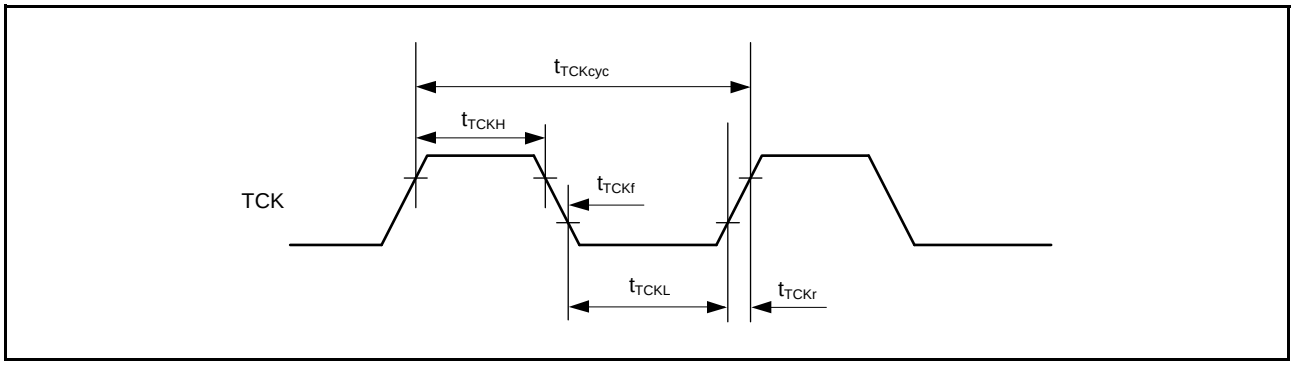


Figure 5.86 Boundary Scan TCK Timing

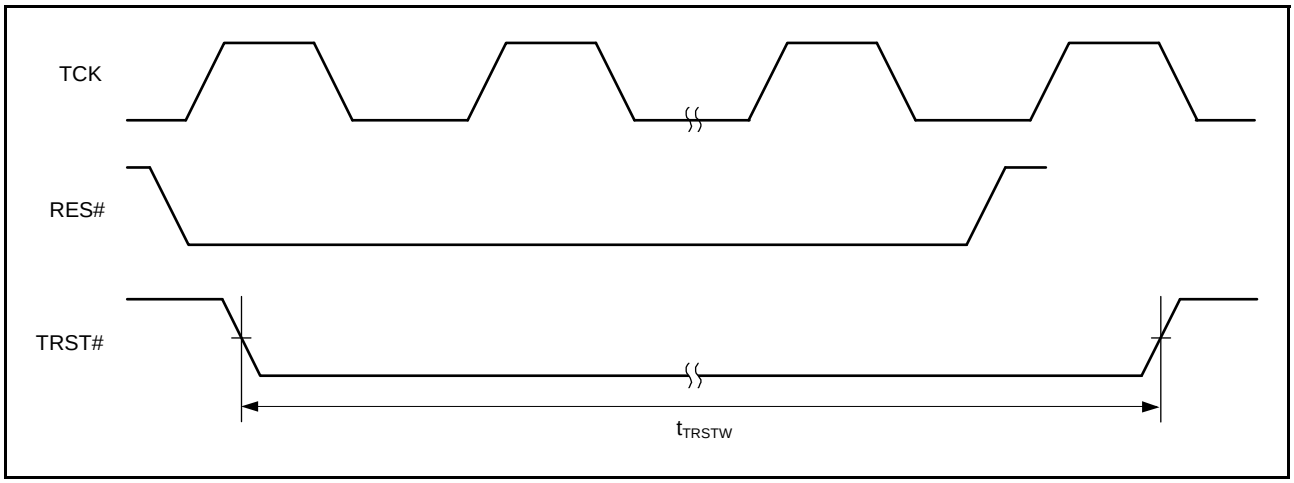


Figure 5.87 Boundary Scan TRST# Timing