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Details

Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mgddfc-31

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (7/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
R11	VCC							
R12		P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
R13		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
R14		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
R15		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	

Note 1. The 176-pin LFBGA does not include the E5 pin.

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (1/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
A1	AVSS0							
A2		P07					IRQ15	ADTRG0#
A3		P40					IRQ8-DS	AN000
A4		P42					IRQ10-DS	AN002
A5		P45					IRQ13-DS	AN005
A6		P90	A16		TXD7/SMOSI7/SSDA7			AN114
A7		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
A8		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
A9		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B	IRQ6	AN106
A10	VSS							
A11		P62	CS2#/RAS#					
A12		PE1	D9[A9/D9]	MTIOC4C/MTIOC3B/ GTIOC1B-A/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12	MMC_D5-B		ANEX1
A13		PE3	D11[A11/D11]	MTIOC4B/ GTIOC2A-A/PO26/ POE8#/TOC3	CTS12#/RTS12#/ SS12#/ET0_ERXD3/	MMC_D7-B		AN101
B1	AVCC1							
B2	AVCC0							
B3		P05					IRQ13	DA1
B4	VREFL0							
B5		P43					IRQ11-DS	AN003
B6		P47					IRQ15-DS	AN007
B7		P91	A17		SCK7			AN115
B8		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
B9		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
B10	VCC							
B11		P61	CS1#/SDCS#					
B12		PE2	D10[A10/D10]	MTIOC4A/ GTIOC0B-A/PO23/ TIC3	RXD12/SMISO12/ SSCL12/RXDX12/	MMC_D6-B	IRQ7-DS	AN100
B13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2			AN102
C1	AVSS1							
C2		P02		TMCI1	SCK6		IRQ10	AN120
C3	VREFH0							
C4		P41					IRQ9-DS	AN001
C5		P46					IRQ14-DS	AN006
C6	VSS							
C7		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
C8		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15- DS	AN007
134		P46					IRQ14- DS	AN006
135		P45					IRQ13- DS	AN005
136		P44					IRQ12- DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10- DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

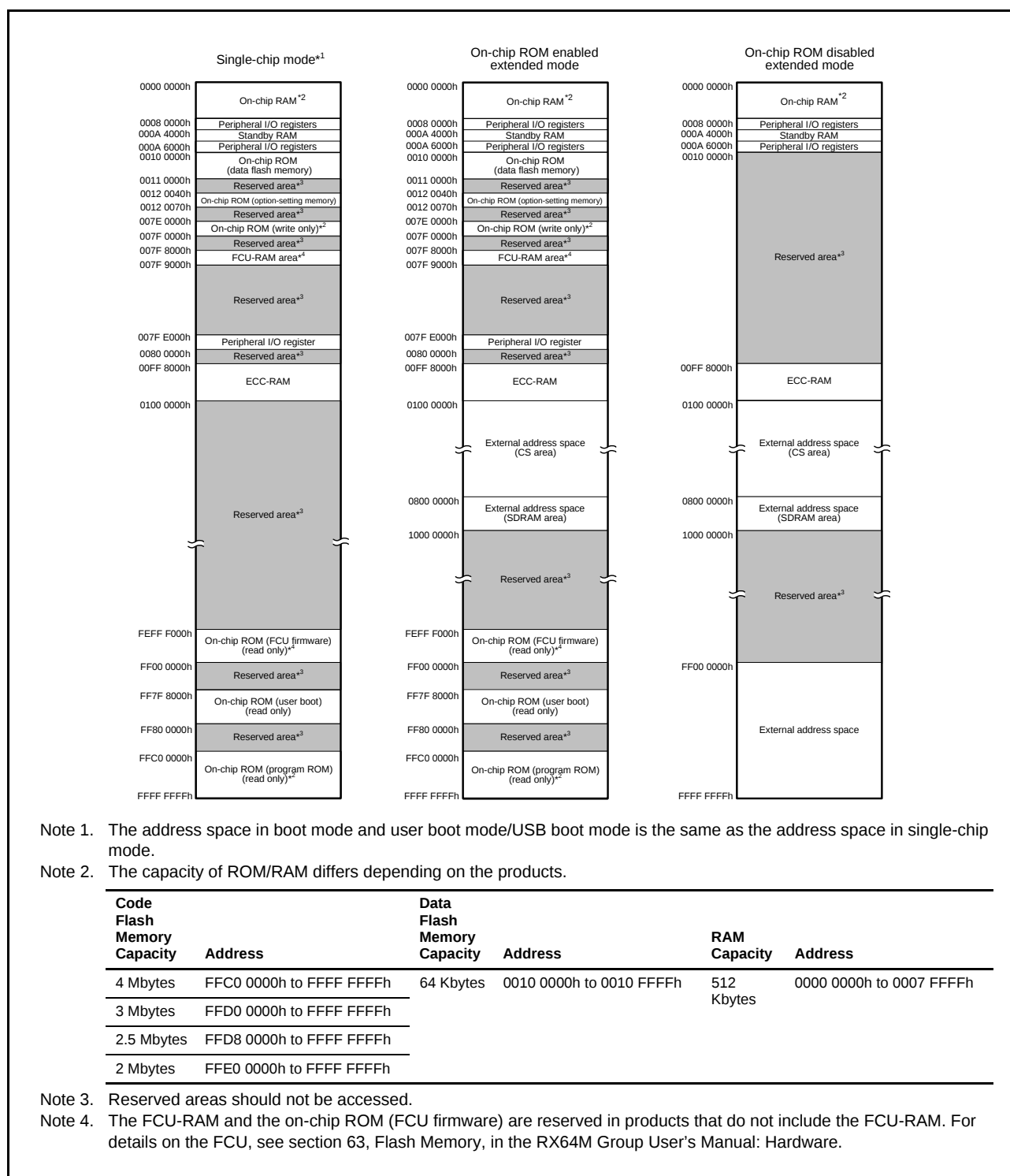


Figure 3.1 Memory Map in Each Operating Mode

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (9 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7709h	ICU	Software Configurable Interrupt B Request Register 9	PIBR9	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 770Ah	ICU	Software Configurable Interrupt B Request Register A	PIBRA	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7780h	ICU	Software Configurable Interrupt B Source Select Register X128	SLIBXR128	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7781h	ICU	Software Configurable Interrupt B Source Select Register X129	SLIBXR129	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7782h	ICU	Software Configurable Interrupt B Source Select Register X130	SLIBXR130	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7783h	ICU	Software Configurable Interrupt B Source Select Register X131	SLIBXR131	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7784h	ICU	Software Configurable Interrupt B Source Select Register X132	SLIBXR132	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7785h	ICU	Software Configurable Interrupt B Source Select Register X133	SLIBXR133	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7786h	ICU	Software Configurable Interrupt B Source Select Register X134	SLIBXR134	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7787h	ICU	Software Configurable Interrupt B Source Select Register X135	SLIBXR135	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7788h	ICU	Software Configurable Interrupt B Source Select Register X136	SLIBXR136	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7789h	ICU	Software Configurable Interrupt B Source Select Register X137	SLIBXR137	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ah	ICU	Software Configurable Interrupt B Source Select Register X138	SLIBXR138	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Bh	ICU	Software Configurable Interrupt B Source Select Register X139	SLIBXR139	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ch	ICU	Software Configurable Interrupt B Source Select Register X140	SLIBXR140	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Dh	ICU	Software Configurable Interrupt B Source Select Register X141	SLIBXR141	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Eh	ICU	Software Configurable Interrupt B Source Select Register X142	SLIBXR142	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Fh	ICU	Software Configurable Interrupt B Source Select Register X143	SLIBXR143	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7790h	ICU	Software Configurable Interrupt B Source Select Register 144	SLIBR144	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7791h	ICU	Software Configurable Interrupt B Source Select Register 145	SLIBR145	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7792h	ICU	Software Configurable Interrupt B Source Select Register 146	SLIBR146	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7793h	ICU	Software Configurable Interrupt B Source Select Register 147	SLIBR147	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7794h	ICU	Software Configurable Interrupt B Source Select Register 148	SLIBR148	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7795h	ICU	Software Configurable Interrupt B Source Select Register 149	SLIBR149	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7796h	ICU	Software Configurable Interrupt B Source Select Register 150	SLIBR150	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7797h	ICU	Software Configurable Interrupt B Source Select Register 151	SLIBR151	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7798h	ICU	Software Configurable Interrupt B Source Select Register 152	SLIBR152	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7799h	ICU	Software Configurable Interrupt B Source Select Register 153	SLIBR153	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Ah	ICU	Software Configurable Interrupt B Source Select Register 154	SLIBR154	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Bh	ICU	Software Configurable Interrupt B Source Select Register 155	SLIBR155	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (16 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR01	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8209h	TMR1	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR01	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Dh	TMR1	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8219h	TMR3	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Dh	TMR3	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	CRC
0008 8300h	RIIC0	I ² C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8301h	RIIC0	I ² C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8302h	RIIC0	I ² C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8303h	RIIC0	I ² C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8304h	RIIC0	I ² C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8305h	RIIC0	I ² C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8306h	RIIC0	I ² C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8307h	RIIC0	I ² C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8308h	RIIC0	I ² C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8309h	RIIC0	I ² C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa

Table 4.1 List of I/O Registers (Address Order) (38 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C428h	RTC	RTC Control Register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ah	RTC	Frequency Register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ch	RTC	Frequency Register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb

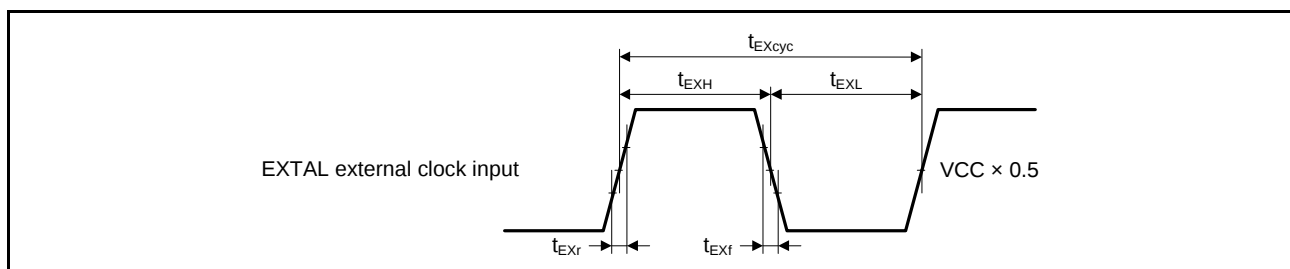
Table 4.1 List of I/O Registers (Address Order) (44 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 00F0h	USB0	PHY Cross Point Adjustment Register	PHYSLEW	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 0400h	USB	Deep Standby USB Transceiver Control/Pin Monitoring Register	DPUSR0R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 0404h	USB	Deep Standby USB Suspend/Resume Interrupt Register	DPUSR1R	32	32	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ⁺⁵	USBb
000A 0500h	PDC	PDC Control Register 0	PCCR0	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0504h	PDC	PDC Control Register 1	PCCR1	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0508h	PDC	PDC Status Register	PCSR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 050Ch	PDC	PDC Pin Monitor Register	PCMONR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0510h	PDC	PDC Receive Data Register	PCDR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0514h	PDC	Vertical Capture Register	VCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000A 0518h	PDC	Horizontal Capture Register	HCR	32	32	2, 3 PCLKB	2 ICLK	PDC
000C 0000h	EDMAC 0	EDMAC Mode Register	EDMR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0008h	EDMAC 0	EDMAC Transmit Request Register	EDTRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0010h	EDMAC 0	EDMAC Receive Request Register	EDRRR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0018h	EDMAC 0	Transmit Descriptor List Start Address Register	TDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0020h	EDMAC 0	Receive Descriptor List Start Address Register	RDLAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0028h	EDMAC 0	ETHERC/EDMAC Status Register	EESR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0030h	EDMAC 0	ETHERC/EDMAC Status Interrupt Enable Register	EESIPR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0038h	EDMAC 0	ETHERC/EDMAC Transmit/Receive Status Copy Enable Register	TRSCER	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0040h	EDMAC 0	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a
000C 0048h	EDMAC 0	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMAC a

Table 5.12 EXTAL Clock Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

**Figure 5.4 EXTAL External Clock Input Timing****Table 5.13 Main Clock Timing**

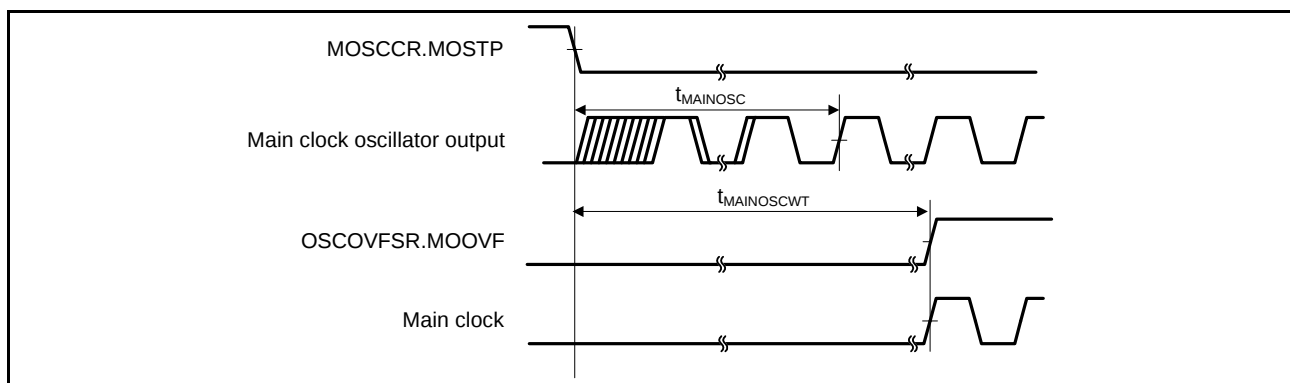
Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 5.5
Main clock oscillator stabilization wait time (crystal)	$t_{MAINSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{MAINSCWT} = [(MSTS[7:0] \text{ bits} \times 32) + 10] / f_{LOCO}$$

**Figure 5.5 Main Clock Oscillation Start Timing**

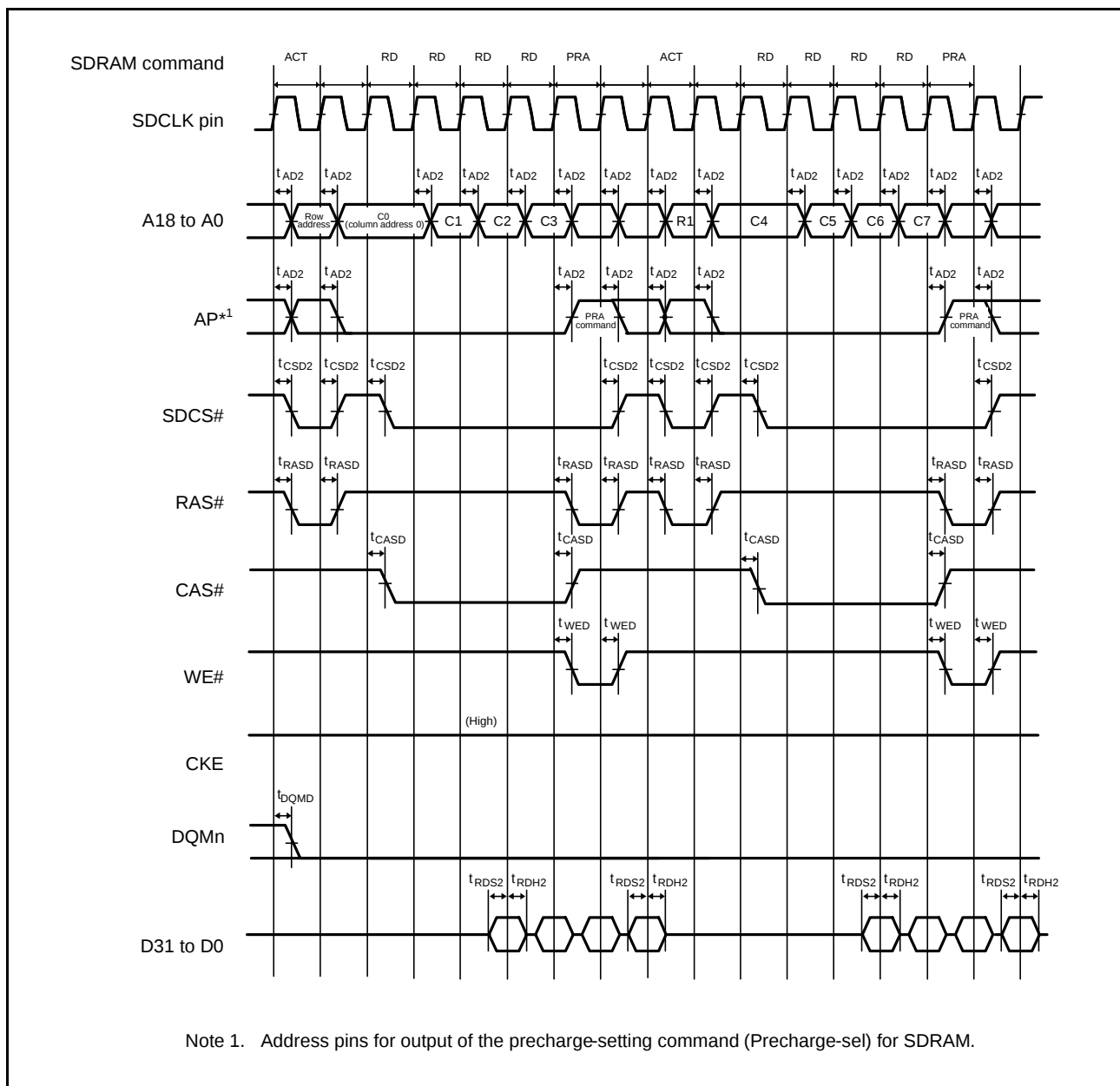


Figure 5.27 SDRAM Space Multiple Read Line Stride Bus Timing

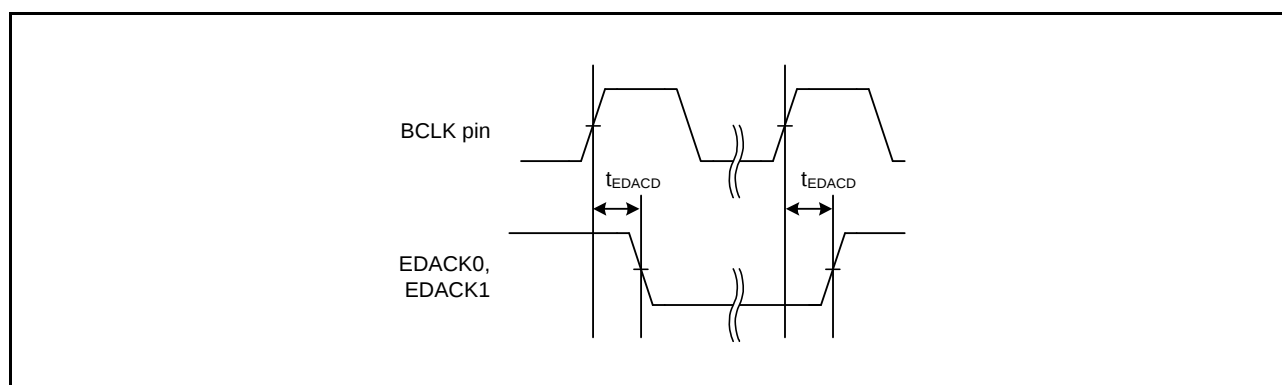


Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

Table 5.33 RSPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
High-drive output is selected by the driving ability control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2	
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{PAcyc}	Figure 5.46	
		Slave		8	4096			
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns		
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—			
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns		
		Slave		$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2$	—			
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns		
		Input		—	1	μs		
	Data input setup time	Master	t_{SU}	6	—	ns	Figure 5.47 to Figure 5.52	
		Slave		$8.3 - t_{PAcyc}$	—			
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—		ns
				t_H	t_{PAcyc}	—		
		Slave			$8.3 + 2 \times t_{PAcyc}$	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}		
		Slave		4	—	t_{PAcyc}		
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}		
		Slave		4	—	t_{PAcyc}		
	Data output delay time	Master	t_{OD}	—	6.3	ns		
		Slave		—	$3 \times t_{PAcyc} + 20$			
Data output hold time	Master	t_{OH}	0	—	ns			
	Slave		0	—				
Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns			
	Slave		$4 \times t_{PAcyc}$	—				
MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns			
	Input		—	1	μs			
SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns			
	Input		—	1	μs			
Slave access time			t_{SA}	—	4	t_{PAcyc}	Figure 5.51, Figure 5.52	
Slave output release time			t_{REL}	—	3	t_{PAcyc}		

Note 1. t_{PAcyc} : PCLKA cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups. For the RSPI interface, the AC portion of the electrical characteristics is measured for each group.

Table 5.35 QSPI Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Max.	Unit*1	Test Conditions*2
QSPI	QSPCLK clock cycle	t_{QScyc}	2	4080	t_{PBcyc} Figure 5.53
	Data input setup time	t_{Su}	6.5	—	ns Figure 5.54,
	Data input hold time	t_{IH}	5	—	ns Figure 5.55
	SS setup time	t_{LEAD}	1.5	8.5	t_{QScyc}
	SS hold time	t_{LAG}	1	8	t_{QScyc}
	Data output delay time	t_{OD}	—	10.0	ns
	Data output hold time	t_{OH}	—5	—	ns
	Successive transmission delay time	t_{TD}	1	8	t_{QScyc}

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. We recommend using pins that have a letter ("A", "B", etc.) to indicate group membership appended to their names as groups.
 For the QSPI interface, the AC portion of the electrical characteristics is measured for each group.

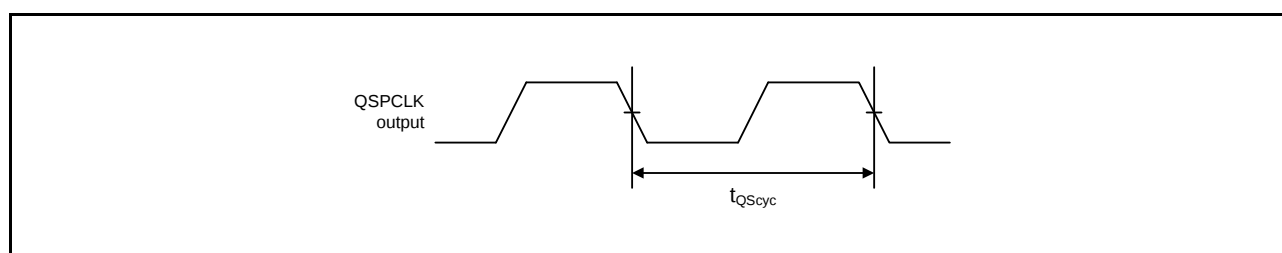
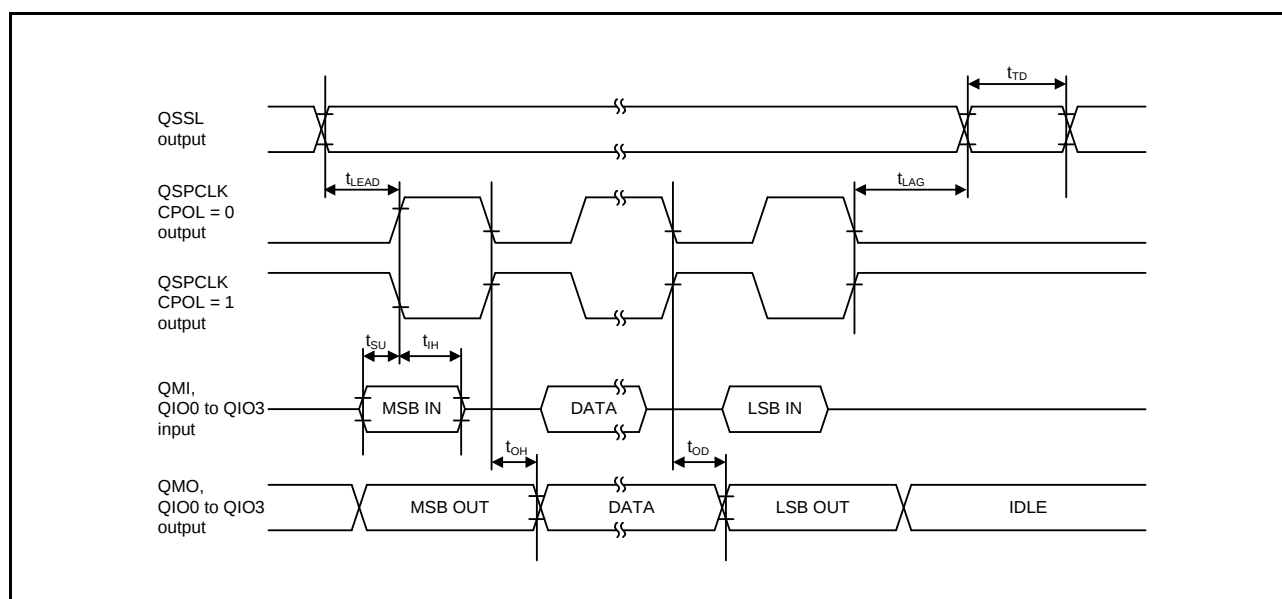
**Figure 5.53 QSPI Clock Timing****Figure 5.54 Transmit/Receive Timing (CPHA = 0)**

Table 5.41 PDC Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.*1	Max.	Unit	Test Conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	ns	Figure 5.72
	PIXCLK input high pulse width	t_{PIXH}	10	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	ns	
	PIXCLK rising time	t_{PIXr}	5	ns	
	PIXCLK falling time	t_{PIXf}	5	ns	
	PCKO output cycle time	t_{PCKcyc}	$2 \times t_{PBcyc}$	ns	Figure 5.73
	PCKO output high pulse width	t_{PCKH}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO output low pulse width	t_{PCKL}	$(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3$	ns	
	PCKO rising time	t_{PCKr}	5	ns	
	PCKO falling time	t_{PCKf}	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	ns	Figure 5.74
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	ns	
	PIXD input setup time	t_{PIXDS}	10	ns	
	PIXD input hold time	t_{PIXDH}	5	ns	

Note 1. t_{PBcyc} : PCLKB cycle

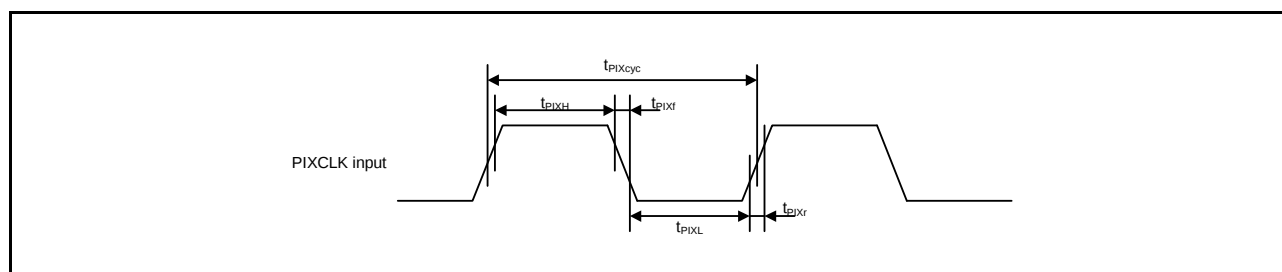
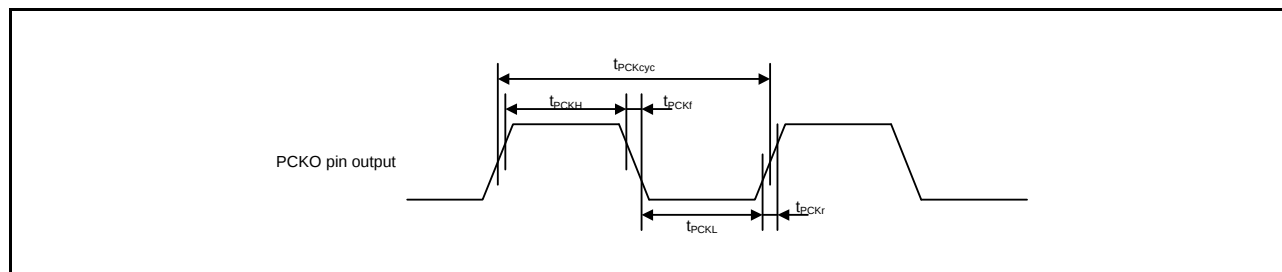
**Figure 5.72 PDC Input Clock Timing****Figure 5.73 PDC Output Clock Timing**

Table 5.44 Battery Charge Characteristics (USBA only)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA =$
 $AVSS_USBA = 0$ V, $USBA_RREF = 2.2$ k $\Omega \pm 1\%$, $USBMCLK = 20/24$ MHz, $PCLKA = 8$ to 120 MHz,
 $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
D+ sink current	I_{DP_SINK}	25	175	μA	
D- sink current	I_{DM_SINK}	25	175	μA	
DCD source current	I_{DP_SRC}	7	13	μA	
Data detection voltage	V_{DAT_REF}	0.25	0.4	V	
D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

5.5 A/D Conversion Characteristics

Table 5.45 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKB = PCLKC = 1$ MHz to 60 MHz, $T_a = T_{opr}$

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	1.06 (0.40 + 0.25) *2	—	—	μs	- Sampling of channel-dedicated sample-and-hold circuits in 24 states - Sampling in 15 states
	Offset error	—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error	—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0 - 0.25 V
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.5	±5.5	LSB	
	DNL differential nonlinearity error	—	±1.0	±2.0	LSB	
	INL integral nonlinearity error	—	±1.5	±3.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	20	μs	
	Dynamic range	0.25	—	VREFH 0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLK = 60 MHz) Permissible signal source impedance (max.) = 1.0 kΩ	0.48 (0.267) *2	—	—	μs	Sampling in 16 states
	Offset error	—	±1.0	±2.5	LSB	
	Full-scale error	—	±1.0	±2.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	±2.0	±4.5	LSB	
	DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
	INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

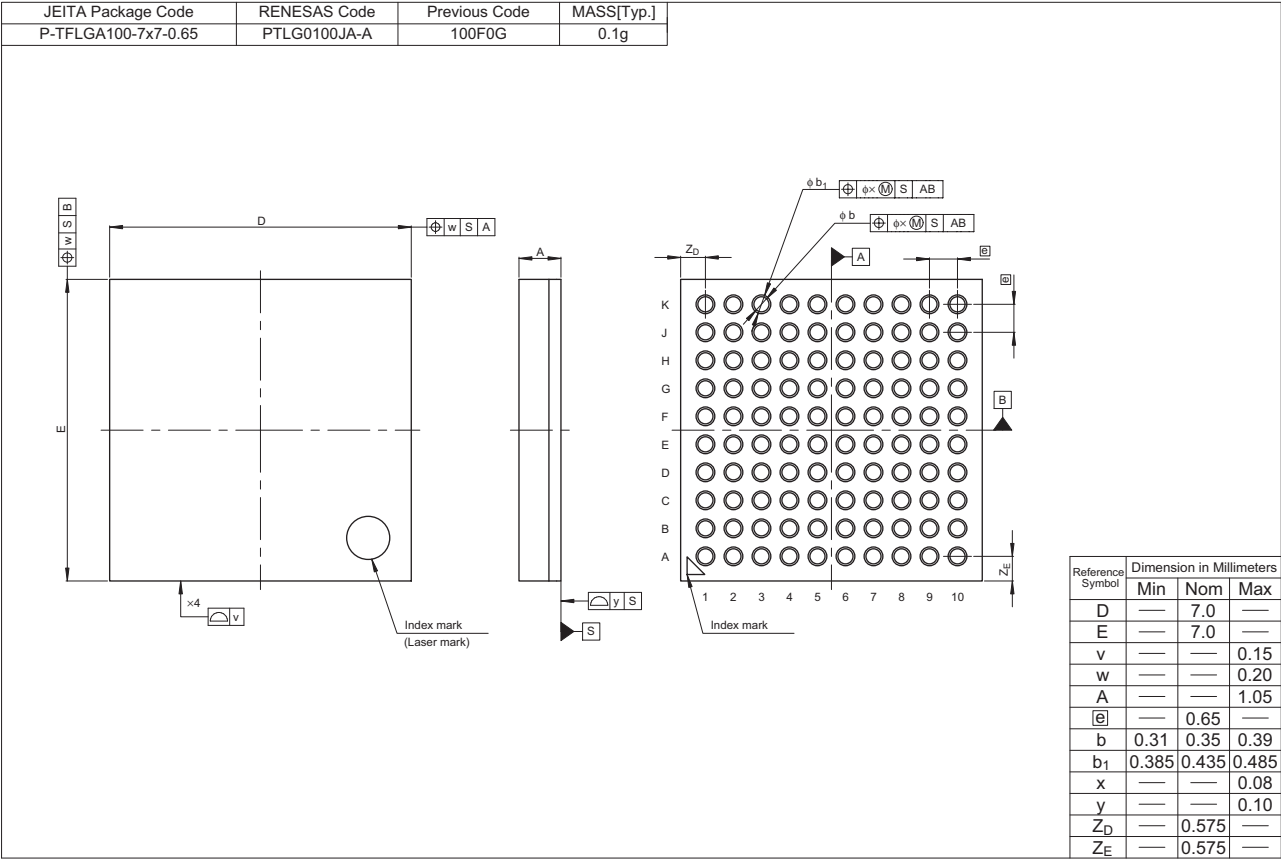


Figure F 100-Pin TFLGA (PTLG0100JA-A)

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Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141