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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2.5MB (2.5M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mghdfb-v1

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I ² C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

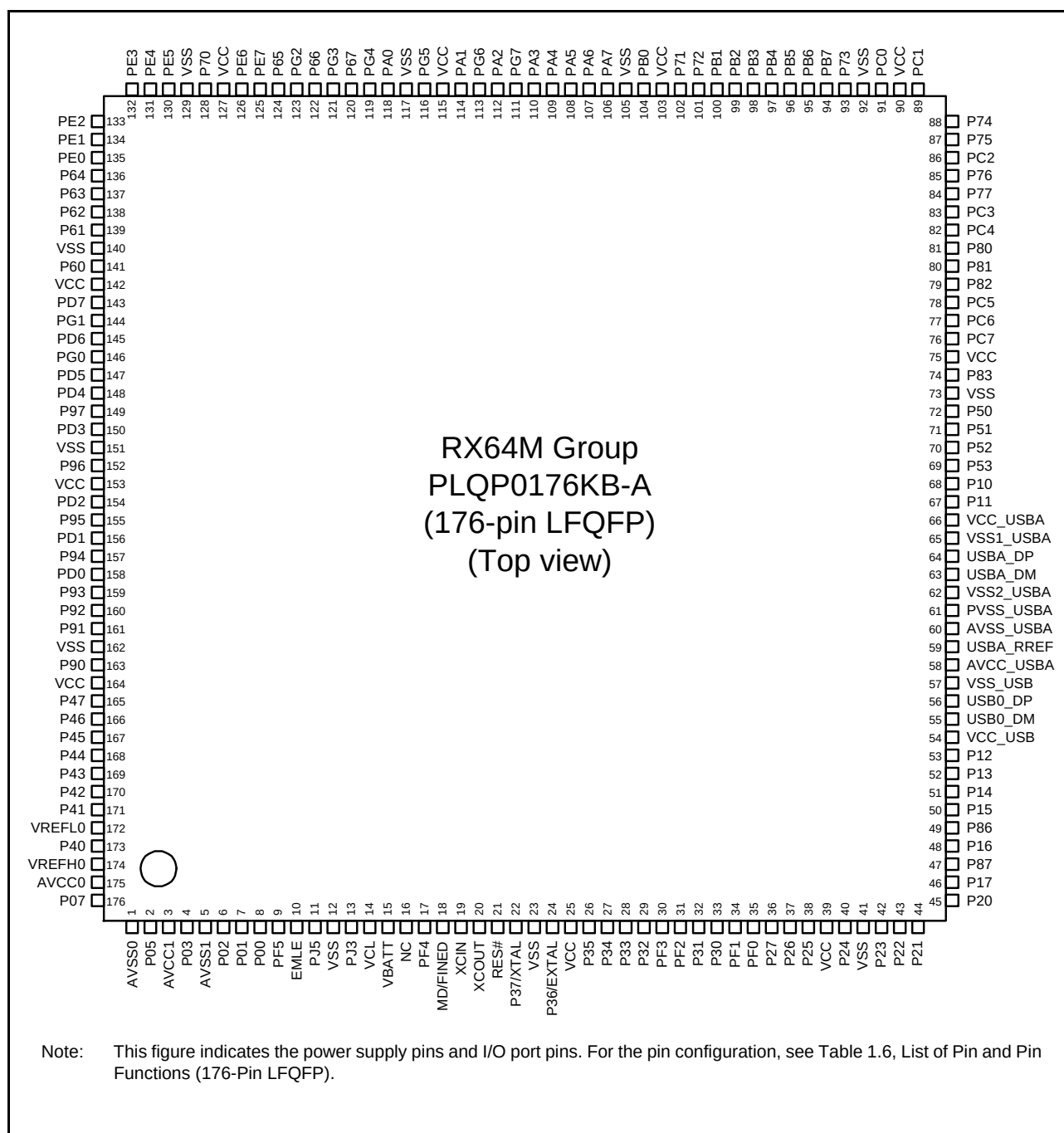


Figure 1.5 Pin Assignment (176-Pin LQFP)

RX64M Group											
PTLG0100JA-A (100-Pin TFLGA)											
(Upper Perspective View)											
	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

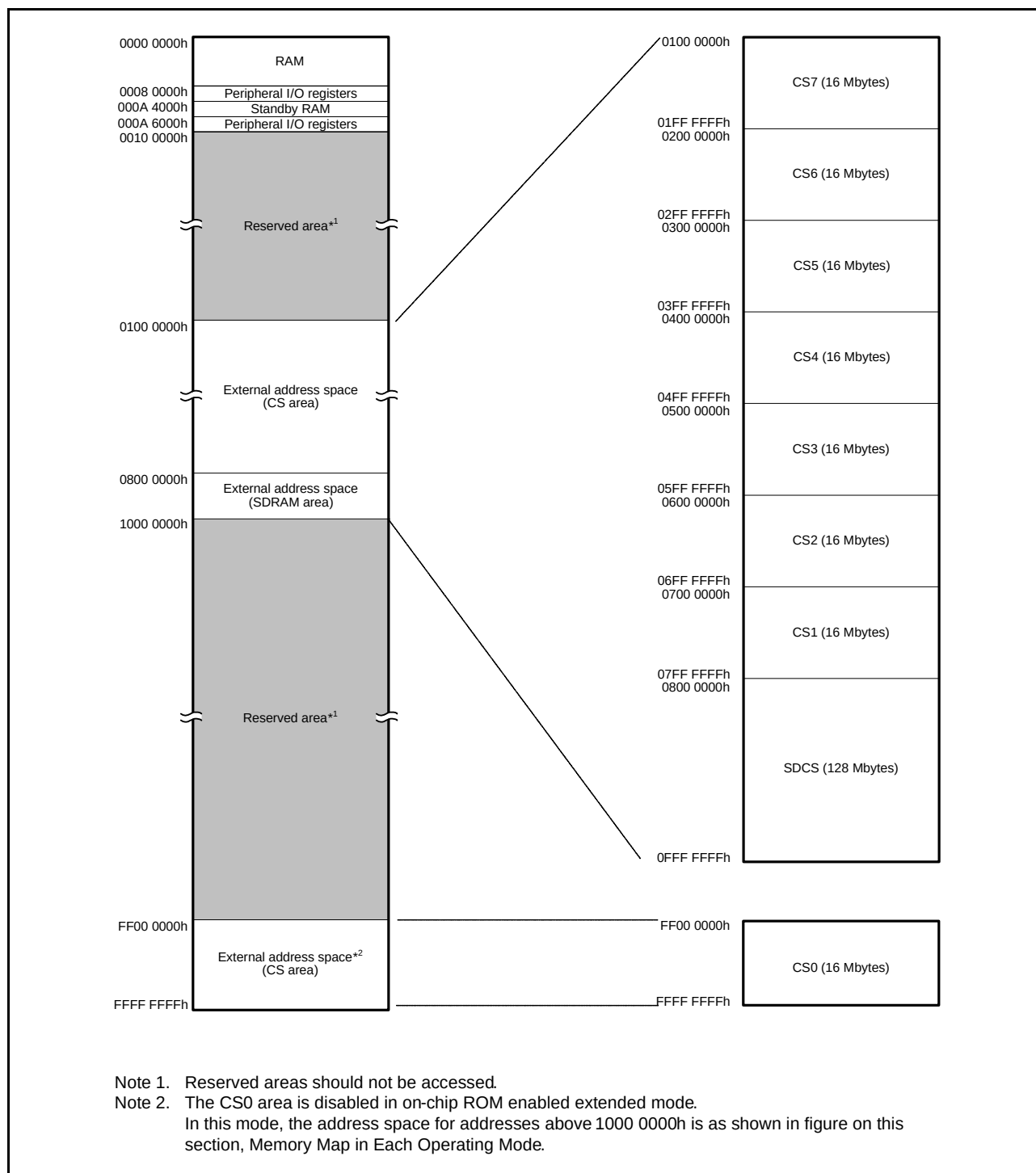
Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer	Communication	Memory Interface Camera Interface	Interrupt	S12ADC, R12DA
177-Pin TFLGA 176-Pin LFBGA				(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)		
E14	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
E15		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	VBATT							
F2	VCL							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
F4	BSCANP							
F12		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
F13	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
F14		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
F15	VSS							
G1	XCIN							
G2	XCOUT							
G3	MD/FINED							
G4	TRST#	PF4						
G12	TRCLK	PG5	D29		ET1_ETXD2			
G13	TRDATA2	PG6	D30		ET1_ETXD3			
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOC0B/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
G15	VCC							
H1	XTAL	P37						
H2	VSS							
H3	RES#							
H4	UPSEL	P35					NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
H14		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
H15	TRDATA3	PG7	D31		ET1_TX_ER			
J1	EXTAL	P36						
J2	VCC							
J3		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J4	TMS	PF3						
J12		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOC0B1/ PO21	RSPCKA-B/ ET0_LINKSTA			
J13	VSS							
J14		PA7	A7	TIOC0B2/PO23	MISOA-B/ ET0_WOL			

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (3 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETS	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		Buses
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		Buses
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK		DMACaA
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 201Fh	DMAC0	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 205Fh	DMAC1	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 209Fh	DMAC2	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA

Table 4.1 List of I/O Registers (Address Order) (4 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA

Table 4.1 List of I/O Registers (Address Order) (9 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7707h	ICU	Software Configurable Interrupt B Request Register 7	PIBR7	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7708h	ICU	Software Configurable Interrupt B Request Register 8	PIBR8	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7709h	ICU	Software Configurable Interrupt B Request Register 9	PIBR9	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 770Ah	ICU	Software Configurable Interrupt B Request Register A	PIBRA	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7780h	ICU	Software Configurable Interrupt B Source Select Register X128	SLIBXR128	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7781h	ICU	Software Configurable Interrupt B Source Select Register X129	SLIBXR129	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7782h	ICU	Software Configurable Interrupt B Source Select Register X130	SLIBXR130	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7783h	ICU	Software Configurable Interrupt B Source Select Register X131	SLIBXR131	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7784h	ICU	Software Configurable Interrupt B Source Select Register X132	SLIBXR132	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7785h	ICU	Software Configurable Interrupt B Source Select Register X133	SLIBXR133	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7786h	ICU	Software Configurable Interrupt B Source Select Register X134	SLIBXR134	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7787h	ICU	Software Configurable Interrupt B Source Select Register X135	SLIBXR135	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7788h	ICU	Software Configurable Interrupt B Source Select Register X136	SLIBXR136	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7789h	ICU	Software Configurable Interrupt B Source Select Register X137	SLIBXR137	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ah	ICU	Software Configurable Interrupt B Source Select Register X138	SLIBXR138	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Bh	ICU	Software Configurable Interrupt B Source Select Register X139	SLIBXR139	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Ch	ICU	Software Configurable Interrupt B Source Select Register X140	SLIBXR140	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Dh	ICU	Software Configurable Interrupt B Source Select Register X141	SLIBXR141	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Eh	ICU	Software Configurable Interrupt B Source Select Register X142	SLIBXR142	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 778Fh	ICU	Software Configurable Interrupt B Source Select Register X143	SLIBXR143	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7790h	ICU	Software Configurable Interrupt B Source Select Register 144	SLIBR144	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7791h	ICU	Software Configurable Interrupt B Source Select Register 145	SLIBR145	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7792h	ICU	Software Configurable Interrupt B Source Select Register 146	SLIBR146	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7793h	ICU	Software Configurable Interrupt B Source Select Register 147	SLIBR147	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7794h	ICU	Software Configurable Interrupt B Source Select Register 148	SLIBR148	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7795h	ICU	Software Configurable Interrupt B Source Select Register 149	SLIBR149	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7796h	ICU	Software Configurable Interrupt B Source Select Register 150	SLIBR150	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7797h	ICU	Software Configurable Interrupt B Source Select Register 151	SLIBR151	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7798h	ICU	Software Configurable Interrupt B Source Select Register 152	SLIBR152	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7799h	ICU	Software Configurable Interrupt B Source Select Register 153	SLIBR153	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Ah	ICU	Software Configurable Interrupt B Source Select Register 154	SLIBR154	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 779Bh	ICU	Software Configurable Interrupt B Source Select Register 155	SLIBR155	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (33 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C095h	PORTA	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C097h	PORTB	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C098h	PORTC	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C099h	PORTC	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Ah	PORTD	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Bh	PORTD	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Ch	PORTE	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Dh	PORTE	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Eh	PORTF	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C09Fh	PORTF	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A0h	PORTG	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A1h	PORTG	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A4h	PORTJ	Open-Drain Control Register 0	ODR0	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0A5h	PORTJ	Open-Drain Control Register 1	ODR1	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C0h	PORT0	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C1h	PORT1	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C2h	PORT2	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C3h	PORT3	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C4h	PORT4	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C5h	PORT5	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C6h	PORT6	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C7h	PORT7	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C8h	PORT8	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0C9h	PORT9	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CAh	PORTA	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CBh	PORTB	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CCh	PORTC	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CDh	PORTD	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CEh	PORTE	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C0CFh	PORTF	Pull-Up Resistor Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (43 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000A 0050h	USB0	USB Address Register	USBADDR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0070h	USB0	PIPE1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0072h	USB0	PIPE2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0074h	USB0	PIPE3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0076h	USB0	PIPE4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0078h	USB0	PIPE5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ah	USB0	PIPE6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Ch	USB0	PIPE7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 007Eh	USB0	PIPE8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0080h	USB0	PIPE9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*5}	USBb

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 4000h	EPTPC	MINT Interrupt Source Status Register	MIESR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4004h	EPTPC	MINT Interrupt Request Permission Register	MIEIPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4010h	EPTPC	ELC Output/IPLS Interrupt Request Permission Register	ELIPPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4014h	EPTPC	ELC Output/IPLS Interrupt Permission Automatic Clearing Register	ELIPACR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4040h	EPTPC	STCA Status Register	STSR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4044h	EPTPC	STCA Status Notification Permission Register	STIPR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4050h	EPTPC	STCA Clock Frequency Setting Register	STCFR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4054h	EPTPC	STCA Operating Mode Register	STMR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4058h	EPTPC	Sync Message Reception Timeout Register	SYNTOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4060h	EPTPC	IPLS Interrupt Request Timer Select Register	IPTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4064h	EPTPC	MINT Interrupt Request Timer Select Register	MITSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4068h	EPTPC	ELC Output Timer Select Register	ELTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 406Ch	EPTPC	Time Synchronization Channel Select Register	STCHSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4080h	EPTPC	Slave Time Synchronization Start Register	SYNSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4084h	EPTPC	Local Time Counter Initial Value Load Directive Register	LCIVLDR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4090h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4094h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4098h	EPTPC	Synchronization Detection Threshold Register	SYNTDBRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 409Ch	EPTPC	Synchronization Detection Threshold Register	SYNTDBRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B0h	EPTPC	Local Time Counter Initial Value Register	LCIVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B4h	EPTPC	Local Time Counter Initial Value Register	LCIVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B8h	EPTPC	Local Time Counter Initial Value Register	LCIVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4124h	EPTPC	Worst 10 Acquisition Directive Register	GETW10R	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4128h	EPTPC	Positive Gradient Limit Register	PLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 412Ch	EPTPC	Positive Gradient Limit Register	PLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4130h	EPTPC	Positive Gradient Limit Register	PLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4134h	EPTPC	Negative Gradient Limit Register	MLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC

Table 4.1 List of I/O Registers (Address Order) (56 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4138h	EPTPC	Negative Gradient Limit Register	MLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 413Ch	EPTPC	Negative Gradient Limit Register	MLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4140h	EPTPC	Statistical Information Retention Control Register	GETINFOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4170h	EPTPC	Local Time Counter	LCCVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4174h	EPTPC	Local Time Counter	LCCVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4178h	EPTPC	Local Time Counter	LCCVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4210h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4214h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4218h	EPTPC	Positive Gradient Worst 10 Value Register	PW10VRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 42D0h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 42D4h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 42D8h	EPTPC	Negative Gradient Worst 10 Value Register	MW10RL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4300h	EPTPC	Timer Start Time Setting Register	TMSTTRU0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4304h	EPTPC	Timer Start Time Setting Register	TMSTTRL0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4308h	EPTPC	Timer Cycle Setting Register 0	TMCYCR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 430Ch	EPTPC	Timer Pulse Width Setting Register 0	TMPLSR0	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4310h	EPTPC	Timer Start Time Setting Register	TMSTTRU1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4314h	EPTPC	Timer Start Time Setting Register	TMSTTRL1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4318h	EPTPC	Timer Cycle Setting Register 1	TMCYCR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 431Ch	EPTPC	Timer Pulse Width Setting Register 1	TMPLSR1	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4320h	EPTPC	Timer Start Time Setting Register	TMSTTRU2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4324h	EPTPC	Timer Start Time Setting Register	TMSTTRL2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4328h	EPTPC	Timer Cycle Setting Register 2	TMCYCR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 432Ch	EPTPC	Timer Pulse Width Setting Register 2	TMPLSR2	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4330h	EPTPC	Timer Start Time Setting Register	TMSTTRU3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4334h	EPTPC	Timer Start Time Setting Register	TMSTTRL3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4338h	EPTPC	Timer Cycle Setting Register 3	TMCYCR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 433Ch	EPTPC	Timer Pulse Width Setting Register 3	TMPLSR3	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4340h	EPTPC	Timer Start Time Setting Register	TMSTTRU4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4344h	EPTPC	Timer Start Time Setting Register	TMSTTRL4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4348h	EPTPC	Timer Cycle Setting Register 4	TMCYCR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 434Ch	EPTPC	Timer Pulse Width Setting Register 4	TMPLSR4	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4350h	EPTPC	Timer Start Time Setting Register	TMSTTRU5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4354h	EPTPC	Timer Start Time Setting Register	TMSTTRL5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4358h	EPTPC	Timer Cycle Setting Register 5	TMCYCR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 435Ch	EPTPC	Timer Pulse Width Setting Register 5	TMPLSR5	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 437Ch	EPTPC	Timer Start Register	TMSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4400h	EPTPC	PRC-TC Status Register	PRSR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4404h	EPTPC	PRC-TC Status Notification Permission Register	PRIPR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4410h	EPTPC	Channel 0 Local MAC Address Register	PRMACRU0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4414h	EPTPC	Channel 0 Local MAC Address Register	PRMACRL0	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4418h	EPTPC	Channel 1 Local MAC Address Register	PRMACRU1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 441Ch	EPTPC	Channel 1 Local MAC Address Register	PRMACRL1	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4420h	EPTPC	Packet Transmission Control Register	TRNDISR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4430h	EPTPC	Relay Mode Register	TRNMR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4434h	EPTPC	Cut-Through Transfer Start Threshold Register	TRNCTTDR	32	32	9, 10 PCLKA	2 to 5 ICLK	EPTPC
000C 4800h	EPTPC 0	SYNFP Status Register	SYSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4804h	EPTPC 0	SYNFP Status Notification Permission Register	SYIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC

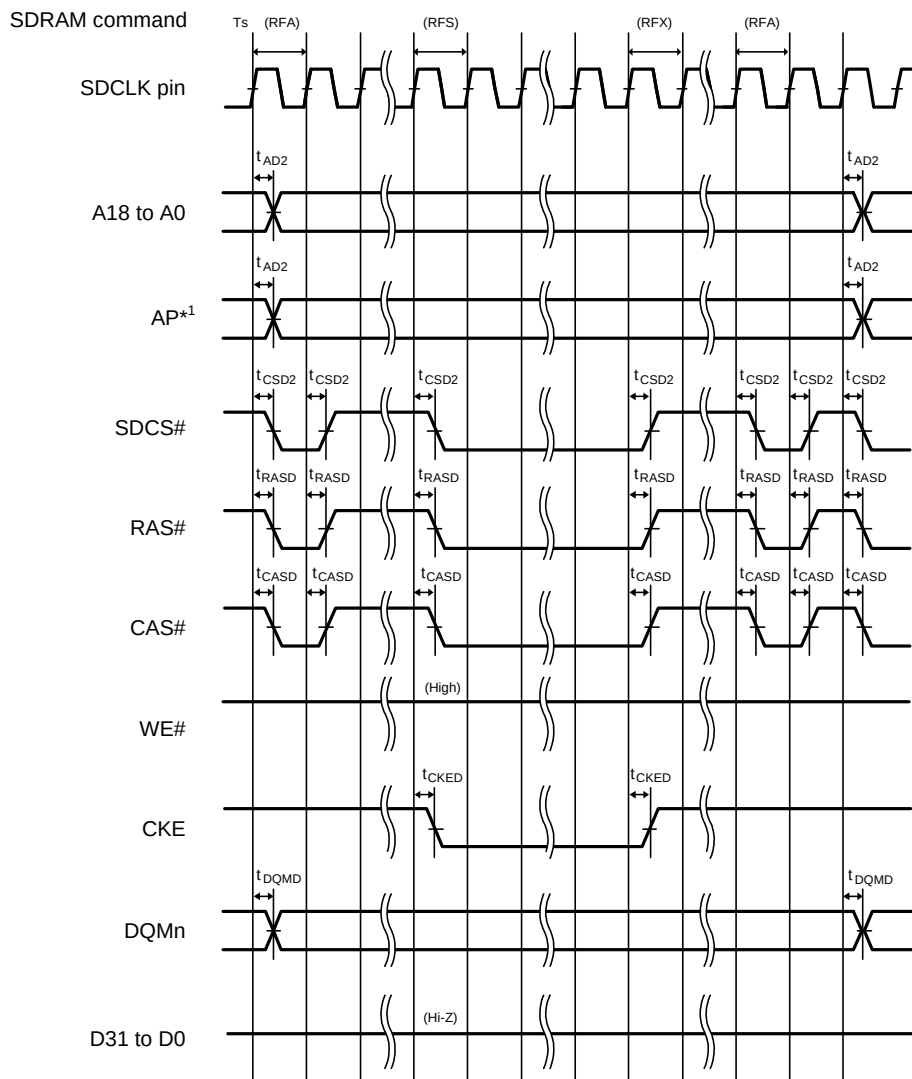


Figure 5.29 SDRAM Space Self-Refresh Bus Timing

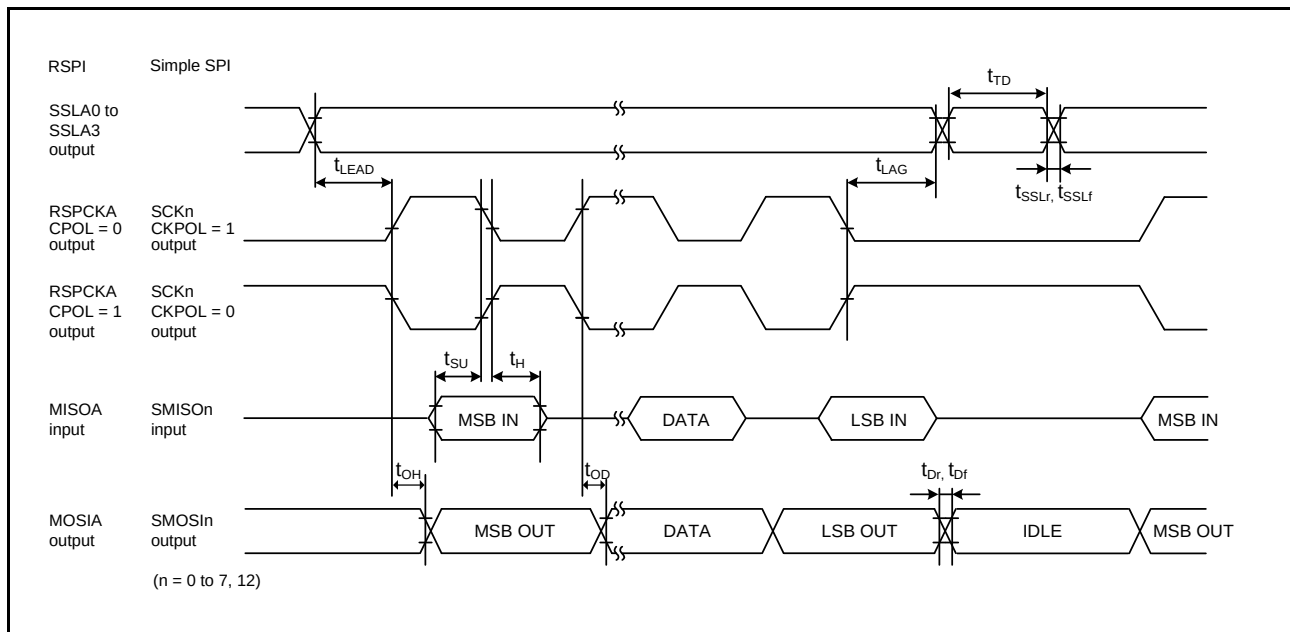


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

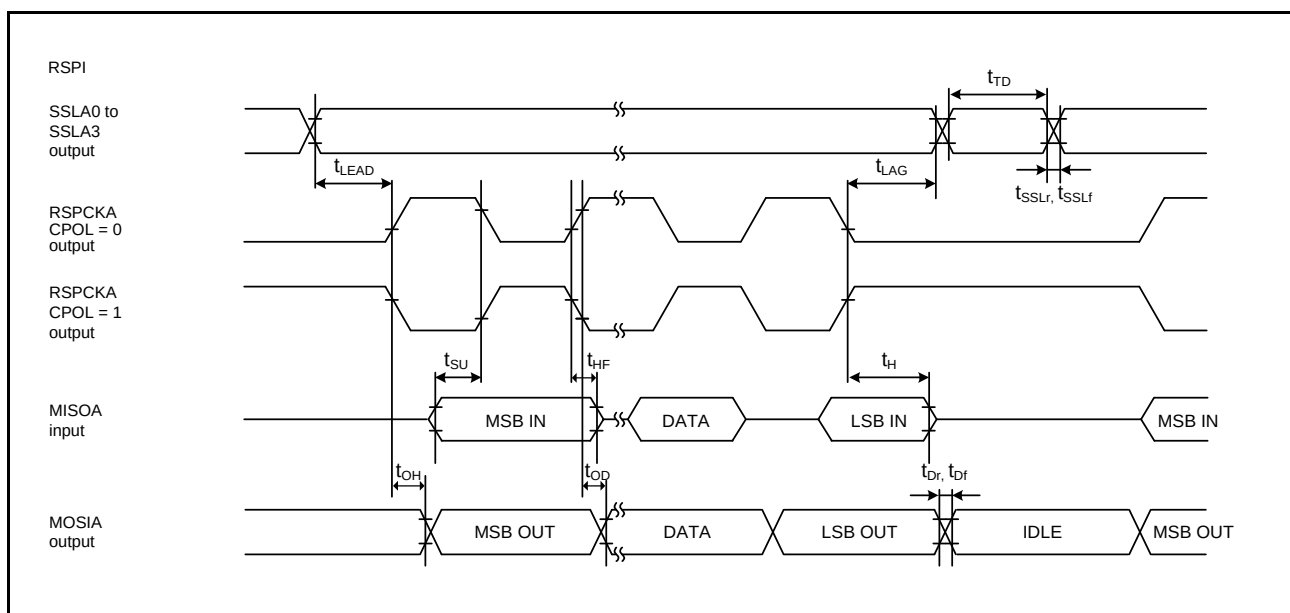


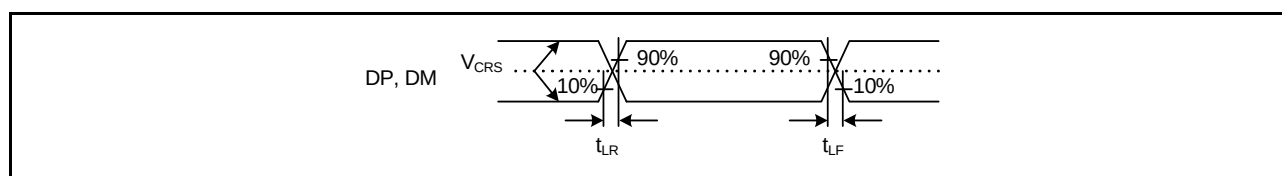
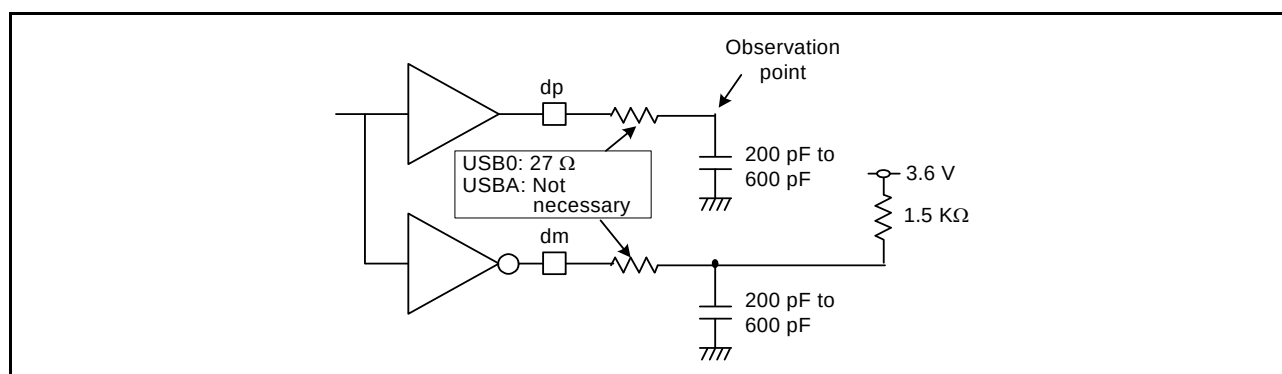
Figure 5.50 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

5.4 USB Characteristics

Table 5.42 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 3.0$ to 3.6 V, $3.0 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $USBA_RREF = 2.2$ k $\Omega \pm 1\%$, $USBMCLK = 20/24$ MHz, $UCLK = 48$ MHz,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$

	Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	DP – DM
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	$I_{OH} = -200$ μ A
	Output low level voltage	V_{OL}	0.0	—	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 5.75
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	k Ω	

**Figure 5.75 DP and DM Output Timing (Low Speed)****Figure 5.76 Test Circuit (Low Speed)**

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.50 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V _{POR}	2.5	2.6	2.7	V	Figure 5.79
		Low power consumption function enabled*2		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V _{det0_1}	2.84	2.94	3.04		Figure 5.80
			V _{det0_2}	2.77	2.87	2.97		
			V _{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V _{det1_1}	2.89	2.99	3.09		Figure 5.81
			V _{det1_2}	2.82	2.92	3.02		
			V _{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V _{det2_1}	2.89	2.99	3.09		Figure 5.82
			V _{det2_2}	2.82	2.92	3.02		
			V _{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.79
	LVD0 reset time		t _{LVD0}	—	0.70	—		Figure 5.80
	LVD1 reset time		t _{LVD1}	—	0.57	—		Figure 5.81
	LVD2 reset time		t _{LVD2}	—	0.57	—		Figure 5.82
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.79, Figure 5.80
Response delay time			t _{det}	—	—	200	μs	Figure 5.79 to Figure 5.82
LVD operation stabilization time (after LVD is enabled)*3			T _{d(E-A)}	—	—	10	μs	Figure 5.81, Figure 5.82
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 3. The voltage of $V_{CC} = AVCC0 = AVCC1$ when LVD1 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 1 level ($V_{det1_1, 2, 3}$) selected by the LVDLVLR.LVD1LVL[3:0] bits.

Similarly, the voltage of $V_{CC} = AVCC0 = AVCC1$ when LVD2 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 2 level ($V_{det2_1, 2, 3}$) selected by the LVDLVLR.LVD2LVL[3:0] bits.

Table 5.54 Data Flash Memory Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,
 Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	μs
	64 bytes	t_{DBC64}	—	—	280	—	—	100	μs
	2 Kbytes	t_{DBC2K}	—	—	6169	—	—	2200	μs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	—
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	μs
Forced stop command		t_{FD}	—	—	32	—	—	20	μs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	—

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 100000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

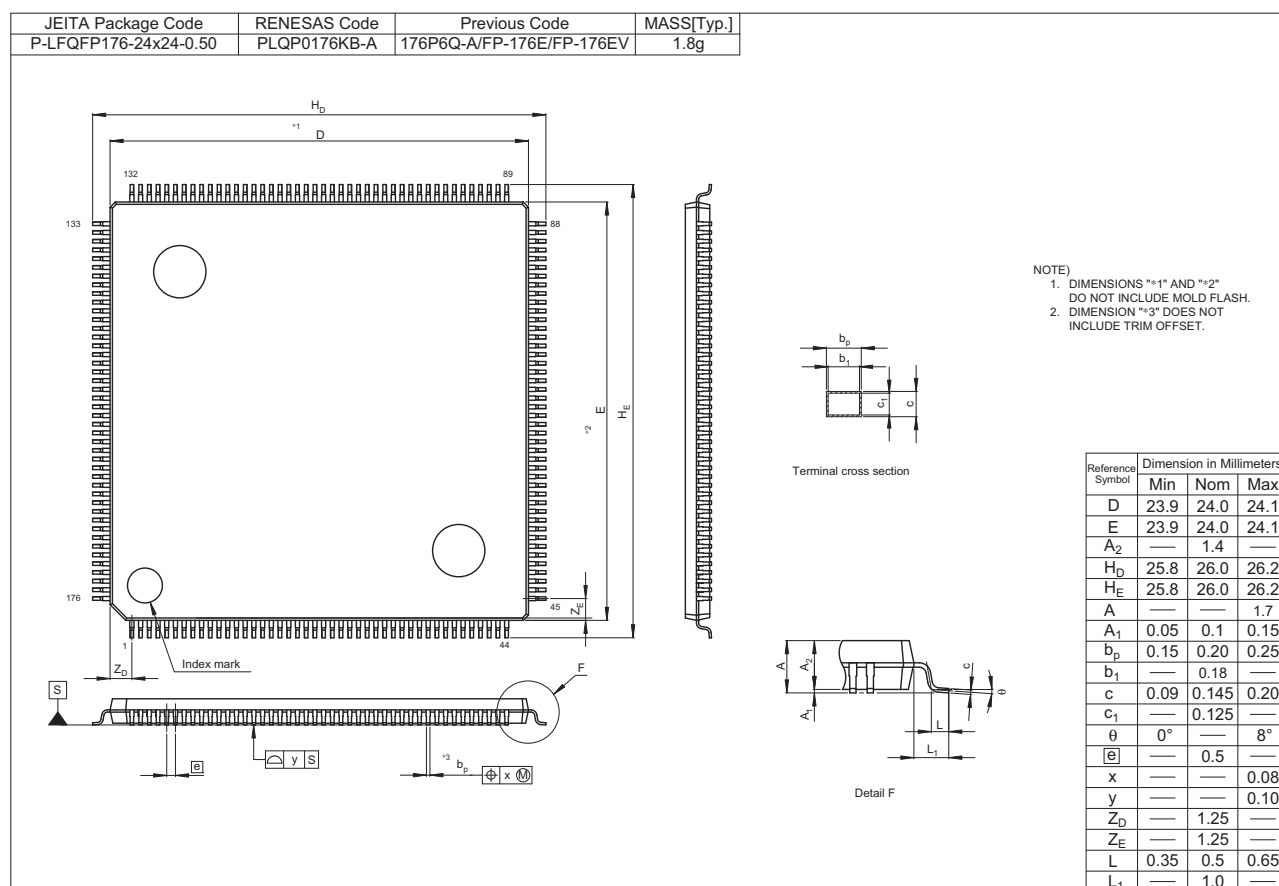


Figure C 176-Pin LFQFP (PLQP0176KB-A)

Figure D 145-Pin TFLGA (PTLG0145KA-A)

REVISION HISTORY	RX64M Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.90	Feb 28, 2014	—	First edition, issued
1.00	Jul 31, 2014	Summary	
		1	■ Data transfer, changed
		1. Overview	
		—	FINEC (Pin), deleted
		2	Table 1.1 Outline of Specifications (1/9), changed
		3	Table 1.1 Outline of Specifications (2/9), changed
		6	Table 1.1 Outline of Specifications (5/9), changed
		7	Table 1.1 Outline of Specifications (6/9), changed
		8	Table 1.1 Outline of Specifications (7/9), changed
		9	Table 1.1 Outline of Specifications (8/9), changed
		10	Table 1.1 Outline of Specifications (9/9), changed
		16	Figure 1.1 How to Read the Product Part Number, changed
		19	Table 1.4 Pin Functions (2/8), changed
		20	Table 1.4 Pin Functions (3/8), changed
		25	Table 1.4 Pin Functions (8/8), note added
		2. CPU, added	
		3. Address Space, added	
		4. I/O Registers, added	
		5. Electrical Characteristics, added	
		Appendix 1. Package Dimensions, added	

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.10	Oct 24, 2016	All	Terms unified: GPTa → GPTA LQFP → LFQFP	
		Features		
		1	AES key lengths, changed	TN-RX*-A122A/E
		1. Overview		
		2	Table 1.1 Outline of Specifications (1/9), changed	TN-RX*-A127A/E
		5	Table 1.1 Outline of Specifications (4/9), changed	
		10	Table 1.1 Outline of Specifications (9/9), changed	TN-RX*-A122A/E
		28	Figure 1.5 Pin Assignment (176-Pin LFQFP), changed	
		48	Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5), changed	
		49	Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5), changed	
		52	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (1/5), changed	
		55	Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (4/5), changed	
		58	Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4), changed	
		59	Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4), changed	
		63	Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/4), changed	
		4. I/O Registers		
		71	(4) Notes on Sleep Mode and Mode Transitions, added	
		73	Table 4.1 List of I/O Registers (Address Order) (2 / 67) 0008 1200h, 0008 1201h, 0008 1204h, 0008 1208h, added	TN-RX*-A127A/E