Renesas Electronics America Inc - R5F564MJGDFB#V1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mjgdfb-v1

Table 1.1 Outline of Specifications (6/9)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	• 2 channels • Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards • Filtering of multicast frames • Direct transfer of frames between two channels by cut-through
	PTP controller for Ethernet controller (EPTPC)	• A block compatible with the IEEE 1588 standard is connected to the Ethernet controller (ETHERC). • Matching with a time stamp can start counting by MTU3 and the GPT.
	DMA controller for Ethernet controller (EDMACa)	• 3 channels (the round-robin method determines the priority of the channels) 2 channels for ETHERC; 1 channel for EPTPC • Alleviation of CPU load by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 4 Kbytes
	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	USB 2.0 FS host/ function module with battery charging (USBA)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port (only in 176-pin devices) • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-power mode and bus power are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 8.5 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Serial communications interfaces (SCIg, SCIh)	• 9 channels (SCIg: 8 channels + SCIh: 1 channel) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	Serial communications interface with FIFO (SCIFA)	• 4 channels • Methods of transfer: Asynchronous and clock synchronous • Desired bit rates can be selected from the internal baud rate generators. • LSB or MSB first is selectable. • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation • Double-speed mode

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Encryption function	AES*3	• Key lengths: 128, 192, and 256 bits • Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	DES*3	• Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) • Support for DES and triple DES • Support for ECB and CBC operating modes • Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode • Compliant with FIPS PUB 46-3 • Compliant with FIPS PUB 81
	SHA*3	• Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) • Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode • Compliant with SHA as defined in FIPS PUB 180-1 and -2 • Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)*3	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 2.7 to 3.6 V, V_{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C (in planning)
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.
Note 3. The product part number differs according to whether or not it supports encryption.
Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

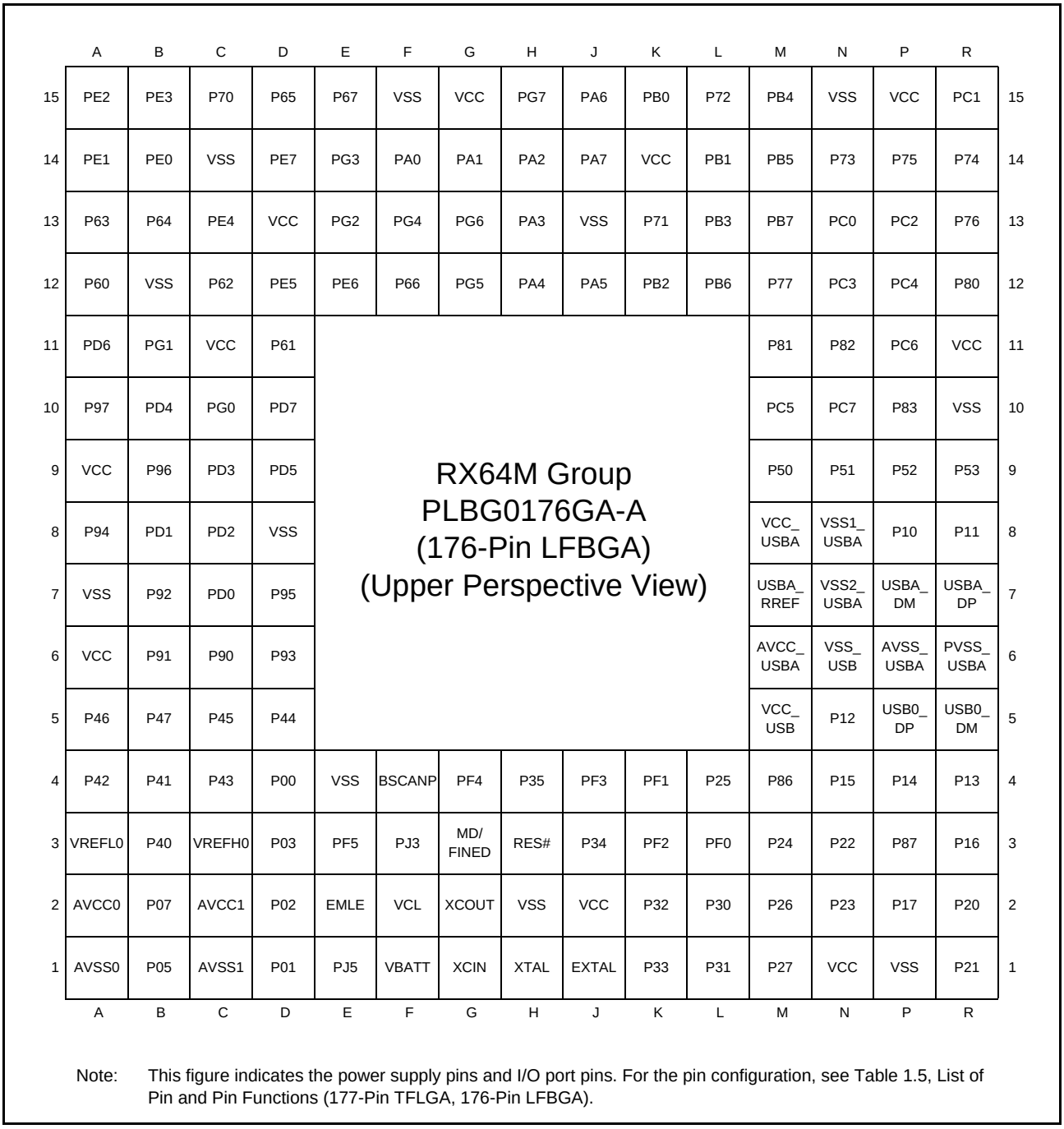
Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX64M	R5F564MLCDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDFC	PLQP0176KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDFC	PLQP0176KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDFC	PLQP0176KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDFC	PLQP0176KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDFB	PLQP0144KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDFB	PLQP0144KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDFB	PLQP0144KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDFB	PLQP0144KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDFP	PLQP0100KB-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDFP	PLQP0100KB-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDFP	PLQP0100KB-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
	UB	Input	USB boot mode or user boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-power mode and the high level selects bus power mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								VCC_ USBA	VSS1_ USBA	P10	P11	8
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USBA	USBA_ DM	USBA_ DP	7
6	VCC	P91	P90	P93								AVCC_ USBA	VSS_ USB	AVSS_ USBA	PVSS_ USBA	6
5	P46	P47	P45	P44								VCC_ USB	P12	USB0_ DP	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
E14	TRDATA1	PG3	D27		ET1_ETXD0/ RMII1_TXD0			
E15		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	VBATT							
F2	VCL							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
F4	BSCANP							
F12		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
F13	TRSYNC	PG4	D28		ET1_ETXD1/ RMII1_TXD1			
F14		PA0	A0/BC0#/ DQM2	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
F15	VSS							
G1	XCIN							
G2	XCOUT							
G3	MD/FINED							
G4	TRST#	PF4						
G12	TRCLK	PG5	D29		ET1_ETXD2			
G13	TRDATA2	PG6	D30		ET1_ETXD3			
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOCB0/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
G15	VCC							
H1	XTAL	P37						
H2	VSS							
H3	RES#							
H4	UPSEL	P35					NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	
H14		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
H15	TRDATA3	PG7	D31		ET1_TX_ER			
J1	EXTAL	P36						
J2	VCC							
J3		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J4	TMS	PF3						
J12		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
J13	VSS							
J14		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (4/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
85		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
86		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
87		P75	CS5#	PO20	SCK11/RTS11#/ ET0_ERXD0/ RMII0_RXD0	MMC_RES#-A/ SDHI_D2-A		
88		P74	A20/CS4#	PO19	CTS11#/ET0_ERXD1/ RMII0_RXD1			
89		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
90	VCC							
91		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
92	VSS							
93		P73	CS3#	PO16	ET0_WOL			
94		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
95		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
97		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
99		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
101		P72	A19/CS2#		ET0_MDC			
102		P71	A18/CS1#		ET0_MDIO			
103	VCC							
104		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
105	VSS							
106		PA7	A7	TIOCB2/PO23	MISOA-B/ ET0_WOL			
107		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
108		PA5	A5	MTIOC6B/ GTIOC0A-C/TIOCB1/ PO21	RSPCKA-B/ ET0_LINKSTA			
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ ET0_MDIO		IRQ6-DS	

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (3/5)

Pin Number 145-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F13		PA2	A2	MTIOC7A/ GTIOC1A-C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
G1	XTAL	P37						
G2	RES							
G3	MD/FINED							
G4	BSCANP							
G10		PA5	A5	MTIOC6B/TIOCB1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
G11		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
G12	VCC							
G13		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
H1	EXTAL	P36						
H2	VCC							
H3	VSS							
H4	UPSEL	P35					NMI	
H10		P72	A19/CS2#		ET0_MDC			
H11		P71	A18/CS1#		ET0_MDIO			
H12		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
J1	TRST#	P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
J2		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/SSCL1		IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
J11		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
J12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
K1	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1			
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1			
K3	TMS	P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/SS1#		IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	

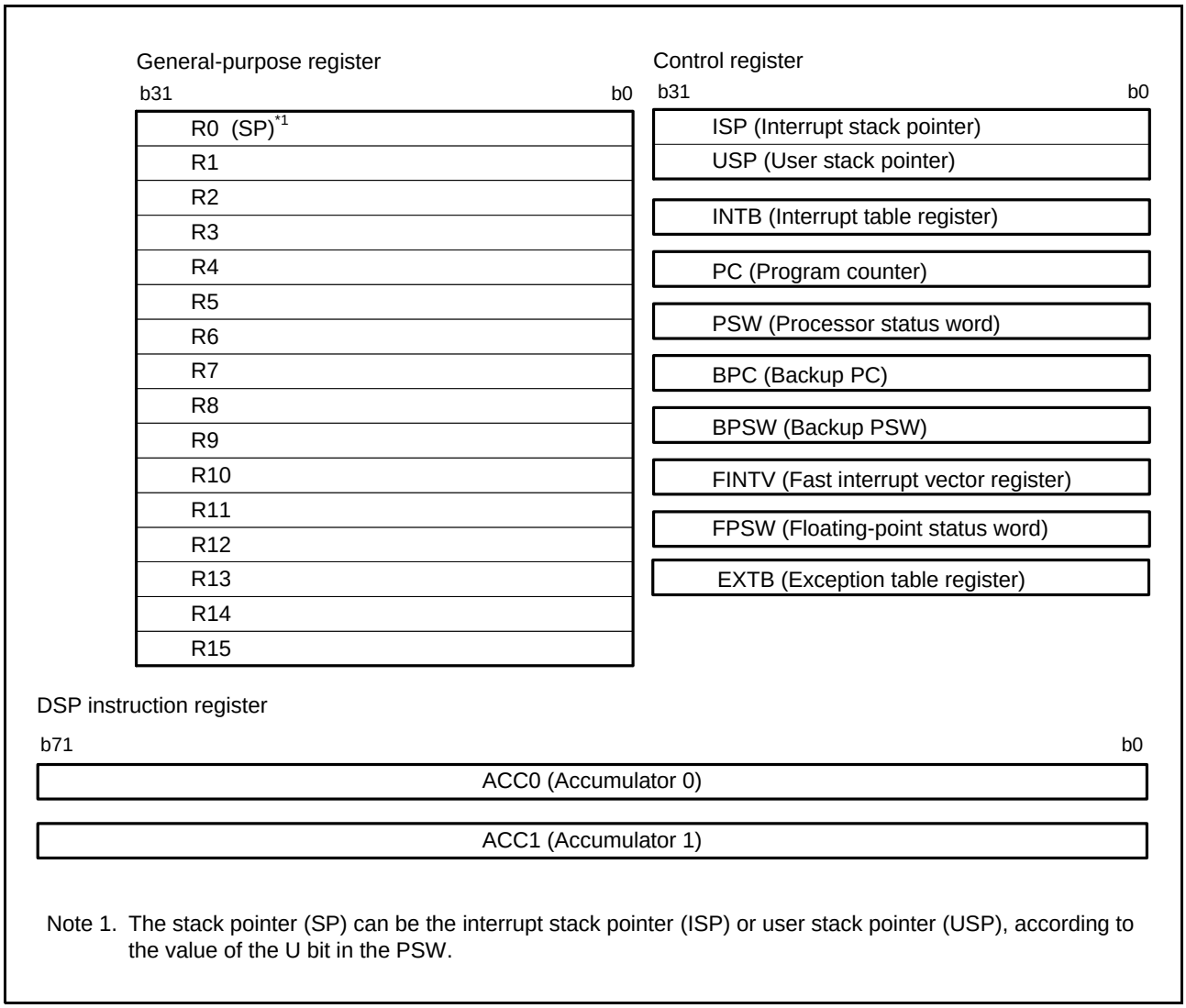
Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/4)

Pin Number 100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
81		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
86		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
87		P47					IRQ15-DS	AN007
88		P46					IRQ14-DS	AN006
89		P45					IRQ13-DS	AN005
90		P44					IRQ12-DS	AN004
91		P43					IRQ11-DS	AN003
92		P42					IRQ10-DS	AN002
93		P41					IRQ9-DS	AN001
94	VREFL0							
95		P40					IRQ8-DS	AN000
96	VREFH0							
97	AVCC0							
98		P07					IRQ15	ADTRG0#
99	AVSS0							
100	P05						IRQ13	DA1

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

2. CPU

Figure 2.1 shows register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK		Operating Modes
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK		Operating Modes
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK		Operating Modes
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK		Low Power Consumption
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK		Low Power Consumption
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK		Low Power Consumption
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK		Low Power Consumption
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit
0008 0024h	SYSTEM	System Clock Control Register 2	SCKCR2	16	16	3 ICLK		Clock Generation Circuit
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK		Clock Generation Circuit
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK		Clock Generation Circuit
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK		Clock Generation Circuit
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK		Clock Generation Circuit
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK		Clock Generation Circuit
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK		Clock Generation Circuit

Table 4.1 List of I/O Registers (Address Order) (16 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8208h	TMR01	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8209h	TMR1	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ah	TMR01	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 820Dh	TMR1	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 8219h	TMR3	Timer Counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2, 3 PCLKB	2 ICLK	TMR
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 821Dh	TMR3	Timer Counter Start Register	TCSTR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	CRC
0008 8300h	RIIC0	I^2C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8301h	RIIC0	I^2C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8302h	RIIC0	I^2C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8303h	RIIC0	I^2C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8304h	RIIC0	I^2C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8305h	RIIC0	I^2C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8306h	RIIC0	I^2C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8307h	RIIC0	I^2C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8308h	RIIC0	I^2C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8309h	RIIC0	I^2C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa

Table 4.1 List of I/O Registers (Address Order) (37 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C282h	SYSTEM	Deep Standby Interrupt Enable Register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C283h	SYSTEM	Deep Standby Interrupt Enable Register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C284h	SYSTEM	Deep Standby Interrupt Enable Register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C285h	SYSTEM	Deep Standby Interrupt Enable Register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C286h	SYSTEM	Deep Standby Interrupt Flag Register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C287h	SYSTEM	Deep Standby Interrupt Flag Register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C288h	SYSTEM	Deep Standby Interrupt Flag Register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C289h	SYSTEM	Deep Standby Interrupt Flag Register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ah	SYSTEM	Deep Standby Interrupt Edge Register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Bh	SYSTEM	Deep Standby Interrupt Edge Register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Ch	SYSTEM	Deep Standby Interrupt Edge Register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C28Dh	SYSTEM	Deep Standby Interrupt Edge Register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-Speed On-Chip Oscillator Power Supply Control Register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C296h	FLASH	Flash P/E Protect Register	FWEPROR	8	8	2 ICLK		Flash
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA

Table 4.1 List of I/O Registers (Address Order) (60 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4D20h	EPTPC1	PTP-primary Message Destination IP Address Setting Register	PPIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D24h	EPTPC1	PTP-pdelay Message Destination IP Address Setting Register	PDIPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D28h	EPTPC1	PTP event Message TOS Setting Register	PETOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D2Ch	EPTPC1	PTP general Message TOS Setting Register	PGTOSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D30h	EPTPC1	PTP-primary Message TTL Setting Register	PPTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D34h	EPTPC1	PTP-pdelay Message TTL Setting Register	PDTTLR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D38h	EPTPC1	PTP event Message UDP Destination Port Number Setting Register	PEUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D3Ch	EPTPC1	PTP general Message UDP Destination Port Number Setting Register	PGUDPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D40h	EPTPC1	Frame Reception Filter Setting Register	FFLTR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D60h	EPTPC1	Frame Reception Filter MAC Address 0 Setting Registers	FMAC0RU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D64h	EPTPC1	Frame Reception Filter MAC Address 0 Setting Registers	FMAC0RL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D68h	EPTPC1	Frame Reception Filter MAC Address 1 Setting Registers	FMAC1RU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D6Ch	EPTPC1	Frame Reception Filter MAC Address 1 Setting Registers	FMAC1RL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC0h	EPTPC1	Asymmetric Delay Setting Register	DASYMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC4h	EPTPC1	Asymmetric Delay Setting Register	DASYMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DC8h	EPTPC1	Timestamp Latency Setting Register	TSLATR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DCCh	EPTPC1	SYNFP Operation Setting Register	SYCONFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DD0h	EPTPC1	SYNFP Frame Format Setting Register	SYFORMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4DD4h	EPTPC1	Response Message Reception Timeout Register	RSTOUTR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000D 0000h	SCIFA8	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0002h	SCIFA8	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0004h	SCIFA8	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0006h	SCIFA8	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0008h	SCIFA8	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ah	SCIFA8	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Ch	SCIFA8	FIFO Control Register	FCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 000Eh	SCIFA8	FIFO Data Count Register	FDR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0010h	SCIFA8	Serial Port Register	SPTR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0012h	SCIFA8	Line Status Register	LSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0014h	SCIFA8	Serial Extended Mode Register	SEMR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0016h	SCIFA8	FIFO Trigger Control Register	FTCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0020h	SCIFA9	Serial Mode Register	SMR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Bit Rate Register	BRR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0022h	SCIFA9	Modulation Duty Register	MDDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0024h	SCIFA9	Serial Control Register	SCR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 0026h	SCIFA9	Transmit FIFO Data Register	FTDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA
000D 0028h	SCIFA9	Serial Status Register	FSR	16	16	3, 4 PCLKB	2 ICLK	SCIFA
000D 002Ah	SCIFA9	Receive FIFO Data Register	FRDR	8	8	3, 4 PCLKB	2 ICLK	SCIFA

Table 5.5 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog power supply current*1	During 12-bit A/D conversion (unit 0)		AI_{CC}	—	0.7	1.0	mA	IAVCC0_AD
	During 12-bit A/D conversion (unit 0) with the channel-dedicated sample-and-hold circuits for 3 channels operating			—	1.7	2.5	mA	IAVCC0_AD+SH
	During 12-bit A/D conversion (unit 1)			—	0.6	1.0	mA	IAVCC1_AD
	During 12-bit A/D conversion (unit 1) with the temperature sensor operating			—	0.7	1.1	mA	IAVCC1_AD+TEMP
	During D/A conversion (per unit)	Without AMP output		—	0.24	0.4	mA	IAVCC1_DA
		With AMP output		—	0.4	0.7	mA	
	Waiting for A/D, D/A, or temperature sensor conversion (all units)			—	0.9	1.4	mA	IAVCC0 + IAVCC1
	A/D, D/A converter, temperature sensor in standby mode (all units)			—	1.3	3.0	µA	IAVCC0 + IAVCC1
Reference power supply current	During 12-bit A/D conversion (unit 0)		AI_{REFH}	—	70	120	µA	IVREFH0
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.4	µA	IVREFH0
	12-bit A/D converter in standby mode (unit 0)			—	0.07	0.2	µA	IVREFH0
USB operating current	Low speed	USB0	$I_{CCUSBLS}$	—	3.5	6.5	mA	VCC_USB
		USBA		—	8.5	12.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	2.8	3.6	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	Full speed	USB0	$I_{CCUSBFS}$	—	4.0	10.0	mA	VCC_USB
		USBA		—	12.0	20.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 0)
		USBA		—	6.5	13.0	mA	VCC_USBA = AVCC_USBA (PHYSET.HSEB = 1)
	Standby mode (direct power down)	USBA	$I_{CCUSBSBY}$	—	0.1	3.0	µA	VCC_USBA = AVCC_USBA
RAM standby voltage			V_{RAM}	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	µs/V	
VCC falling gradient*2			SfVCC	8.4	—	—	µs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D conversion (unit 1) and D/A conversion.

Note 2. This applies when V_{BATT} is used.

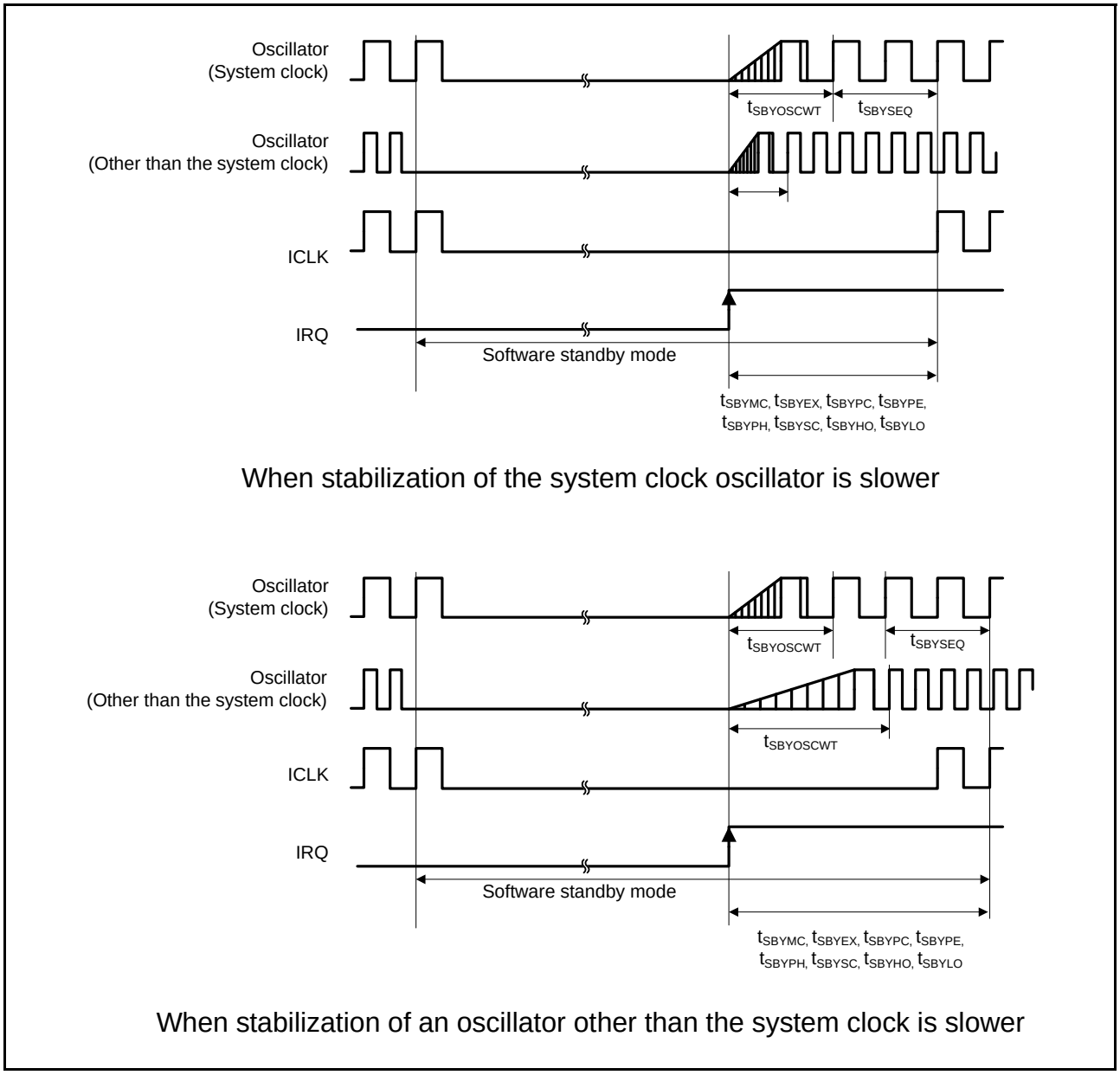


Figure 5.12 Software Standby Mode Cancellation Timing

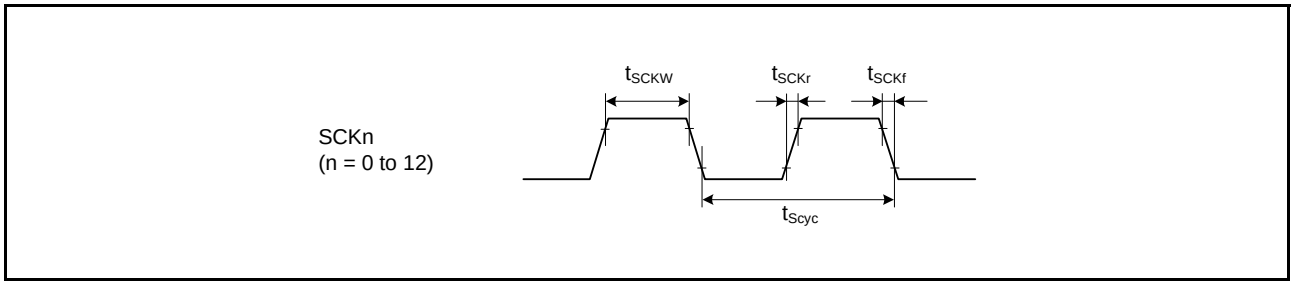


Figure 5.44 SCK Clock Input Timing

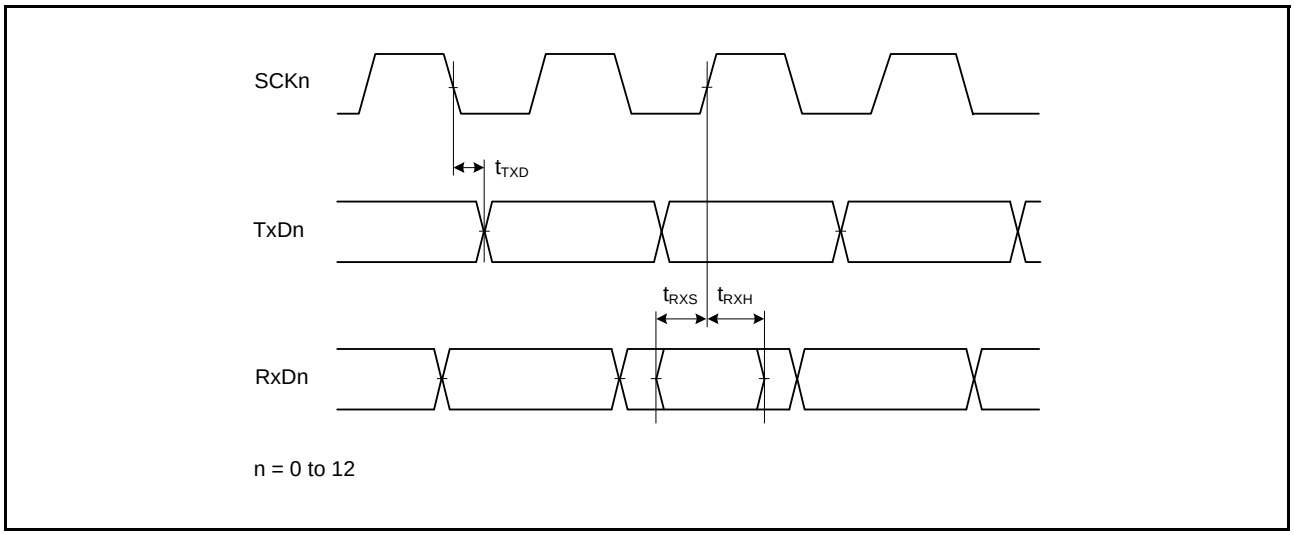


Figure 5.45 SCI Input/Output Timing: Clock Synchronous Mode

Table 5.40 ETHERC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	—	ns	Figure 5.62 to Figure 5.64
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100 ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII_xxxx*1 output delay time	T_{co}	2.5	15.0	ns	
	RMII_xxxx*2 setup time	T_{su}	3	—	ns	
	RMII_xxxx*2 hold time	T_{hd}	1	—	ns	
	RMII_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	5	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.66
ETHERC (MII)	ET_TX_CLK cycle time	t_{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t_{TENd}	1	20	ns	Figure 5.67
	ET_ETXD0 to ET_ETXD3 output delay time	t_{MTDd}	1	20	ns	
	ET_CRS setup time	t_{CRSs}	10	—	ns	
	ET_CRS hold time	t_{CRSh}	10	—	ns	
	ET_COL setup time	t_{COLs}	10	—	ns	Figure 5.68
	ET_COL hold time	t_{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t_{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t_{RDVs}	10	—	ns	Figure 5.69
	ET_RX_DV hold time	t_{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t_{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t_{MRDh}	10	—	ns	
	ET_RX_ER setup time	t_{RERs}	10	—	ns	Figure 5.70
	ET_RX_ER hold time	t_{RESh}	10	—	ns	
	ET_WOL output delay time	t_{WOLd}	1	23.5	ns	Figure 5.71

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

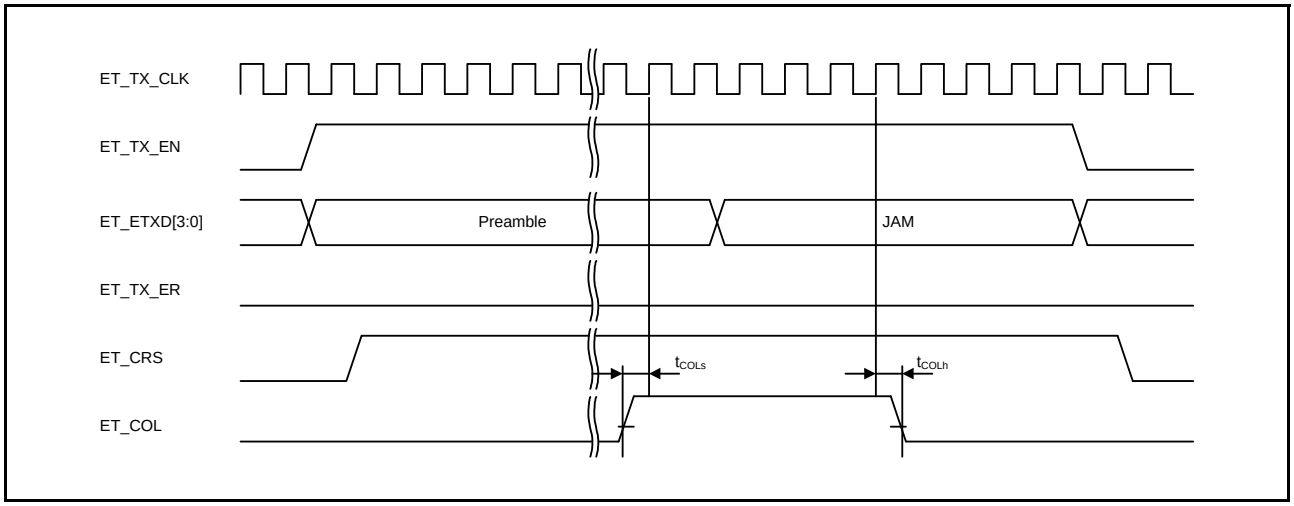


Figure 5.68 MII Transmission Timing (Conflict Occurrence)

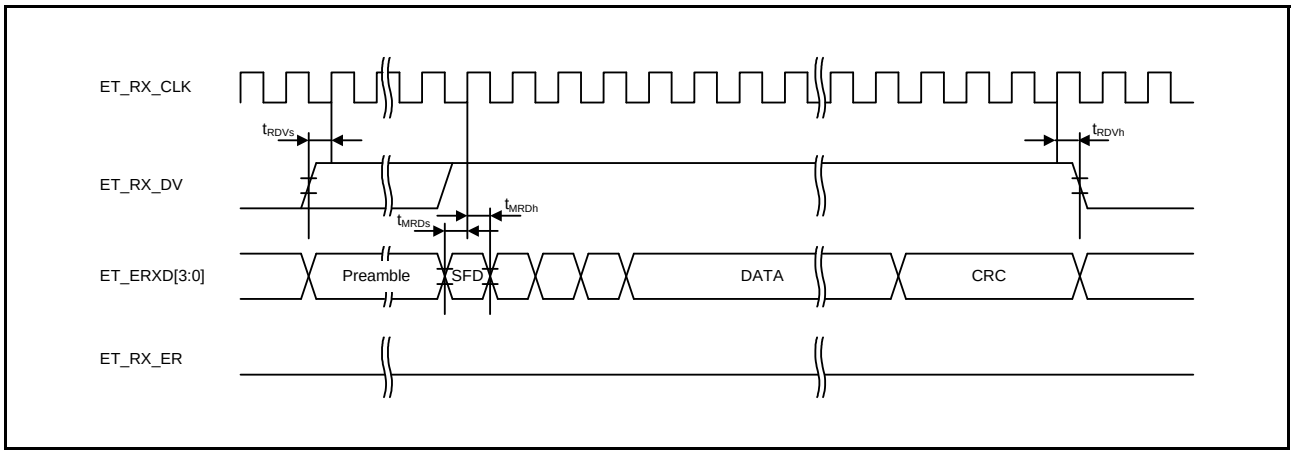


Figure 5.69 MII Reception Timing (Normal Operation)

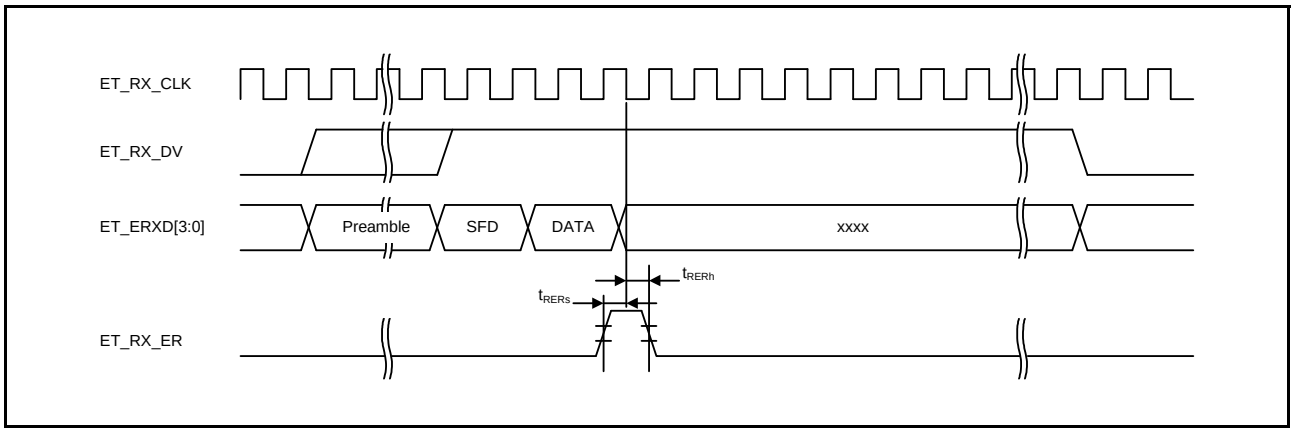


Figure 5.70 MII Reception Timing (Error Occurrence)

Table 5.44 Battery Charge Characteristics (USBA only)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
D+ sink current	I_{DP_SINK}	25	175	μA	
D- sink current	I_{DM_SINK}	25	175	μA	
DCD source current	I_{DP_SRC}	7	13	μA	
Data detection voltage	V_{DAT_REF}	0.25	0.4	V	
D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA