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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlcdfb-31

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Encryption function	AES*3	• Key lengths: 128, 192, and 256 bits • Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	DES*3	• Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) • Support for DES and triple DES • Support for ECB and CBC operating modes • Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode • Compliant with FIPS PUB 46-3 • Compliant with FIPS PUB 81
	SHA*3	• Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) • Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode • Compliant with SHA as defined in FIPS PUB 180-1 and -2 • Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)*3	• Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$, VCC_USBA = AVCC_USBA = 2.7 to 3.6 V, VBATT = 2.0 to 3.6 V
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C (in planning)
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LFQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LFQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) 100-pin LFQFP (PLQP0100KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX64M Group		
Package	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	RXD0 to RXD7	Input	Input pins for received data
	TXD0 to TXD7	Output	Output pins for transmitted data
	CTS0# to CTS7#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS7#	Output	Output pins for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL0 to SSCL7	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA7	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK0 to SCK7	I/O	Input/output pins for the clock
	SMISO0 to SMISO7	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI7	I/O	Input/output pins for master transmission of data
	SS0# to SS7#	Input	Chip-select input pins
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock
	SSDA12	I/O	Input/output pin for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface with FIFO (SCIFA)	SCK8 to SCK11	I/O	Input/output pins for the clock
	RXD8 to RXD11	Input	Input pins for received data
	TXD8 to TXD11	Output	Output pins for transmitted data
	CTS8# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS8# to RTS11#	Output	Output pins for controlling the start of transmission and reception
I ² C bus interface	SCL0[FM+], SCL2	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA2	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain

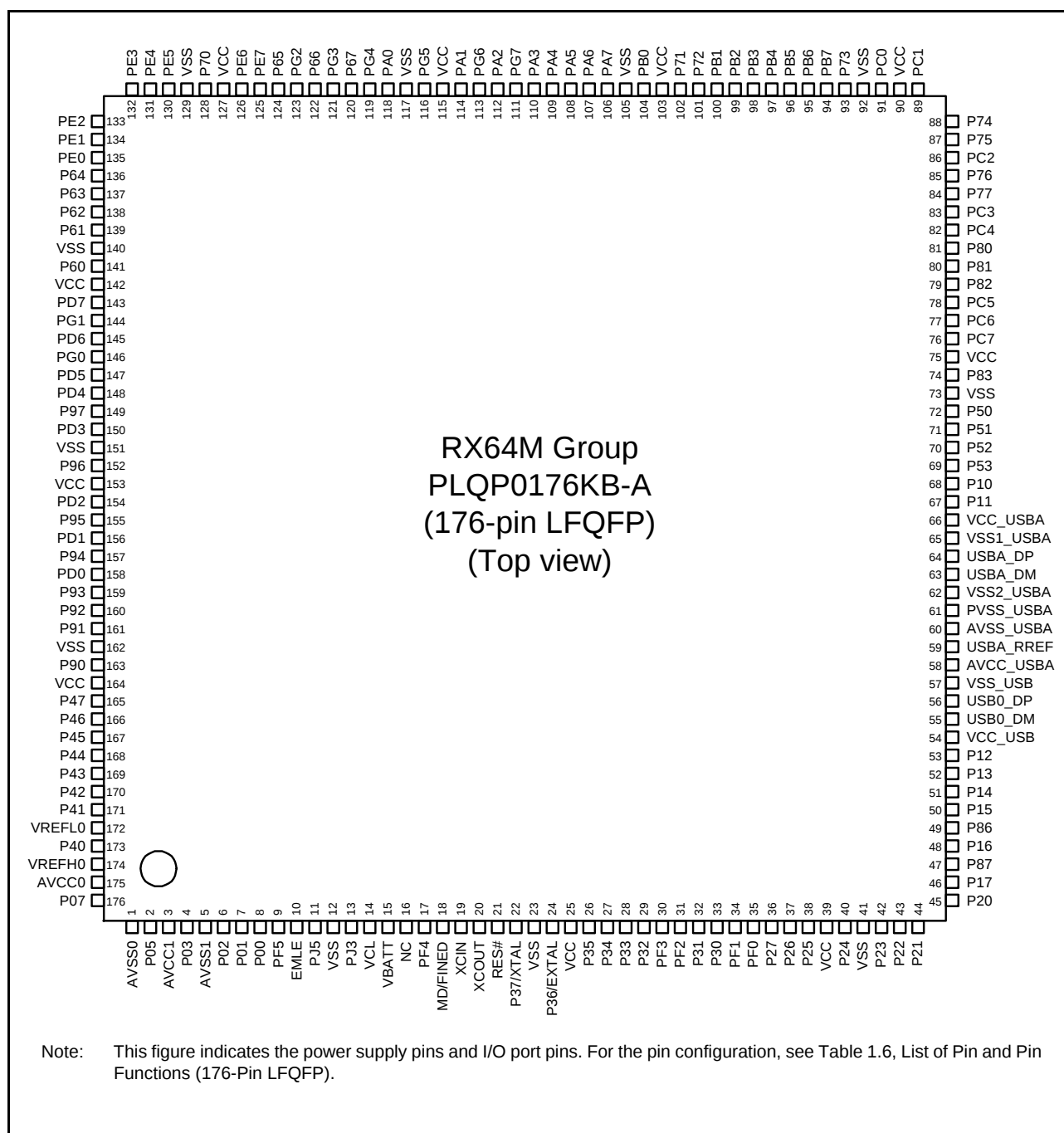


Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15-DS	AN007
134		P46					IRQ14-DS	AN006
135		P45					IRQ13-DS	AN005
136		P44					IRQ12-DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10-DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (2/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C8		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
C9		PE5	D13[A13/ D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0		IRQ5	AN103
C10		PE4	D12[A12/ D12]	MTIOC4D/MTIOC1A/ GTIOC1A-A/PO28	ET0_ERXD2			AN102
D1	XCIN							
D2	XCOU							
D3	MD/FINED							
D4	VBATT							
D5		P45					IRQ13- DS	AN005
D6		P46					IRQ14- DS	AN006
D7		PE6	D14[A14/ D14]	MTIOC6C/GTIOC3B- E/TIC1		MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
D8		PE7	D15[A15/ D15]	MTIOC6A/GTIOC3A- E/TOC1		MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D9		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/GTIOC2A- C/TIOC0B/PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E1	XTAL	P37						
E2	VSS							
E3	RES#							
E4	TRST#	P34		MTIOC0A/TMC13/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
E5		P41					IRQ9-DS	AN001
E6		PA2	A2	MTIOC7A/GTIOC1A- C/PO18	RXD5/SMISO5/ SSCL5/SSLA3-B			
E7		PA6	A6	MTIC5V/MTCLKB/ GTETR-C/TIOCA2/ TMC13/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
E8		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ ET0_MDC		IRQ5-DS	
E9		PA5	A5	MTIOC6B/TIOC0B1/ GTIOC0A-C/PO21	RSPCKA-B/ ET0_LINKSTA			
E10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35					NMI	
F4		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOU/RTIC2/ POE0#/POE10#	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS	
F5		P12		TMC11	RXD2/SMISO2/ SSCL2/SCLO[FM+]		IRQ2	

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/4)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
81		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
82		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
83		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
84		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
85		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
86		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
87		P47					IRQ15-DS	AN007
88		P46					IRQ14-DS	AN006
89		P45					IRQ13-DS	AN005
90		P44					IRQ12-DS	AN004
91		P43					IRQ11-DS	AN003
92		P42					IRQ10-DS	AN002
93		P41					IRQ9-DS	AN001
94	VREFL0							
95		P40					IRQ8-DS	AN000
96	VREFH0							
97	AVCC0							
98		P07					IRQ15	ADTRG0#
99	AVSS0							
100	P05						IRQ13	DA1

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (4 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	DMACaA
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2	ICLK	DMACaA
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2	ICLK	DMACaA
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2	ICLK	DMACaA
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2	ICLK	DMACaA
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2	ICLK	DMACaA
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	DMACaA
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	DMACaA
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	DMACaA
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	DMACaA
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2	ICLK	DMACaA

Table 4.1 List of I/O Registers (Address Order) (6 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 285Dh	EXDMA C1	EXDMA Software Start Register	EDMREQ	8	8	1, 2 BCLK		EXDMA Ca
0008 285Eh	EXDMA C1	EXDMA Status Register	EDMSTS	8	8	1, 2 BCLK		EXDMA Ca
0008 2860h	EXDMA C1	EXDMA External Request Sense Mode Register	EDMRMD	8	8	1, 2 BCLK		EXDMA Ca
0008 2861h	EXDMA C1	EXDMA External Request Flag Register	EDMERF	8	8	1, 2 BCLK		EXDMA Ca
0008 2862h	EXDMA C1	EXDMA Peripheral Request Flag Register	EDMPRF	8	8	1, 2 BCLK		EXDMA Ca
0008 2A00h	EXDMA C	EXDMAC Module Start Register	EDMAST	8	8	1, 2 BCLK		EXDMA Ca
0008 2BE0h	EXDMA C	Cluster Buffer Register 0	CLSBR0	32	32	1, 2 BCLK		EXDMA Ca
0008 2BE4h	EXDMA C	Cluster Buffer Register 1	CLSBR1	32	32	1, 2 BCLK		EXDMA Ca
0008 2BE8h	EXDMA C	Cluster Buffer Register 2	CLSBR2	32	32	1, 2 BCLK		EXDMA Ca
0008 2BECh	EXDMA C	Cluster Buffer Register 3	CLSBR3	32	32	1, 2 BCLK		EXDMA Ca
0008 2BF0h	EXDMA C	Cluster Buffer Register 4	CLSBR4	32	32	1, 2 BCLK		EXDMA Ca
0008 2BF4h	EXDMA C	Cluster Buffer Register 5	CLSBR5	32	32	1, 2 BCLK		EXDMA Ca
0008 2BF8h	EXDMA C	Cluster Buffer Register 6	CLSBR6	32	32	1, 2 BCLK		EXDMA Ca
0008 2BFCh	EXDMA C	Cluster Buffer Register 7	CLSBR7	32	32	1, 2 BCLK		EXDMA Ca
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1, 2 BCLK		Buses
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1, 2 BCLK		Buses
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1, 2 BCLK		Buses
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1, 2 BCLK		Buses
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1, 2 BCLK		Buses
0008 3022h	BSC	CS2 Mode Register	CS2MOD	16	16	1, 2 BCLK		Buses
0008 3024h	BSC	CS2 Wait Control Register 1	CS2WCR1	32	32	1, 2 BCLK		Buses
0008 3028h	BSC	CS2 Wait Control Register 2	CS2WCR2	32	32	1, 2 BCLK		Buses
0008 3032h	BSC	CS3 Mode Register	CS3MOD	16	16	1, 2 BCLK		Buses
0008 3034h	BSC	CS3 Wait Control Register 1	CS3WCR1	32	32	1, 2 BCLK		Buses
0008 3038h	BSC	CS3 Wait Control Register 2	CS3WCR2	32	32	1, 2 BCLK		Buses
0008 3042h	BSC	CS4 Mode Register	CS4MOD	16	16	1, 2 BCLK		Buses
0008 3044h	BSC	CS4 Wait Control Register 1	CS4WCR1	32	32	1, 2 BCLK		Buses
0008 3048h	BSC	CS4 Wait Control Register 2	CS4WCR2	32	32	1, 2 BCLK		Buses
0008 3052h	BSC	CS5 Mode Register	CS5MOD	16	16	1, 2 BCLK		Buses
0008 3054h	BSC	CS5 Wait Control Register 1	CS5WCR1	32	32	1, 2 BCLK		Buses
0008 3058h	BSC	CS5 Wait Control Register 2	CS5WCR2	32	32	1, 2 BCLK		Buses
0008 3062h	BSC	CS6 Mode Register	CS6MOD	16	16	1, 2 BCLK		Buses
0008 3064h	BSC	CS6 Wait Control Register 1	CS6WCR1	32	32	1, 2 BCLK		Buses
0008 3068h	BSC	CS6 Wait Control Register 2	CS6WCR2	32	32	1, 2 BCLK		Buses
0008 3072h	BSC	CS7 Mode Register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 Wait Control Register 1	CS7WCR1	32	32	1, 2 BCLK		Buses
0008 3078h	BSC	CS7 Wait Control Register 2	CS7WCR2	32	32	1, 2 BCLK		Buses
0008 3802h	BSC	CS0 Control Register	CS0CR	16	16	1, 2 BCLK		Buses
0008 380Ah	BSC	CS0 Recovery Cycle Register	CS0REC	16	16	1, 2 BCLK		Buses
0008 3812h	BSC	CS1 Control Register	CS1CR	16	16	1, 2 BCLK		Buses
0008 381Ah	BSC	CS1 Recovery Cycle Register	CS1REC	16	16	1, 2 BCLK		Buses

Table 4.1 List of I/O Registers (Address Order) (8 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUA
0008 711Ah to 0008 71FFh	ICU	DTC Transfer Request Enable Registers 026 to 255	DTCER026 to DTCER255	8	8	2 ICLK		ICUA
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUA
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUA
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUA
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUA
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUA
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8	2 ICLK		ICUA
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8	2 ICLK		ICUA
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8	2 ICLK		ICUA
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8	2 ICLK		ICUA
0008 7410h	ICU	DMAC Trigger Select Register 4	DMRSR4	8	8	2 ICLK		ICUA
0008 7414h	ICU	DMAC Trigger Select Register 5	DMRSR5	8	8	2 ICLK		ICUA
0008 7418h	ICU	DMAC Trigger Select Register 6	DMRSR6	8	8	2 ICLK		ICUA
0008 741Ch	ICU	DMAC Trigger Select Register 7	DMRSR7	8	8	2 ICLK		ICUA
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUA
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUA
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUA
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUA
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUA
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUA
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUA
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUA
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUA
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUA
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUA
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7630h	ICU	Group BL0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (12 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 7908h	ICU	Software Configurable Interrupt A Request Register 8	PIAR8	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 7909h	ICU	Software Configurable Interrupt A Request Register 9	PIAR9	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Ah	ICU	Software Configurable Interrupt A Request Register A	PIARA	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 790Bh	ICU	Software Configurable Interrupt A Request Register B	PIARB	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D0h	ICU	Software Configurable Interrupt A Source Select Register 208	SLIAR208	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D1h	ICU	Software Configurable Interrupt A Source Select Register 209	SLIAR209	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D2h	ICU	Software Configurable Interrupt A Source Select Register 210	SLIAR210	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D3h	ICU	Software Configurable Interrupt A Source Select Register 211	SLIAR211	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D4h	ICU	Software Configurable Interrupt A Source Select Register 212	SLIAR212	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D5h	ICU	Software Configurable Interrupt A Source Select Register 213	SLIAR213	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D6h	ICU	Software Configurable Interrupt A Source Select Register 214	SLIAR214	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D7h	ICU	Software Configurable Interrupt A Source Select Register 215	SLIAR215	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D8h	ICU	Software Configurable Interrupt A Source Select Register 216	SLIAR216	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79D9h	ICU	Software Configurable Interrupt A Source Select Register 217	SLIAR217	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DAh	ICU	Software Configurable Interrupt A Source Select Register 218	SLIAR218	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DBh	ICU	Software Configurable Interrupt A Source Select Register 219	SLIAR219	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DCh	ICU	Software Configurable Interrupt A Source Select Register 220	SLIAR220	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DDh	ICU	Software Configurable Interrupt A Source Select Register 221	SLIAR221	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DEh	ICU	Software Configurable Interrupt A Source Select Register 222	SLIAR222	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79DFh	ICU	Software Configurable Interrupt A Source Select Register 223	SLIAR223	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E0h	ICU	Software Configurable Interrupt A Source Select Register 224	SLIAR224	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E1h	ICU	Software Configurable Interrupt A Source Select Register 225	SLIAR225	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E2h	ICU	Software Configurable Interrupt A Source Select Register 226	SLIAR226	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E3h	ICU	Software Configurable Interrupt A Source Select Register 227	SLIAR227	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E4h	ICU	Software Configurable Interrupt A Source Select Register 228	SLIAR228	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E5h	ICU	Software Configurable Interrupt A Source Select Register 229	SLIAR229	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E6h	ICU	Software Configurable Interrupt A Source Select Register 230	SLIAR230	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E7h	ICU	Software Configurable Interrupt A Source Select Register 231	SLIAR231	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E8h	ICU	Software Configurable Interrupt A Source Select Register 232	SLIAR232	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79E9h	ICU	Software Configurable Interrupt A Source Select Register 233	SLIAR233	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79EAh	ICU	Software Configurable Interrupt A Source Select Register 234	SLIAR234	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA
0008 79EBh	ICU	Software Configurable Interrupt A Source Select Register 235	SLIAR235	8	8	2 ICLK to 1 PCLKA	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (38 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Registers 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C428h	RTC	RTC Control Register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ah	RTC	Frequency Register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Ch	RTC	Frequency Register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	RTCd
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C444h	RTC	Time Capture Control Register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2, 3 PCLKB	2 ICLK	RTCd
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2, 3 PCLKB	2 ICLK	RTCd

Table 4.1 List of I/O Registers (Address Order) (52 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C85h	MTU5	Timer Control Register 2	TCR2U	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C95h	MTU5	Timer Control Register 2	TCR2V	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA5h	MTU5	Timer Control Register 2	TCR2W	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 2000h	GPT	General PWM Timer Software Start Register	GTSTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2002h	GPT	Noise Filter Control Register	NFCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register	GTHSCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register	GTHCCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register	GTHSSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register	GTHPSR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Ch	GPT	General PWM Timer Write-Protection Register	GTWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 200Eh	GPT	General PWM Timer Sync Register	GTSYNC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register	GTETINT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register	GTBDR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2018h	GPT	General PWM Timer Start Write-Protection Register	GTSWP	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2100h	GPT0	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2102h	GPT0	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2104h	GPT0	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2106h	GPT0	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2108h	GPT0	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Ah	GPT0	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Ch	GPT0	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 210Eh	GPT0	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2110h	GPT0	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2112h	GPT0	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2114h	GPT0	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2116h	GPT0	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2118h	GPT0	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Ah	GPT0	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Ch	GPT0	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 211Eh	GPT0	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2120h	GPT0	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA

Table 4.1 List of I/O Registers (Address Order) (57 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLKA	ICLK < PCLKA	
000C 4810h	EPTPC 0	SYNFP MAC Address Register	SYMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4814h	EPTPC 0	SYNFP MAC Address Register	SYMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 481Ch	EPTPC 0	SYNFP Local IP Address Register	SYIPADDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4840h	EPTPC 0	SYNFP Specification Version Setting Register	SYSPVRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4844h	EPTPC 0	SYNFP Domain Number Setting Register	SYDOMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4850h	EPTPC 0	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4854h	EPTPC 0	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4858h	EPTPC 0	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 485Ch	EPTPC 0	Delay_Resp Message Flag Field Setting Register	DYRPFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4860h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4864h	EPTPC 0	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4868h	EPTPC 0	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4880h	EPTPC 0	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4890h	EPTPC 0	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4894h	EPTPC 0	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4898h	EPTPC 0	SYNFP Transmission Enable Register	SYTRENR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A0h	EPTPC 0	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A4h	EPTPC 0	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48A8h	EPTPC 0	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C0h	EPTPC 0	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C4h	EPTPC 0	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48C8h	EPTPC 0	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48CCh	EPTPC 0	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48D0h	EPTPC 0	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48D4h	EPTPC 0	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E0h	EPTPC 0	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E4h	EPTPC 0	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48E8h	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48ECh	EPTPC 0	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48F0h	EPTPC 0	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 48F4h	EPTPC 0	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC

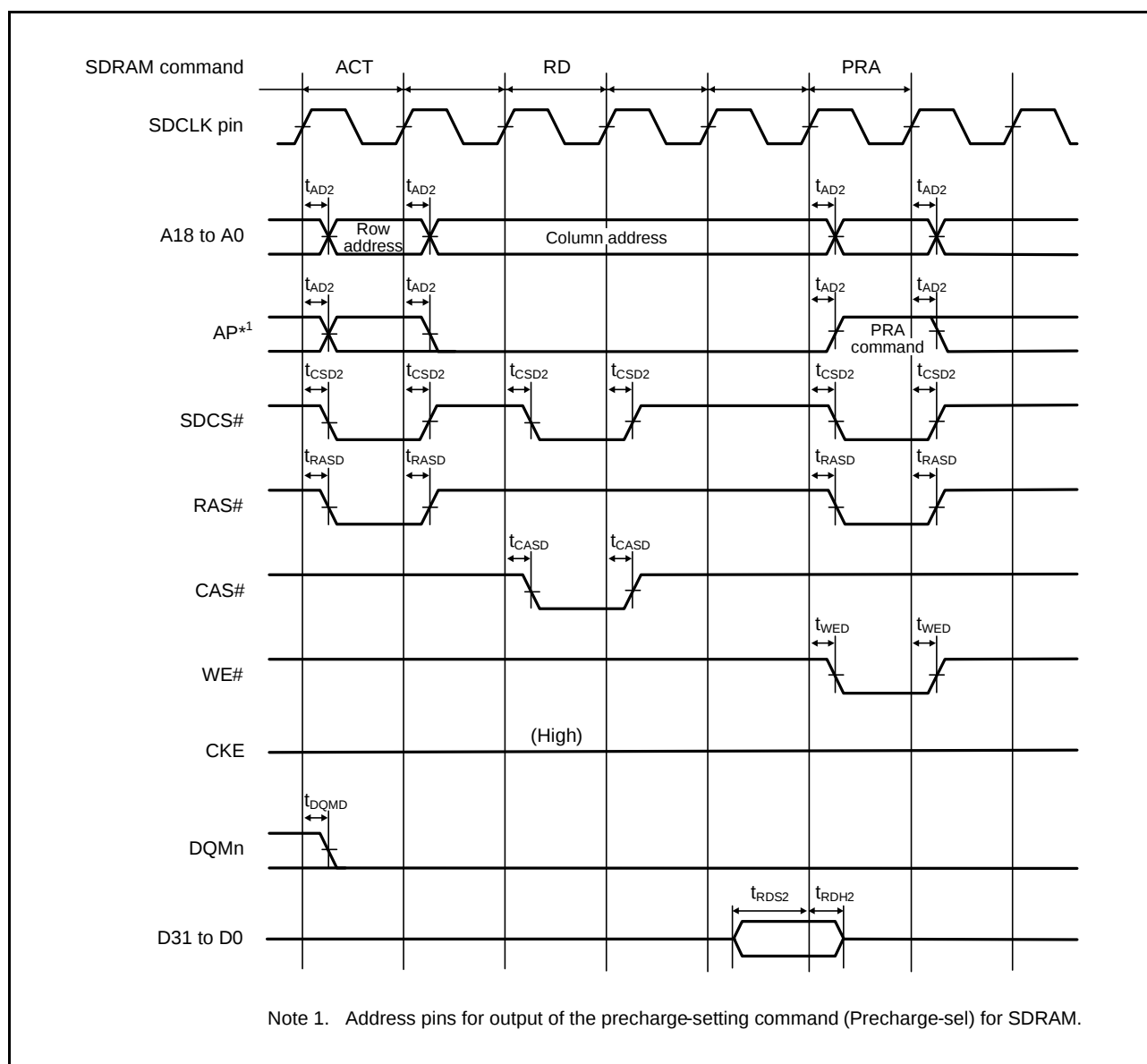


Figure 5.23 SDRAM Space Single Read Bus Timing

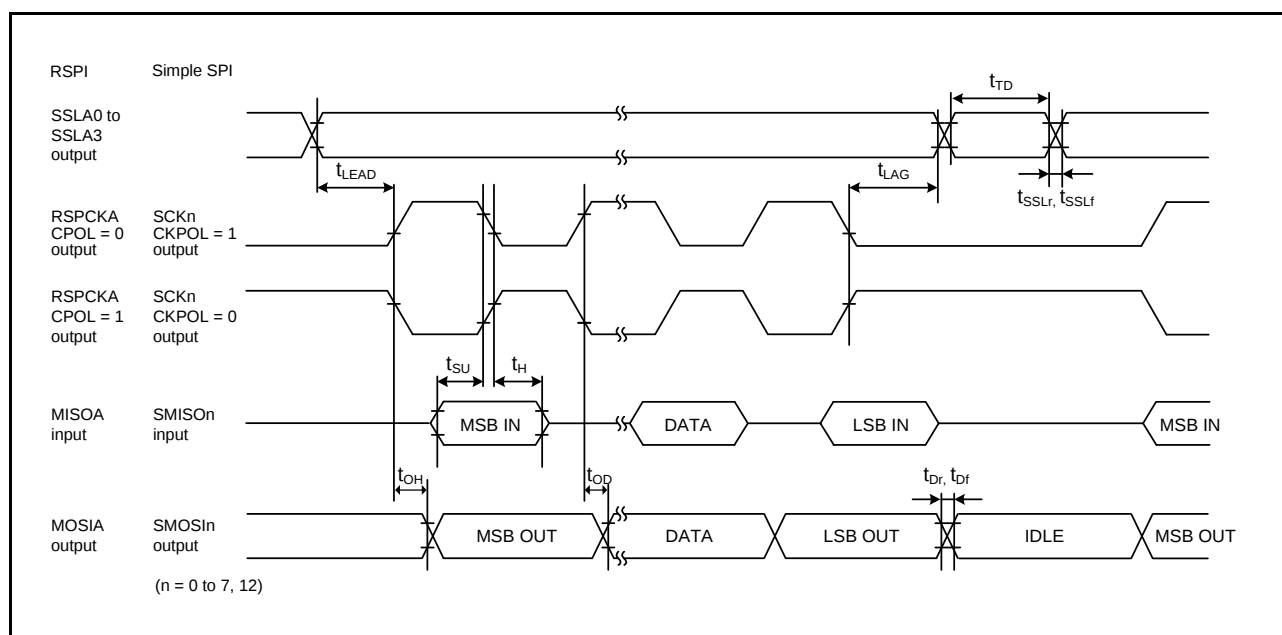


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

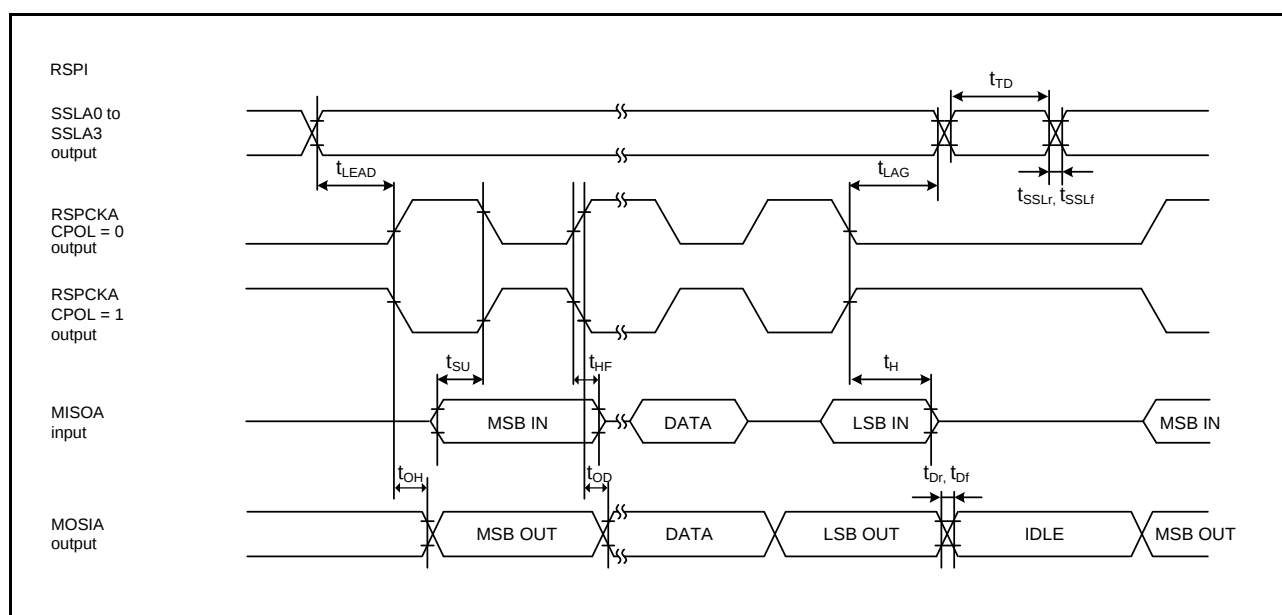


Figure 5.50 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

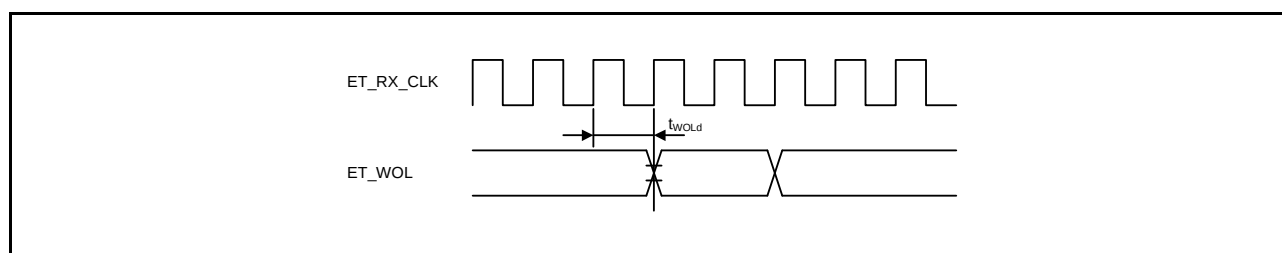
**Figure 5.71 WOL Output Timing (MII)**

Table 5.54 Data Flash Memory Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,

$V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V

$V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,

Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	μs
	64 bytes	t_{DBC64}	—	—	280	—	—	100	μs
	2 Kbytes	t_{DBC2K}	—	—	6169	—	—	2200	μs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	—
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	μs
Forced stop command		t_{FD}	—	—	32	—	—	20	μs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	—

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 100000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

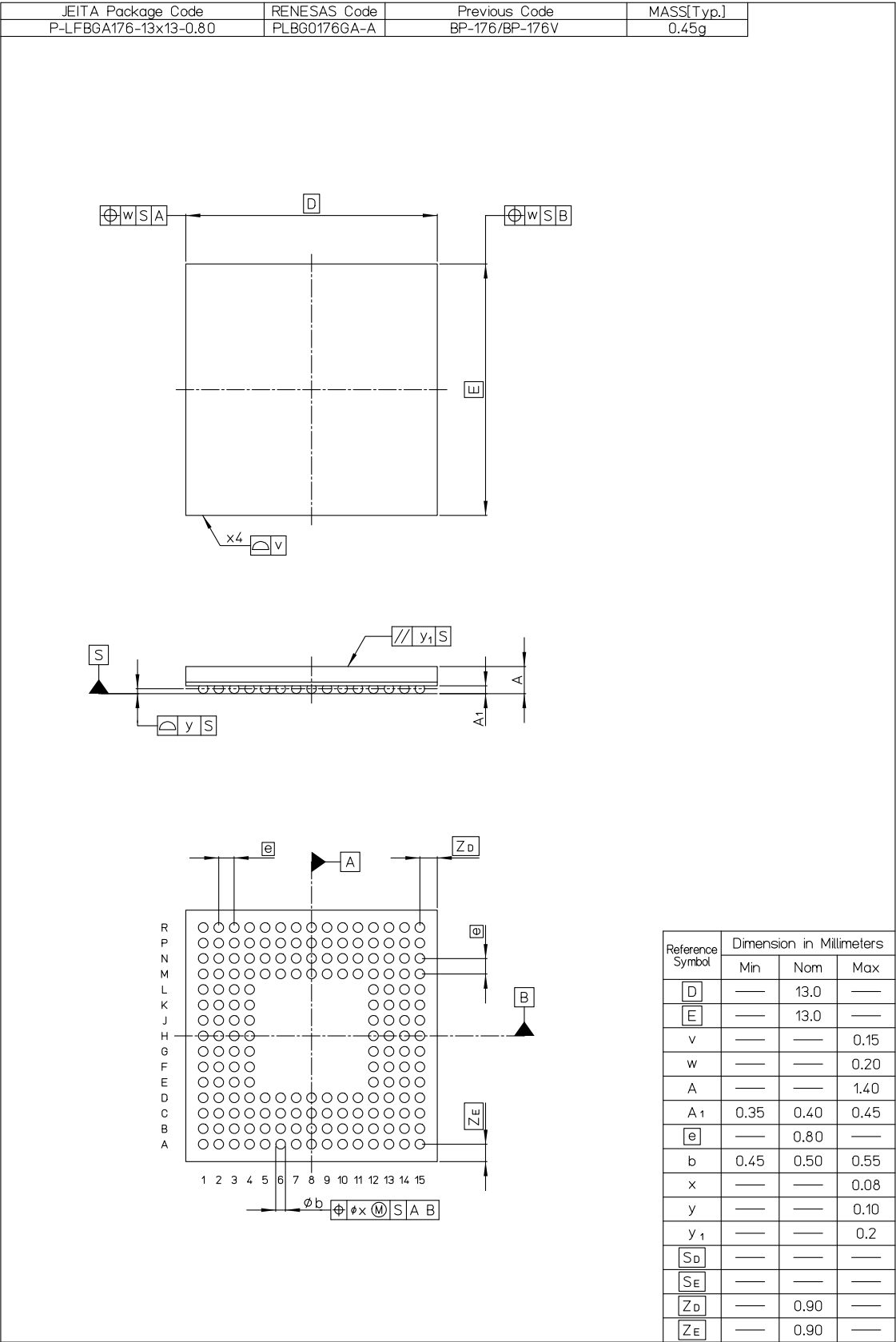


Figure B 176-Pin LFBGA (PLBG0176GA-A)

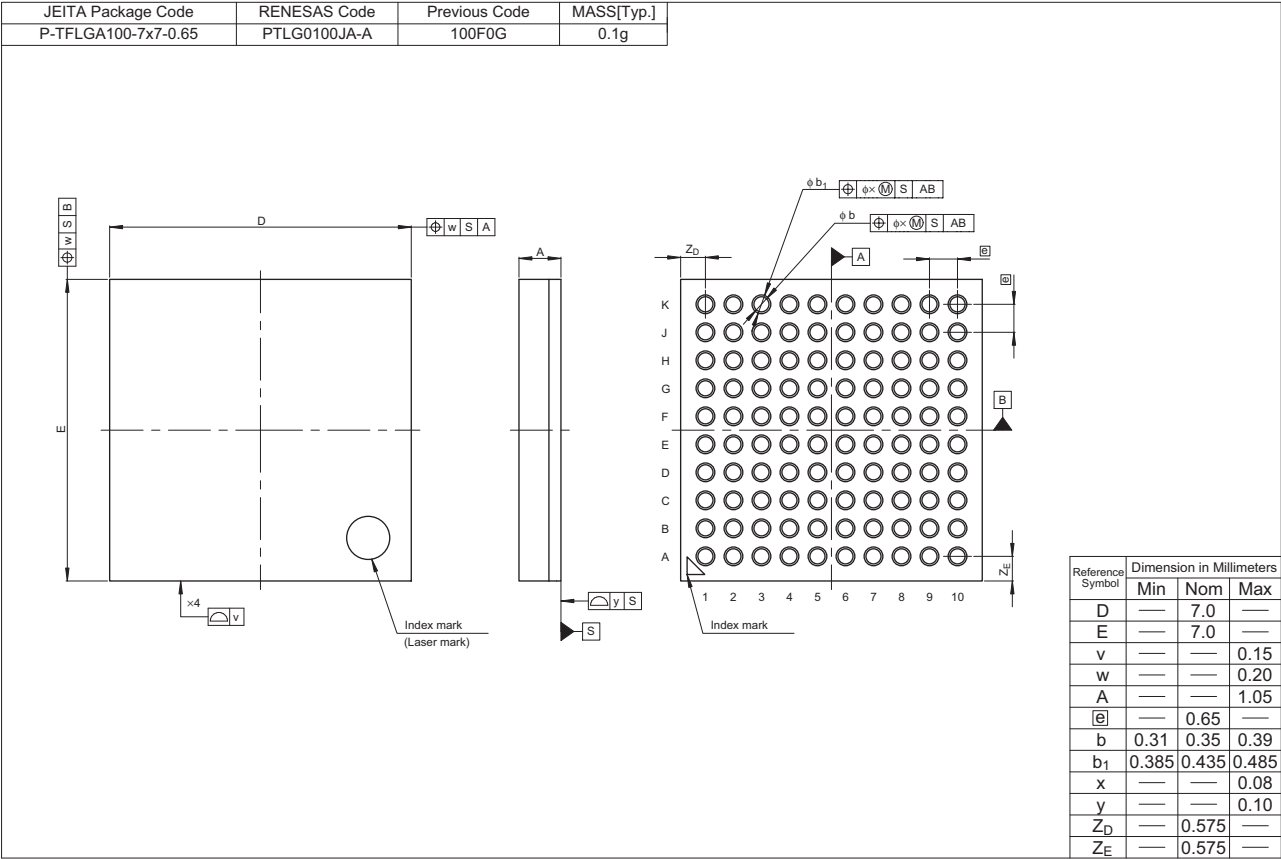


Figure F 100-Pin TFLGA (PTLG0100JA-A)