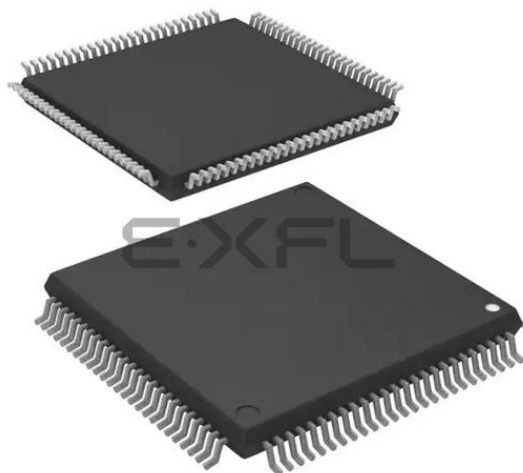




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlddfp-v1

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 120 MHz 32-bit RX CPU (RXv2) - Minimum instruction execution time: One instruction per state (cycle of the system clock) - Address space: 4-Gbyte linear - Register set of the CPU - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 11 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: $32 \times 32 \rightarrow 64$ bits - On-chip divider: $32 / 32 \rightarrow 32$ bits - Barrel shifter: 32 bits
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	Code flash memory	- Capacity: 2 Mbytes, 2.5 Mbytes, 3 Mbytes, 4 Mbytes 120 MHz, no-wait access - On-board programming: Four types - Off-board programming (parallel programmer mode) - The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9.
	Data flash memory	- Capacity: 64 Kbytes - Programming/erasing: 100,000 times
	RAM	- Capacity: 512 Kbytes 120 MHz, no-wait access - SED (single error detection)
	Unique ID	12-byte length ID unique to the device
	RAM with ECC	- Capacity: 32 Kbytes 120 MHz, single wait access - SEC-DED (single error correction/double error detection)
	Standby RAM	- Capacity: 8 Kbytes - Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access
Operating modes		- Operating modes by the mode-setting pins at the time of release from the reset state - Single-chip mode - Boot mode (for the SCI interface) - Boot mode (for the USB interface) - User boot mode - Selection of operating mode by register setting - Single-chip mode, user boot mode - On-chip ROM disabled extended mode - On-chip ROM enabled extended mode - Endian selectable

Table 1.1 Outline of Specifications (2/9)

Classification	Module/Function	Description
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICKL), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICKL): Up to 120 MHz Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt. • Voltage detection circuit 0 - Capable of generating an internal reset - The option-setting memory can be used to select enabling or disabling of the reset. - Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V) • Voltage detection circuits 1 and 2 - Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V) - Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) - Capable of generating an internal reset • Two types of timing are selectable for release from reset - An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable - Voltage detection monitoring - Event linking
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes - Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating.

Table 1.3 List of Products (2/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX64M	R5F564MFCDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDFP	PLQP0100KB-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDBG	PLBG0176GA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDBG	PLBG0176GA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDBG	PLBG0176GA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDBG	PLBG0176GA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDLC	PTLG0177KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDLC	PTLG0177KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDLC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGLDC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDLDC	PTLG0177KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDLDC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDLDC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDLDC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDLDC	PTLG0177KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDLK	PTLG0145KA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDLK	PTLG0145KA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGLDK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDLK	PTLG0145KA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available

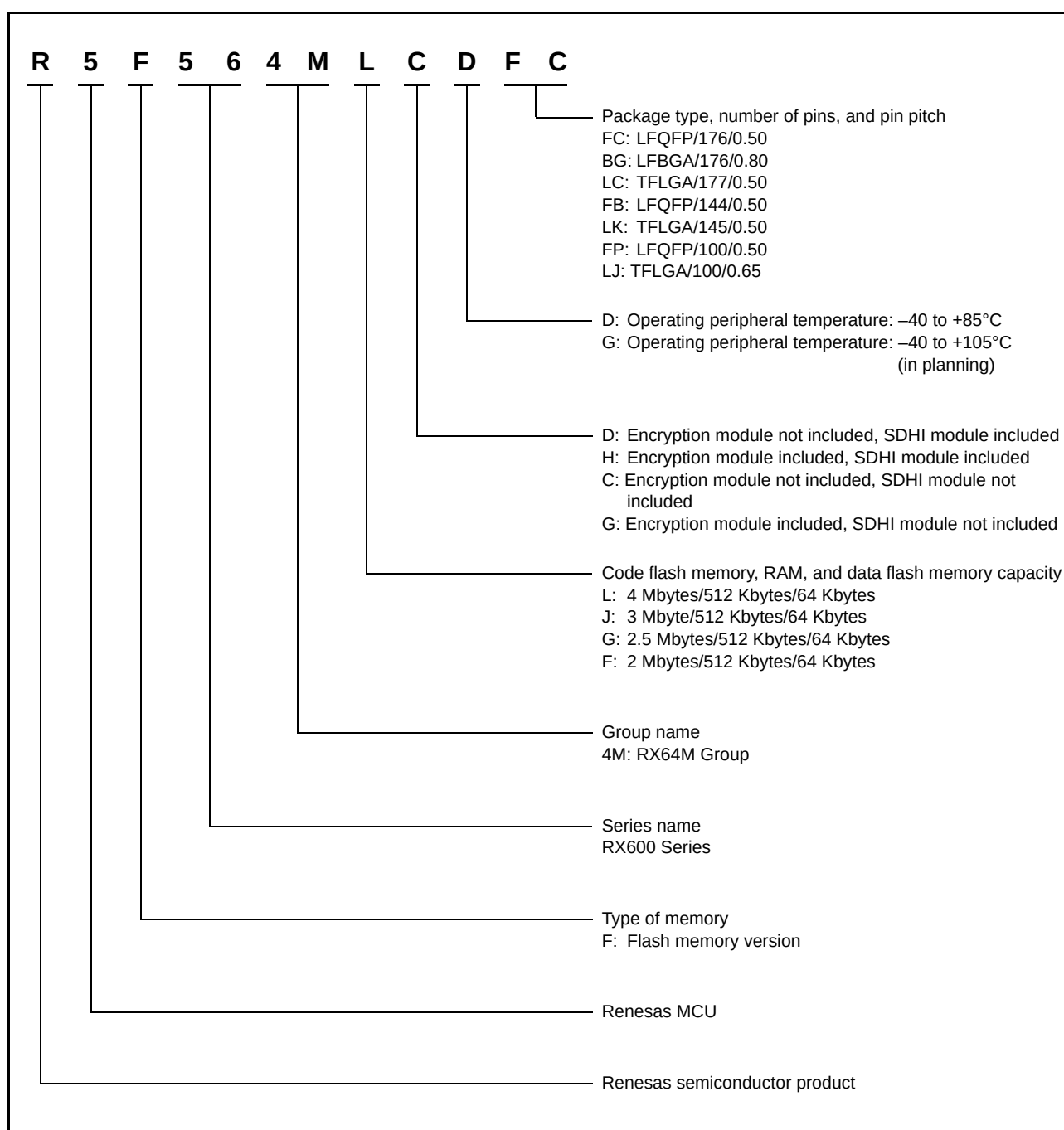


Figure 1.1 How to Read the Product Part Number

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX64M Group PLBG0176GA-A (176-Pin LFBGA) (Upper Perspective View)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								VCC_ USB_A	VSS1_ USB_A	P10	P11	8
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USB_A	USBA_ DM	USBA_ DP	7
6	VCC	P91	P90	P93								AVCC_ USB_A	VSS_ USB	AVSS_ USB_A	PVSS_ USB_A	6
5	P46	P47	P45	P44								VCC_ USB	P12	USB0_ DP	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCiG, SCIh, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
P2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOC0B/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
P3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOC0B5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
P5					USB0_DP			
P6	AVSS_ USBA							
P7					USBA_DM			
P8		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
P9		P52	RD#		RXD2/SMISO2/ SSCL2			
P10		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
P13		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV/	MMC_CD-A/ SDHI_D3-A		
P14		P75	CS5#	PO20	SCK11/RTS11/ ET0_ERXD0/ RMII0_RXD0/	MMC_RES#-A/ SDHI_D2-A		
P15	VCC							
R1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOC0B3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOC0B1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
R4		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
R5					USB0_DM			
R6	PVSS_ USBA							
R7					USBA_DP			
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN			
R9		P53*2	BCLK					
R10	VSS							

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (2/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/ET1_WOL			
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT			
38		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
39	VCC							
40		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
41	VSS							
42		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSISCK0	PIXD7		
43		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ USBA_OVRCURB/ AUDIO_MCLK	PIXD6		
44		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
45		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
46		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
47		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
48		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
49		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
50		P15		MTIOC0B/MTCLKB/ GTETRg-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS/ USBA_VBUSEN/ SSIWS1	PIXD0	IRQ5	
51		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
52		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
53		P12	WR3#/BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		IRQ2	
54	VCC_USB							
55					USB0_DM			
56					USB0_DP			

Table 1.8 List of Pin and Pin Functions (144-Pin LQFP) (5/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
117		P60	CS0#					
118	VCC							
119		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
120		PD6	D6[A6/D6]	MTIC5V/MTIOC8A/ POE4#		MMC_D0-B/ SDHI_D0-B/ QIO0-B/QMO-B	IRQ6	AN106
121		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
122		PD4	D4[A4/D4]	MTIOC8B/POE11#		MMC_CMD-B/ SDHI_CMD-B/ QSSL-B	IRQ4	AN112
123		PD3	D3[A3/D3]	MTIOC8D/ GTIOC0A-E/POE8#/ TOC2		MMC_D3-B/ SDHI_D3-B/ QIO3-B	IRQ3	AN111
124		PD2	D2[A2/D2]	MTIOC4D/ GTIOC0B-E/TIC2	CRX0	MMC_D2-B/ SDHI_D2-B/ QIO2-B	IRQ2	AN110
125		PD1	D1[A1/D1]	MTIOC4B/ GTIOC1A-E/POE0#	CTX0		IRQ1	AN109
126		PD0	D0[A0/D0]	GTIOC1B-E/POE4#			IRQ0	AN108
127		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
128		P92	A18	POE4#	RXD7/SMISO7/SSCL7			AN116
129		P91	A17		SCK7			AN115
130	VSS							
131		P90	A16		TXD7/SMOSI7/SSDA7			AN114
132	VCC							
133		P47					IRQ15-DS	AN007
134		P46					IRQ14-DS	AN006
135		P45					IRQ13-DS	AN005
136		P44					IRQ12-DS	AN004
137		P43					IRQ11-DS	AN003
138		P42					IRQ10-DS	AN002
139		P41					IRQ9-DS	AN001
140	VREFL0							
141		P40					IRQ8-DS	AN000
142	VREFH0							
143	AVCC0							
144		P07					IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H9		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
J1		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/ MTIOC4B/GTIOC0B- B/TIOCB0/TCLKD/ TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMC11/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/#SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOC3D/ PO3	TXD3/CTS0#/#RTS0#/ SMOSI3/SS0#/ SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/#RTS1#/#SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/#BC1#/ WAIT#		SCK2			
K8		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/#ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B- D/TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B- D/TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 4.1 List of I/O Registers (Address Order) (3 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 12C3h	ECCRAM	ECCRAM 1-Bit Error Status Register	ECCRAM1STS	8	8	2 ICLK		RAM
0008 12C4h	ECCRAM	ECCRAM Protection Register	ECCRAMPRCR	8	8	2 ICLK		RAM
0008 12C8h	ECCRAM	ECCRAM 2-Bit Error Address Capture Register	ECCRAM2ECAD	32	32	2 ICLK		RAM
0008 12CCh	ECCRAM	ECCRAM 1-Bit Error Address Capture Register	ECCRAM1ECAD	32	32	2 ICLK		RAM
0008 12D0h	ECCRAM	ECCRAM Protection Register 2	ECCRAMPRCR2	8	8	2 ICLK		RAM
0008 12D4h	ECCRAM	ECCRAM Test Control Register	ECCRAMETST	8	8	2 ICLK		RAM
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		Buses
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		Buses
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		Buses
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		Buses
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK		DMACaA
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 201Fh	DMAC0	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 205Fh	DMAC1	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 209Fh	DMAC2	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA

Table 4.1 List of I/O Registers (Address Order) (29 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 B13Ah	ELC	Event Link Setting Register 42	ELSR42	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Bh	ELC	Event Link Setting Register 43	ELSR43	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Ch	ELC	Event Link Setting Register 44	ELSR44	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Dh	ELC	Event Link Setting Register 45	ELSR45	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B13Fh	ELC	Event Link Option Setting Register F	ELOPF	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B141h	ELC	Event Link Option Setting Register H	ELOPH	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B142h	ELC	Event Link Option Setting Register I	ELOPI	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B143h	ELC	Event Link Option Setting Register J	ELOPJ	8	8	2, 3 PCLKB	2 ICLK	ELC
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIh
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4, 5 PCLKB	2 ICLK	SCIh
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B321h	SCI12	Control Register 0	CR0	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B322h	SCI12	Control Register 1	CR1	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B323h	SCI12	Control Register 2	CR2	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B324h	SCI12	Control Register 3	CR3	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B325h	SCI12	Port Control Register	PCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B327h	SCI12	Status Register	STR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2, 3 PCLKB	2 ICLK	SCIh
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2, 3 PCLKB	2 ICLK	SCIh

Table 4.1 List of I/O Registers (Address Order) (41 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0009 1852h	CAN1	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1853h	CAN1	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 1854h	CAN1	Time Stamp Register	TSR	16	16	2, 3 PCLKB	2 ICLK	CAN
0009 1856h	CAN1	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 1858h	CAN1	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2200h to 0009 23FFh	CAN2	Mailbox Registers 0 to 31	MB0 to 31	128	8, 16, 32*6	2, 3 PCLKB	2 ICLK	CAN
0009 2400h to 0009 241Fh	CAN2	Mask Registers 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2420h	CAN2	FIFO Received ID Compare Register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2424h	CAN2	FIFO Received ID Compare Register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2428h	CAN2	Mask Invalid Register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 242Ch	CAN2	Mailbox Interrupt Enable Register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2820h to 0009 283Fh	CAN2	Message Control Registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2840h	CAN2	Control Register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2842h	CAN2	Status Register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2844h	CAN2	Bit Configuration Register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 2848h	CAN2	Receive FIFO Control Register	RFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2849h	CAN2	Receive FIFO Pointer Control Register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ah	CAN2	Transmit FIFO Control Register	TFCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Bh	CAN2	Transmit FIFO Pointer Control Register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Ch	CAN2	Error Interrupt Enable Register	EIER	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Dh	CAN2	Error Interrupt Factor Judge Register	EIFR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Eh	CAN2	Receive Error Count Register	RECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 284Fh	CAN2	Transmit Error Count Register	TECR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2850h	CAN2	Error Code Store Register	ECSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2851h	CAN2	Channel Search Support Register	CSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2852h	CAN2	Mailbox Search Status Register	MSSR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2853h	CAN2	Mailbox Search Mode Register	MSMR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 2854h	CAN2	Time Stamp Register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2856h	CAN2	Acceptance Filter Support Register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	CAN
0009 2858h	CAN2	Test Control Register	TCR	8	8	2, 3 PCLKB	2 ICLK	CAN
0009 4200h	CMTW0	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4204h	CMTW0	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4208h	CMTW0	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4210h	CMTW0	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4214h	CMTW0	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4218h	CMTW0	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 421Ch	CMTW0	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4220h	CMTW0	Output Compare Register 0	CMWOCR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4224h	CMTW0	Output Compare Register 1	CMWOCR1	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4280h	CMTW1	Timer Start Register	CMWSTR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4284h	CMTW1	Timer Control Register	CMWCR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4288h	CMTW1	Timer I/O Control Register	CMWIOR	16	16	2, 3 PCLKB	2 ICLK	CMTW
0009 4290h	CMTW1	Timer Counter	CMWCNT	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4294h	CMTW1	Compare Match Constant Register	CMWCOR	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 4298h	CMTW1	Input Capture Register 0	CMWICR0	32	32	2, 3 PCLKB	2 ICLK	CMTW
0009 429Ch	CMTW1	Input Capture Register 1	CMWICR1	32	32	2, 3 PCLKB	2 ICLK	CMTW

Table 4.1 List of I/O Registers (Address Order) (48 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0440h	PTPED MAC	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0448h	PTPED MAC	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0450h	PTPED MAC	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0458h	PTPED MAC	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0464h	PTPED MAC	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0468h	PTPED MAC	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0470h	PTPED MAC	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0478h	PTPED MAC	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 047Ch	PTPED MAC	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04C8h	PTPED MAC	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04CCh	PTPED MAC	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D4h	PTPED MAC	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D8h	PTPED MAC	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0500h	EPTPC	PTP Reset Register	PTRSTR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 0504h	EPTPC	STCA Clock Select Register	STCSELR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 1200h	MTU3	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (54 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2200h	GPT2	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2204h	GPT2	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2206h	GPT2	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2208h	GPT2	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 220Ch	GPT2	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 220Eh	GPT2	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2210h	GPT2	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2212h	GPT2	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2214h	GPT2	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2216h	GPT2	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2218h	GPT2	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 221Ch	GPT2	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 221Eh	GPT2	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2220h	GPT2	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2224h	GPT2	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2228h	GPT2	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2230h	GPT2	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2234h	GPT2	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2236h	GPT2	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2280h	GPT3	General PWM Timer I/O Control Register	GTIOR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register	GTINTAD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2284h	GPT3	General PWM Timer Control Register	GTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2286h	GPT3	General PWM Timer Buffer Enable Register	GTBER	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2288h	GPT3	General PWM Timer Count Direction Register	GTUDC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 228Ch	GPT3	General PWM Timer Status Register	GTST	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 228Eh	GPT3	General PWM Timer Counter	GTCNT	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2290h	GPT3	General PWM Timer Compare Capture Register A	GTCCRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2292h	GPT3	General PWM Timer Compare Capture Register B	GTCCRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2294h	GPT3	General PWM Timer Compare Capture Register C	GTCCRC	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2296h	GPT3	General PWM Timer Compare Capture Register D	GTCCRD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 2298h	GPT3	General PWM Timer Compare Capture Register E	GTCCRE	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA

Table 5.4 DC Characteristics (3)

Conditions: $V_{CC} = AVCC0 = AVCC1 = VREFH0 = V_{CC_USB} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = VREFL0 = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	110	mA	ICLK = 120 MHz PCLKA = 120 MHz PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 60 MHz FCLK = 60 MHz BCLK = 120 MHz BCLK pin = 60 MHz	
		Normal	Peripheral function clock signal supplied*4		—	39	—			
			Peripheral function clock signal stopped*4		—	16	—			
		Coremark	Peripheral function clock signal stopped*4		—	21	—			
		Sleep mode: Supply of the clock signal to peripheral modules is stopped*4				32	61			
		All-module-clock-stop mode (reference value)			—	10	28			
		Increased by BGO operation *5	Reading from the code flash memory while the data flash memory is being programmed		—	7	—			
			Reading from the code flash memory while the code flash memory is being programmed		—	10	—			
		Low-speed operating mode 1: Supply of the clock signal to peripheral modules is stopped*4			—	3	—			All clocks 1 MHz
		Low-speed operating mode 2: Supply of the clock signal to peripheral modules is stopped*4			—	1.2	—			All clocks 32.768 kHz
	Software standby mode		—	0.7	10					
	Deep software standby mode	Power supplied to standby RAM and USB resume detecting unit (USB0 only)		—	22	63	μA			
		Power not supplied to standby RAM and USB resume detecting unit (USB0 only)	Power-on reset circuit and low-power consumption function disabled*6	—	12.5	26				
			Power-on reset circuit and low-power consumption function enabled*7	—	3.1	13.5				
		Increased by RTC operation	When a crystal resonator for low clock loads is in use	—	0.6	—				
			When a crystal resonator for standard clock loads is in use	—	2.0	—				
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal resonator for low clock loads is in use	—	0.9	—		V _{BATT} = 2.0 V, VCC = 0 V		
				—	1.6	—		V _{BATT} = 3.3 V, VCC = 0 V		
				—	1.7	—		V _{BATT} = 2.0 V, VCC = 0 V		
				—	3.3	—		V _{BATT} = 3.3 V, VCC = 0 V		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Supply of the clock signal to peripheral modules is stopped in this state. This does not include operations as BGO (background operations).

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK/PCLKA:PCLKB/PCLKC/PCLKD:BCLK:BCLK pin = 10:5:10:5 when EXTAL = 12 MHz)
 I_{CC} Max. = $0.77 \times f + 18$ (max. operation in high-speed operating mode)
 I_{CC} Typ. = $0.08 \times f + 6$ (normal operation in high-speed operating mode)
 I_{CC} Typ. = $0.5 \times f + 2.6$ (low-speed operating mode 1)
 I_{CC} Max. = $0.36 \times f + 18$ (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether supply of the clock signal to peripheral modules continues or is stopped only depends on the state determined by the settings of the bits in module stop control registers A to D. The setting for the peripheral module clock stopped state is FCLK = BCLK = PCLKA = PCLKB = PCLKC = PCLKD = BCLK pin = 3.75 MHz (division by 64).

Note 5. This is the increase for programming or erasure of the code flash memory (limitations apply to the combinations of ranges in which writing proceed) or data flash memory during program execution in the code flash memory.

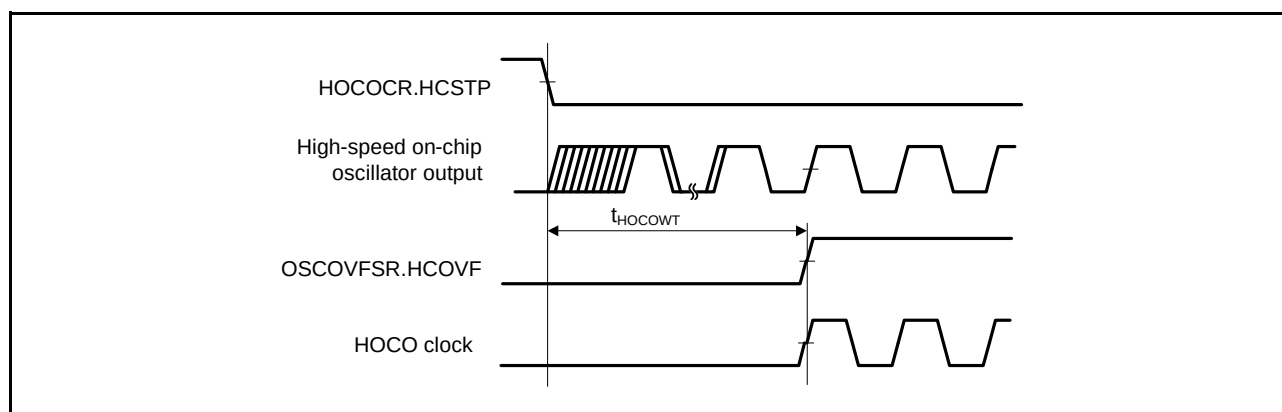
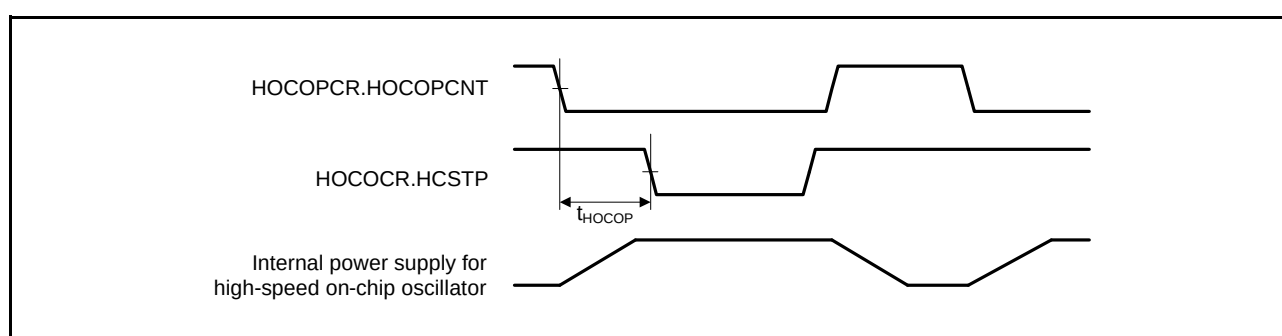
Note 6. The low power consumption function is disabled and DEEPCUT[1:0] = 01b.

Note 7. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Table 5.15 HOCO Clock Timing

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	f_{HOCO}	15.61	16	16.39	MHz	$-20^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$
		17.56	18	18.44	MHz	
		19.52	20	20.48	MHz	
		15.52	16	16.48	MHz	$-40^{\circ}\text{C} \leq T_a < -20^{\circ}\text{C}$
		17.46	18	18.54	MHz	
		19.40	20	20.60	MHz	
HOCO clock oscillation stabilization wait time	t_{HOCOWT}	—	105	149	μs	Figure 5.8
HOCO clock power supply stabilization time	t_{HOCOP}	—	—	150	μs	Figure 5.9

**Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)****Figure 5.9 High-Speed On-Chip Oscillator Power Supply Control Timing**

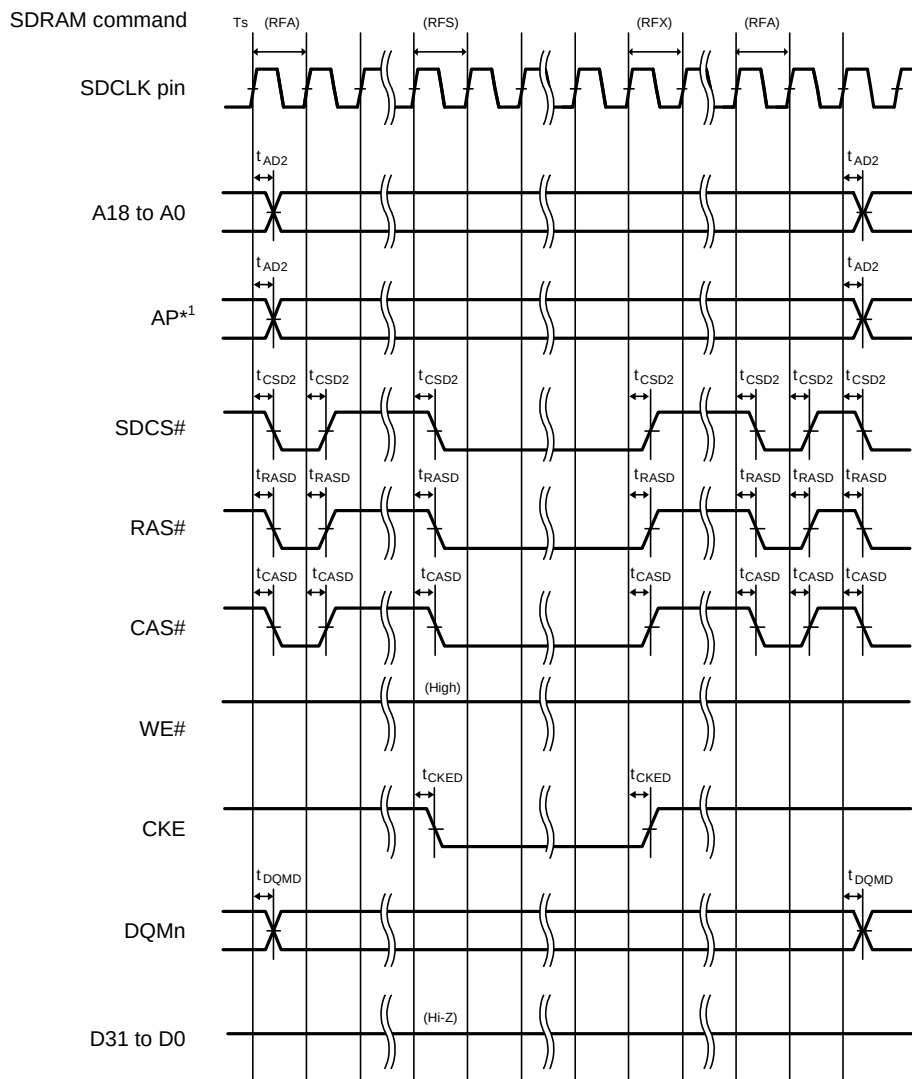


Figure 5.29 SDRAM Space Self-Refresh Bus Timing

Table 5.34 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, T_a = T_{opr}
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions	
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{PBcyc}	Figure 5.46	
	SCK clock cycle input (slave)		8	65536			
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}		
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}		
	SCK clock rise/fall time	$t_{\text{SPCKr}}, t_{\text{SPCKf}}$	—	20	ns		
	Data input setup time	t_{SU}	33.3	—	ns	Figure 5.47 to Figure 5.52	
	Data input hold time	t_{H}	33.3	—	ns		
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}		
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}		
	Data output delay time	t_{OD}	—	33.3	ns		
	Data output hold time	t_{OH}	−10	—	ns		
	Data rise/fall time	$t_{\text{Dr}}, t_{\text{Df}}$	—	16.6	ns		
	SS input rise/fall time	$t_{\text{SSLr}}, t_{\text{SSLf}}$	—	16.6	ns		
	Slave access time	t_{SA}	—	5	t_{PBcyc}		Figure 5.51, Figure 5.52
	Slave output release time	t_{REL}	—	5	t_{PBcyc}		

Note 1. $t_{PB_{Cyc}}$: PCLKB cycle

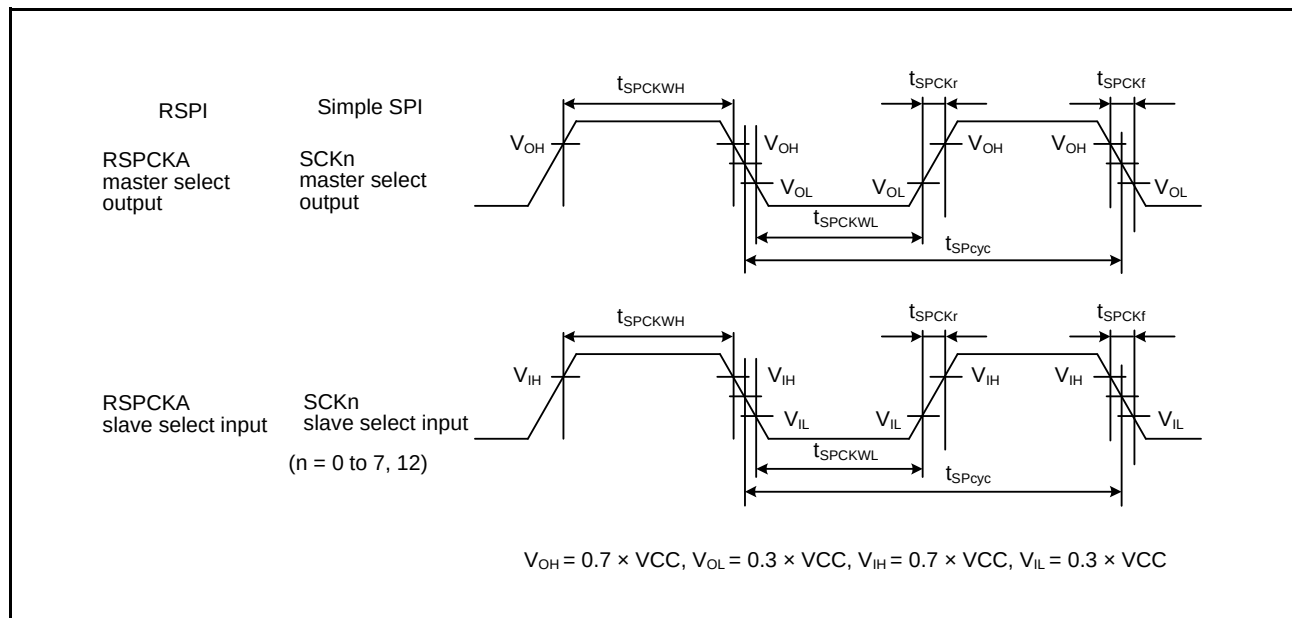


Figure 5.46 RSPI Clock Timing and Simple SPI Clock Timing

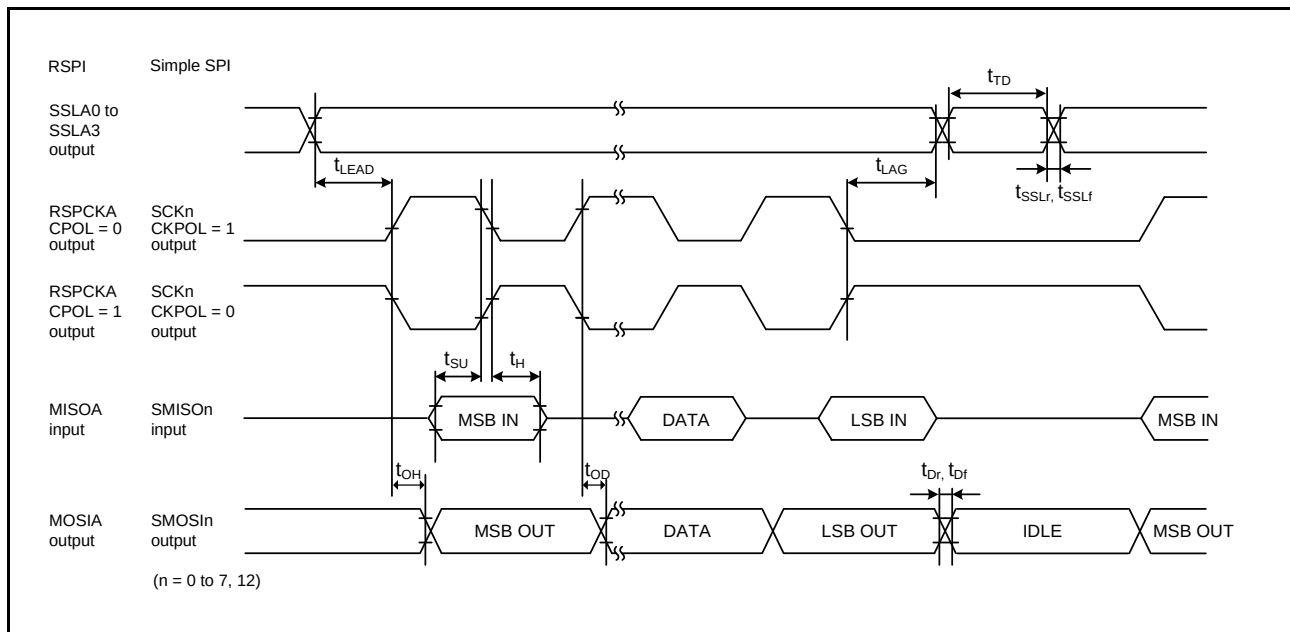


Figure 5.49 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

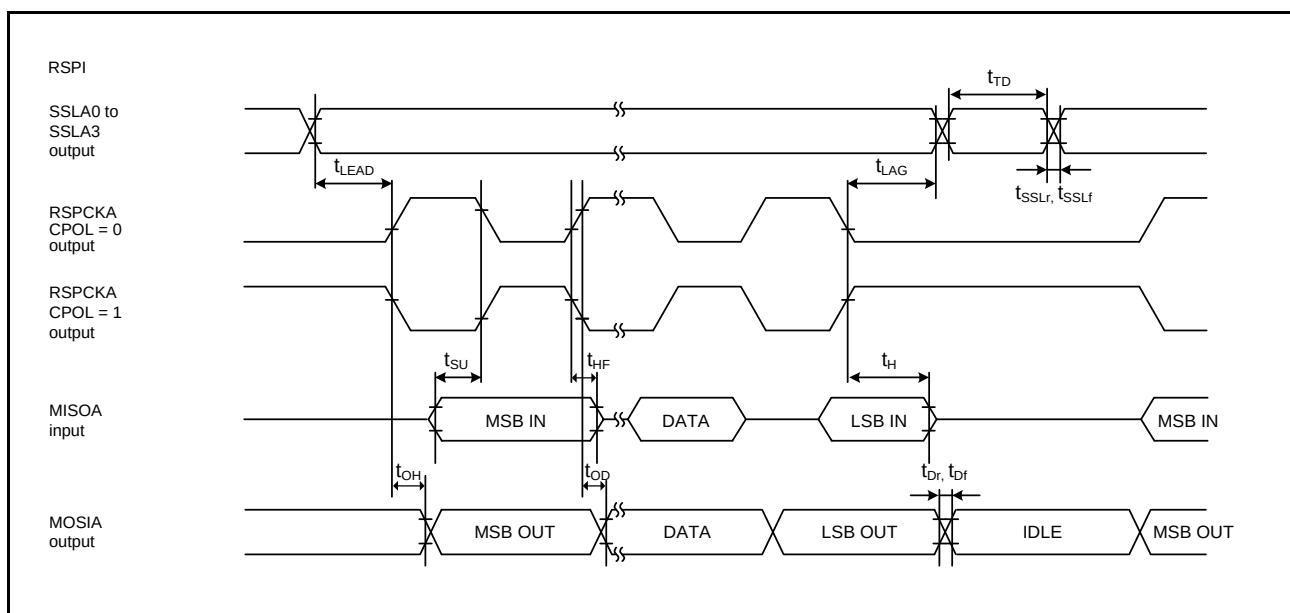


Figure 5.50 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKB Division Ratio Set to 1/2)

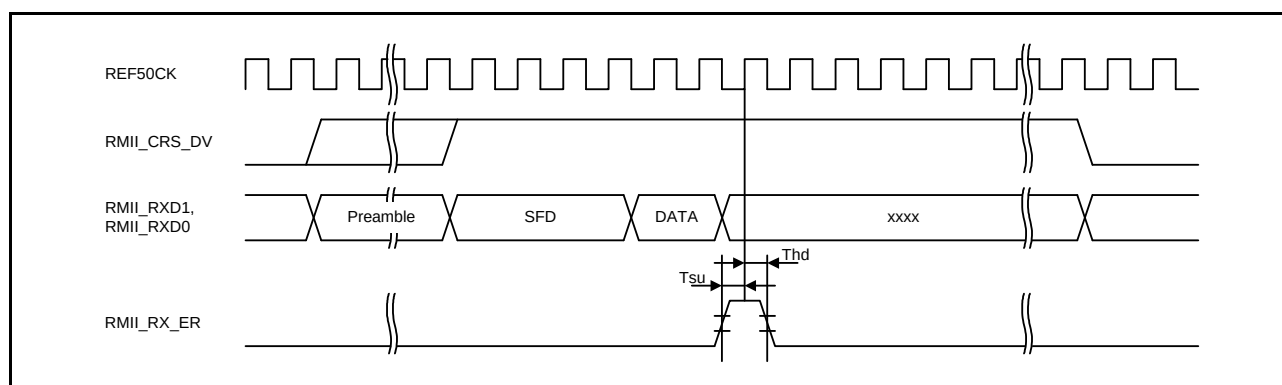


Figure 5.65 RMII Reception Timing (Error Occurrence)

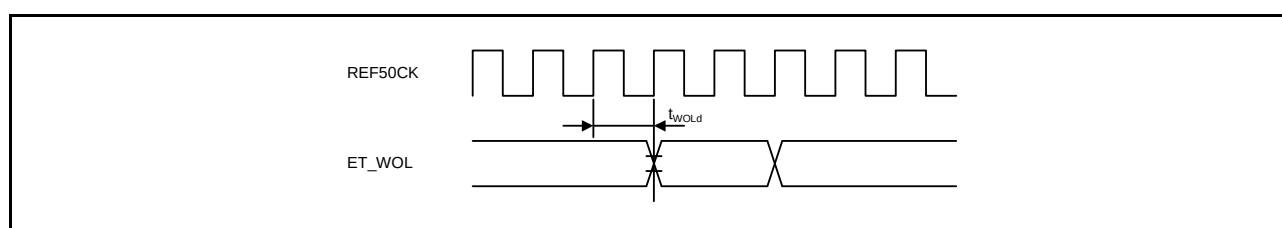


Figure 5.66 WOL Output Timing (RMII)

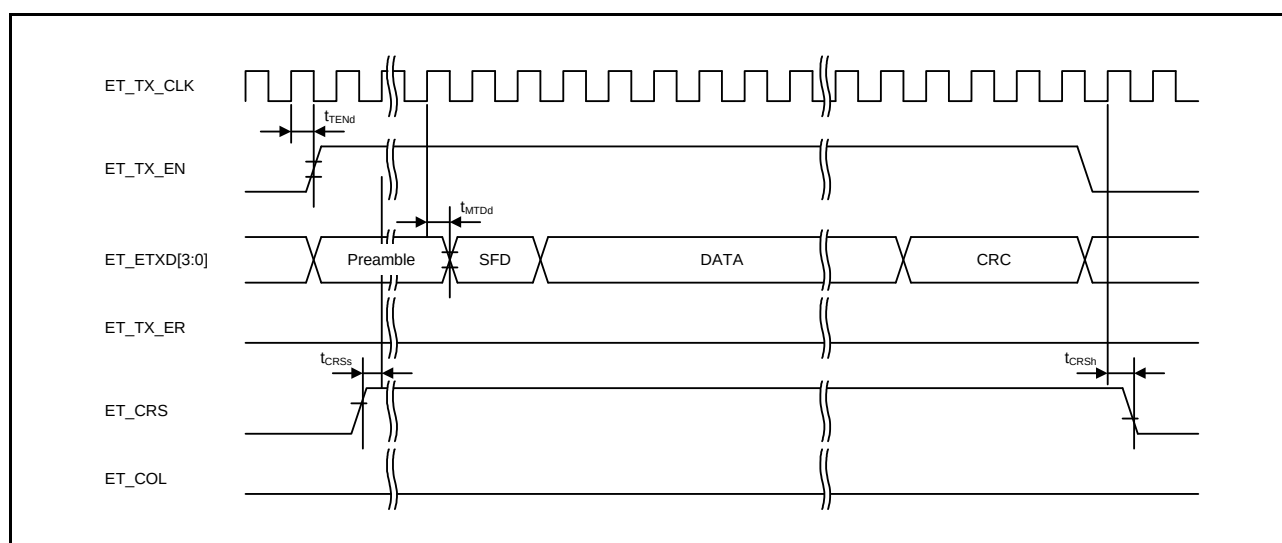


Figure 5.67 MII Transmission Timing (Normal Operation)