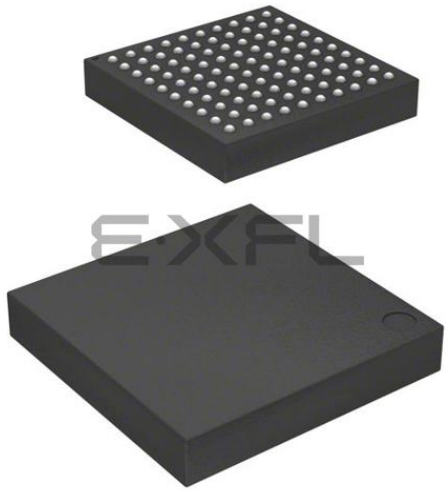

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RXv2 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 4MB (4M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 552K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFLGA |
| Supplier Device Package | 100-TFLGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlddlj-21 |

**Table 1.1 Outline of Specifications (2/9)**

| Classification | Module/Function | Description |
|---|---|---|
| Clock | Clock generation circuit | • Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator<br>• The peripheral module clocks can be set to frequencies above that of the system clock.<br>• Main-clock oscillation stoppage detection<br>• Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz<br>Peripheral modules of MTU3, GPT, RSPI, SCIFA, USBA, ETHERC, EPTPC, EDMAC, and AES run in synchronization with PCLKA, which operates at up to 120 MHz.<br>Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz<br>ADCLK in the SD12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz<br>ADCLK in the SD12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz<br>Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz<br>Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz<br>• Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit |
| Reset | | Nine types of reset<br>• RES# pin reset: Generated when the RES# pin is driven low.<br>• Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises.<br>• Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls.<br>• Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby.<br>• Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs.<br>• Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs.<br>• Software reset: Generated by register setting. |
| Power-on reset | | If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled. |
| Voltage detection circuit (LVDA) | | Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or internal interrupt.<br>• Voltage detection circuit 0<br>Capable of generating an internal reset<br>The option-setting memory can be used to select enabling or disabling of the reset.<br>Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, and 2.80 V)<br>• Voltage detection circuits 1 and 2<br>Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, and 2.85 V)<br>Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency)<br>Capable of generating an internal reset<br>• Two types of timing are selectable for release from reset<br>An internal interrupt can be requested.<br>• Detection of voltage rising above and falling below thresholds is selectable.<br>• Maskable or non-maskable interrupt is selectable<br>Voltage detection monitoring<br>Event linking |
| Low power consumption | Low power consumption facilities | • Module stop function<br>• Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| | Battery backup function | • When the voltage on the VCC pin drops, battery power from the VBATT pin is supplied to keep the real-time clock (RTC) operating. |

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products (1/3)**

| Group | Part No. | Package | Code Flash Memory Capacity | RAM Capacity | Data Flash Memory Capacity | Operating Frequency (Max.) | Encryption Module | SDHI |
|---|---|---|---|---|---|---|---|---|
| RX64M | R5F564MLCDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFC | PLQP0176KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFC | PLQP0176KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFC | PLQP0176KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MFCDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MFDDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MFGDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MFHDFC | PLQP0176KB-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MLCDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFB | PLQP0144KA-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFB | PLQP0144KA-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFB | PLQP0144KA-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MFCDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MFDDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MFGDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MFHDFB | PLQP0144KA-A | 2 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MLCDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MLDDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MLGDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MLHDFP | PLQP0100KB-A | 4 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MJCDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MJDDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MJGDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MJHDFP | PLQP0100KB-A | 3 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |
| | R5F564MGCDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Not supported |
| | R5F564MGDDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Not supported | Available |
| | R5F564MGGDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Not supported |
| | R5F564MGHDFP | PLQP0100KB-A | 2.5 Mbytes | 512 Kbytes | 64 Kbytes | 120 MHz | Available | Available |

**Table 1.4 Pin Functions (3/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| General-purpose PWM timer | GTIOC0A-A/GTIOC0A-B/ GTIOC0A-C/GTIOC0A-D/ GTIOC0A-E, GTIOC0B-A/GTIOC0B-B/ GTIOC0B-C/GTIOC0B-D/ GTIOC0B-E | I/O | GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC1A-A/GTIOC1A-B/ GTIOC1A-C/GTIOC1A-D/ GTIOC1A-E, GTIOC1B-A/GTIOC1B-B/ GTIOC1B-C/GTIOC1B-D/ GTIOC1B-E | I/O | GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC2A-A/GTIOC2A-B/ GTIOC2A-C/GTIOC2A-D/ GTIOC2A-E, GTIOC2B-A/GTIOC2B-B/ GTIOC2B-C/GTIOC2B-D/ GTIOC2B-E | I/O | GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins |
| | GTIOC3A-D/GTIOC3A-E, GTIOC3B-D/GTIOC3B-E | I/O | GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins |
| | GTETRG-B/GTETRG-C/ GTETRG-D | Input | External trigger input pin for GPT0 to GPT3 |
| 16-bit timer pulse unit | TIOCA0, TIOCB0 TIOCC0, TIOCD0 | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | TIOCA1, TIOCB1 | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins |
| | TIOCA2, TIOCB2 | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins |
| | TIOCA3, TIOCB3 TIOCC3, TIOCD3 | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins |
| | TIOCA4, TIOCB4 | I/O | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins |
| | TIOCA5, TIOCB5 | I/O | The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins |
| | TCLKA, TCLKB TCLKC, TCLKD | Input | Input pins for external clock signals or for phase counting mode clock signals |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals |
| 8-bit timer | TMO0 to TMO3 | Output | Compare match output pins |
| | TMCI0 to TMCI3 | Input | Input pins for external clocks to be input to the counter |
| | TMRI0 to TMRI3 | Input | Input pins for the counter reset |
| Compare match timer W | TIC0 to TIC3 | Input | Input pins for CMTW |
| | TOC0 to TOC3 | Output | Output pins for CMTW |

**Table 1.4 Pin Functions (6/8)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| USB 2.0 host/function module | VCC_USB, VCC_USBA | Input | Power supply pins |
| | VSS_USB, VSS1_USBA, VSS2_USBA | Input | Ground pins |
| | AVCC_USBA | Input | USBA analog power supply pin |
| | AVSS_USBA | Input | USBA analog ground pin. Short this pin with the PVSS_USBA pin. |
| | PVSS_USBA | Input | USBA PLL circuit ground pin. Short this pin with the AVSS_USBA pin. |
| | USBA_RREF | I/O | USBA reference current supply pin. Connect 2.2 kΩ (±1%) to the AVSS_USBA pin. |
| | USB0_DP, USBA_DP | I/O | Input or output USB transceiver D+ data. |
| | USB0_DM, USBA_DM | I/O | Input or output USB transceiver D- data. |
| | USB0_EXICEN, USBA_EXICEN | Output | Connect to the OTG power IC. |
| | USB0_ID, USBA_ID | Input | Connect to the OTG power IC. |
| | USB0_VBUSEN USBA_VBUSEN | Output | USB VBUS power enable pins |
| | USB0_OVRCURA/ USB0_OVRCURB, USBA_OVRCURA/ USBA_OVRCURB | Input | USB overcurrent pins |
| | USB0_VBUS, USBA_VBUS | Input | USB cable connection/disconnection detection input pins |
| CAN module | CRX0, CRX1-DS, CRX2 | Input | Input pins |
| | CTX0 to CTX2 | Output | Output pins |
| Serial peripheral interface | RSPCKA-A/RSPCKA-B | I/O | Clock input/output pin |
| | MOSIA-A/MOSIA-B | I/O | Inputs or outputs data output from the master |
| | MISOA-A/MISOA-B | I/O | Inputs or outputs data output from the slave |
| | SSLA0-A/SSLA0-B | I/O | Input or output pin for slave selection |
| | SSLA1-A/SSLA1-B to SSLA3-A/SSLA3-B | Output | Output pin for slave selection |
| Quad serial peripheral interface | QSPCLK-A/-B | Output | QSPI clock output pin |
| | QSSL-A/-B | Output | QSPI slave output pin |
| | QMO-A/-B, QIO0-A/-B | I/O | Master transmit data/data 0 |
| | QMI-A/-B, QIO1-A/-B | I/O | Master input data/data 1 |
| | QIO2-A/-B, QIO3-A/-B | I/O | Data 2, data 3 |
| Serial sound interface | SSISCK0, SSISCK1 | I/O | SSI serial bit clock pins |
| | SSIWS0, SSIWS1 | I/O | Word select pins |
| | SSITXD0, SSITXD1 | Output | Serial data output pins |
| | SSIRXD0, SSIRXD1 | Input | Serial data input pins |
| | SSIDATA0, SSIDATA1 | I/O | Serial data input/output pins |
| | AUDIO_MCLK | Input | Master clock pin for audio |

**Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (6/7)**

| Pin Number 176-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus EXDMAC SDRAMC | Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC) | Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI) | Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC) | Interrupt | S12ADC, R12DA |
|---|---|---|---|---|---|---|---|---|
| 143 | | PD7 | D7[A7/D7] | MTIC5U/POE0# | | MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B | IRQ7 | AN107 |
| 144 | | PG1 | D25 | | ET1_RX_ER/ RMII1_RX_ER | | | |
| 145 | | PD6 | D6[A6/D6] | MTIC5V/MTIOC8A/ POE4# | | MMC_D0-B/ SDHI_D0-B/ QIO0-B/ QMO-B | IRQ6 | AN106 |
| 146 | | PG0 | D24 | | ET1_RX_CLK/ REF50CK1 | | | |
| 147 | | PD5 | D5[A5/D5] | MTIC5W/MTIOC8C/ POE10# | | MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B | IRQ5 | AN113 |
| 148 | | PD4 | D4[A4/D4] | MTIOC8B/POE11# | | MMC_CMD-B/ SDHI_CMD-B/ QSSL-B | IRQ4 | AN112 |
| 149 | | P97 | A23/D23 | | ET1_ERXD3 | | | |
| 150 | | PD3 | D3[A3/D3] | MTIOC8D/ GTIOC0A-E/POE8#/ TOC2 | | MMC_D3-B/ SDHI_D3-B/ QIO3-B | IRQ3 | AN111 |
| 151 | VSS | | | | | | | |
| 152 | | P96 | A22/D22 | | ET1_ERXD2 | | | |
| 153 | VCC | | | | | | | |
| 154 | | PD2 | D2[A2/D2] | MTIOC4D/ GTIOC0B-E/TIC2 | CRX0 | MMC_D2-B/ SDHI_D2-B/ QIO2_B | IRQ2 | AN110 |
| 155 | | P95 | A21/D21 | | ET1_ERXD1/ RMII1_RXD1 | | | |
| 156 | | PD1 | D1[A1/D1] | MTIOC4B/ GTIOC1A-E/POE0# | CTX0 | | IRQ1 | AN109 |
| 157 | | P94 | A20/D20 | | ET1_ERXD0/ RMII1_RXD0 | | | |
| 158 | | PD0 | D0[A0/D0] | GTIOC1B-E/POE4# | | | IRQ0 | AN108 |
| 159 | | P93 | A19/D19 | POE0# | ET1_LINKSTA/CTS7#/ RTS7#/SS7# | | | AN117 |
| 160 | | P92 | A18/D18 | POE4# | ET1_CRS/ RMII1_CRS_DV/ RXD7/SMISO7/SSCL7 | | | AN116 |
| 161 | | P91 | A17/D17 | | ET1_COL/SCK7 | | | AN115 |
| 162 | VSS | | | | | | | |
| 163 | | P90 | A16/D16 | | ET1_RX_DV/ TXD7/SMOSI7/SSDA7 | | | AN114 |
| 164 | VCC | | | | | | | |
| 165 | | P47 | | | | | IRQ15-DS | AN007 |
| 166 | | P46 | | | | | IRQ14-DS | AN006 |
| 167 | | P45 | | | | | IRQ13-DS | AN005 |
| 168 | | P44 | | | | | IRQ12-DS | AN004 |
| 169 | | P43 | | | | | IRQ11-DS | AN003 |
| 170 | | P42 | | | | | IRQ10-DS | AN002 |
| 171 | | P41 | | | | | IRQ9-DS | AN001 |
| 172 | VREFL0 | | | | | | | |

## 4.1 I/O Register Addresses (Address Order)

**Table 4.1 List of I/O Registers (Address Order) (1 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 0000h | SYSTEM | Mode Monitor Register | MDMONR | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0002h | SYSTEM | Mode Status Register | MDSR | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0006h | SYSTEM | System Control Register 0 | SYSCR0 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0008h | SYSTEM | System Control Register 1 | SYSCR1 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 000Ch | SYSTEM | Standby Control Register | SBYCR | 16 | 16 | 3 ICLK | | Low Power Consumption |
| 0008 0010h | SYSTEM | Module Stop Control Register A | MSTPCRA | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0014h | SYSTEM | Module Stop Control Register B | MSTPCRB | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0018h | SYSTEM | Module Stop Control Register C | MSTPCRC | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 001Ch | SYSTEM | Module Stop Control Register D | MSTPCRD | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0020h | SYSTEM | System Clock Control Register | SCKCR | 32 | 32 | 3 ICLK | | Clock Generation Circuit |
| 0008 0024h | SYSTEM | System Clock Control Register 2 | SCKCR2 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0026h | SYSTEM | System Clock Control Register 3 | SCKCR3 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0028h | SYSTEM | PLL Control Register | PLLCR | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 002Ah | SYSTEM | PLL Control Register 2 | PLLCR2 | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0030h | SYSTEM | External Bus Clock Control Register | BCKCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0032h | SYSTEM | Main Clock Oscillator Control Register | MOSCCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0033h | SYSTEM | Sub-Clock Oscillator Control Register | SOSCCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0034h | SYSTEM | Low-Speed On-Chip Oscillator Control Register | LOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |

**Table 4.1 List of I/O Registers (Address Order) (48 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 0440h | PTPEDMAC | Missed-Frame Counter Register | RMFCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0448h | PTPEDMAC | Transmit FIFO Threshold Register | TFTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0450h | PTPEDMAC | FIFO Depth Register | FDR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0458h | PTPEDMAC | Receive Method Control Register | RMCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0464h | PTPEDMAC | Transmit FIFO Underflow Counter | TFUCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0468h | PTPEDMAC | Receive FIFO Overflow Counter | RFOCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0470h | PTPEDMAC | Flow Control Start FIFO Threshold Setting Register | FCFTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0478h | PTPEDMAC | Receive Data Padding Insert Register | RPADIR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 047Ch | PTPEDMAC | Transmit Interrupt Setting Register | TRIMD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 04C8h | PTPEDMAC | Receive Buffer Write Address Register | RBWAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 04CCh | PTPEDMAC | Receive Descriptor Fetch Address Register | RDFAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 04D4h | PTPEDMAC | Transmit Buffer Read Address Register | TBRAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 04D8h | PTPEDMAC | Transmit Descriptor Fetch Address Register | TDFAR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | EDMACa |
| 000C 0500h | EPTPC | PTP Reset Register | PTRSTR | 32 | 32 | 3, 4 PCLKA | 2, 3 ICLK | EPTPC |
| 000C 0504h | EPTPC | STCA Clock Select Register | STCSELR | 32 | 32 | 3, 4 PCLKA | 2, 3 ICLK | EPTPC |
| 000C 1200h | MTU3 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1201h | MTU4 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1202h | MTU3 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1203h | MTU4 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1204h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1205h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1206h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1207h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1208h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1209h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 120Ah | MTU | Timer Output Master Enable Register A | TOERA | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 120Dh | MTU | Timer Gate Control Register A | TGCRA | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 120Eh | MTU | Timer Output Control Register 1A | TOCR1A | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 120Fh | MTU | Timer Output Control Register 2A | TOCR2A | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1210h | MTU3 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1212h | MTU4 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1214h | MTU | Timer Cycle Data Register A | TCDRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1216h | MTU | Timer Dead Time Data Register A | TDDRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1218h | MTU3 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 121Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 121Ch | MTU4 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 121Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1220h | MTU | Timer Subcounter A | TCNTSA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1222h | MTU | Timer Cycle Buffer Register A | TCBRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1224h | MTU3 | Timer General Register C | TGRC | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1226h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1228h | MTU4 | Timer General Register C | TGRC | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (50 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1406h | MTU2 | Timer Counter | TCNT | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1408h | MTU2 | Timer General Register A | TGRA | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 140Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 140Ch | MTU2 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1600h | MTU8 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1601h | MTU8 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1602h | MTU8 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1603h | MTU8 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1604h | MTU8 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1606h | MTU8 | Timer Control Register 2 | TCR2 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1608h | MTU8 | Timer Counter | TCNT | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 160Ch | MTU8 | Timer General Register A | TGRA | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1610h | MTU8 | Timer General Register B | TGRB | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1614h | MTU8 | Timer General Register C | TGRC | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1618h | MTU8 | Timer General Register D | TGRD | 32 | 32 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A00h | MTU6 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A01h | MTU7 | Timer Control Register | TCR | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A02h | MTU6 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A03h | MTU7 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A04h | MTU6 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A05h | MTU6 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A06h | MTU7 | Timer I/O Control Register H | TIORH | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A07h | MTU7 | Timer I/O Control Register L | TIORL | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A08h | MTU6 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A09h | MTU7 | Timer Interrupt Enable Register | TIER | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A0Ah | MTU | Timer Output Master Enable Register B | TOERB | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |
| 000C 1A0Eh | MTU | Timer Output Control Register 1B | TOCR1B | 8 | 8 | 5, 6 PCLKA | 2, 3 ICLK | MTU3a |

**Table 4.1 List of I/O Registers (Address Order) (54 / 67)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 21C2h | GPT1 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2200h | GPT2 | General PWM Timer I/O Control Register | GTIOR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2202h | GPT2 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2204h | GPT2 | General PWM Timer Control Register | GTCR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2206h | GPT2 | General PWM Timer Buffer Enable Register | GTBER | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2208h | GPT2 | General PWM Timer Count Direction Register | GTUDC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 220Ah | GPT2 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 220Ch | GPT2 | General PWM Timer Status Register | GTST | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 220Eh | GPT2 | General PWM Timer Counter | GTCNT | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2210h | GPT2 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2212h | GPT2 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2214h | GPT2 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2216h | GPT2 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2218h | GPT2 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 221Ah | GPT2 | General PWM Timer Compare Capture Register F | GTCCRF | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 221Ch | GPT2 | General PWM Timer Cycle Setting Register | GTPR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 221Eh | GPT2 | General PWM Timer Cycle Setting Buffer Register | GTPBR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2220h | GPT2 | General PWM Timer Cycle Setting Double-Buffer Register | GTPDBR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2224h | GPT2 | A/D Converter Start Request Timing Register A | GTADTRA | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2226h | GPT2 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2228h | GPT2 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 222Ch | GPT2 | A/D Converter Start Request Timing Register B | GTADTRB | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 222Eh | GPT2 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2230h | GPT2 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2234h | GPT2 | General PWM Timer Output Negate Control Register | GTONCR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2236h | GPT2 | General PWM Timer Dead Time Control Register | GTDTCR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2238h | GPT2 | General PWM Timer Dead Time Value Register U | GTDVU | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 223Ah | GPT2 | General PWM Timer Dead Time Value Register D | GTDVD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 223Ch | GPT2 | General PWM Timer Dead Time Buffer Register U | GTDBU | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 223Eh | GPT2 | General PWM Timer Dead Time Buffer Register D | GTDBD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2240h | GPT2 | General PWM Timer Output Protection Function Status Register | GTSOS | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2242h | GPT2 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2280h | GPT3 | General PWM Timer I/O Control Register | GTIOR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2282h | GPT3 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2284h | GPT3 | General PWM Timer Control Register | GTCR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2286h | GPT3 | General PWM Timer Buffer Enable Register | GTBER | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2288h | GPT3 | General PWM Timer Count Direction Register | GTUDC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 228Ah | GPT3 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 228Ch | GPT3 | General PWM Timer Status Register | GTST | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 228Eh | GPT3 | General PWM Timer Counter | GTCNT | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2290h | GPT3 | General PWM Timer Compare Capture Register A | GTCCRA | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2292h | GPT3 | General PWM Timer Compare Capture Register B | GTCCRB | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2294h | GPT3 | General PWM Timer Compare Capture Register C | GTCCRC | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2296h | GPT3 | General PWM Timer Compare Capture Register D | GTCCRD | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |
| 000C 2298h | GPT3 | General PWM Timer Compare Capture Register E | GTCCRE | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | GPTA |

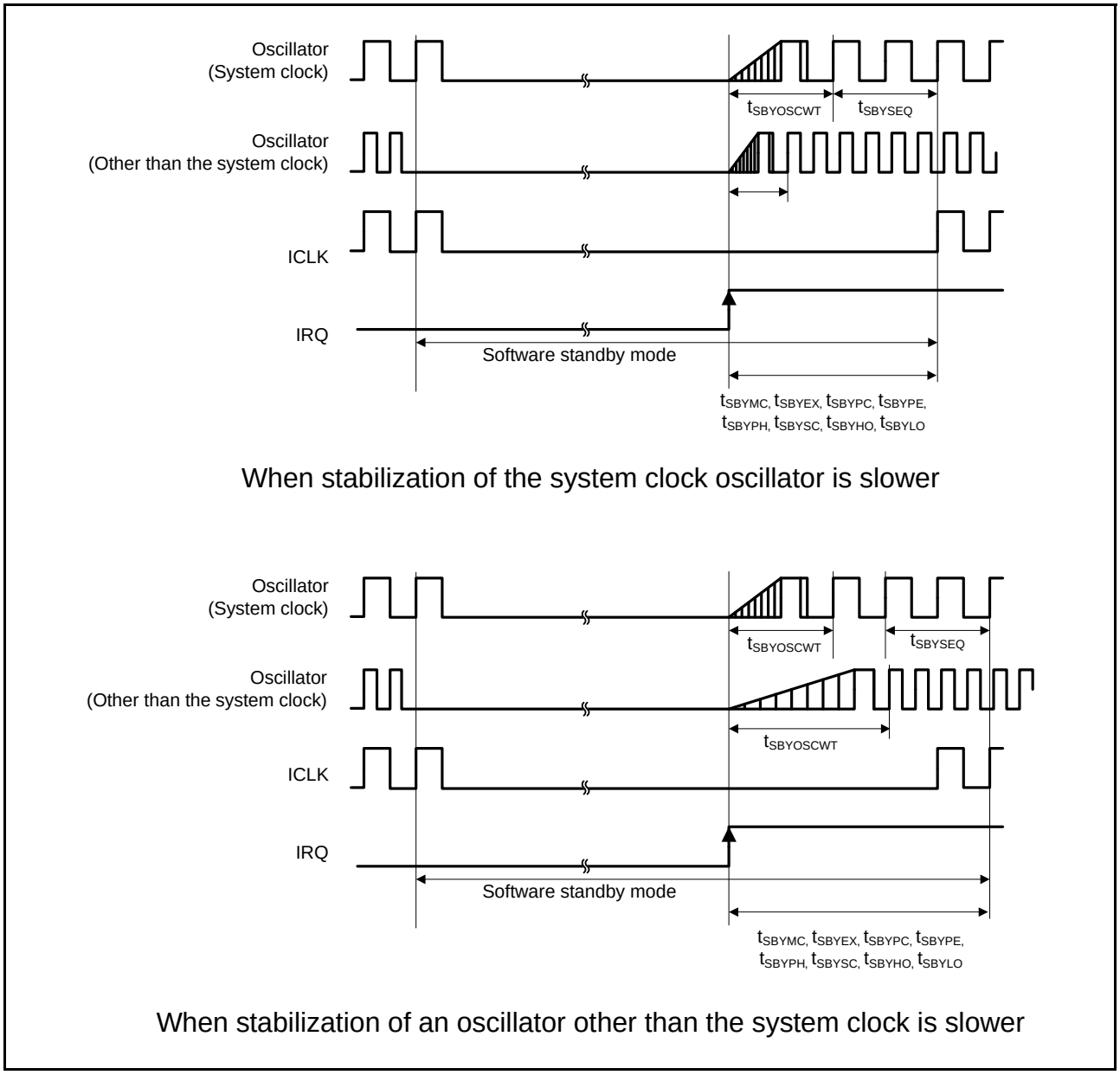



**Figure 5.12 Software Standby Mode Cancellation Timing**

## 5.3.4 Control Signal Timing

**Table 5.20 Control Signal Timing**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PLCKB = 8 to 60 MHz, $T_a = T_{opr}$

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | — | — | ns | $t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.14 |
| | | $t_{PBcyc} \times 2$ | — | — | ns | $t_{PBcyc} \times 2 > 200$ ns, Figure 5.14 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | — | ns | $t_{PBcyc} \times 2 \leq 200$ ns, Figure 5.15 |
| | | $t_{PBcyc} \times 2$ | — | — | ns | $t_{PBcyc} \times 2 > 200$ ns, Figure 5.15 |

Note 1. $t_{PBcyc}$: PCLKB cycle

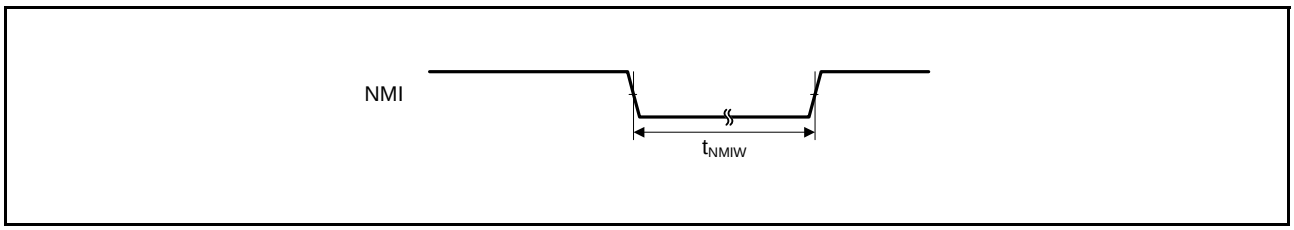



**Figure 5.14 NMI Interrupt Input Timing**

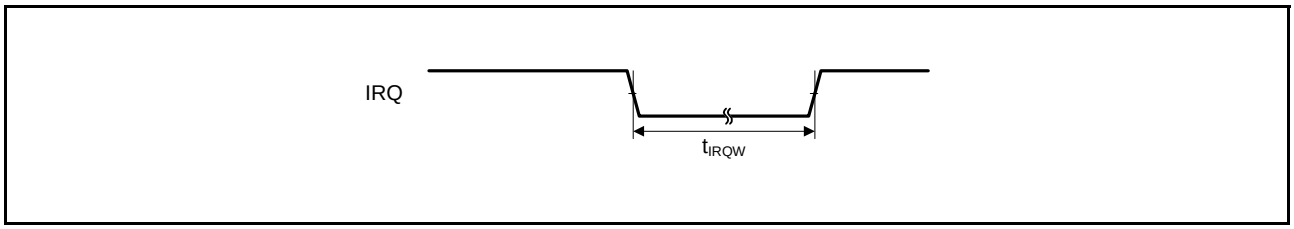



**Figure 5.15 IRQ Interrupt Input Timing**

### Table 5.25 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| TMR | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$, $t_{TMCWL}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.36 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

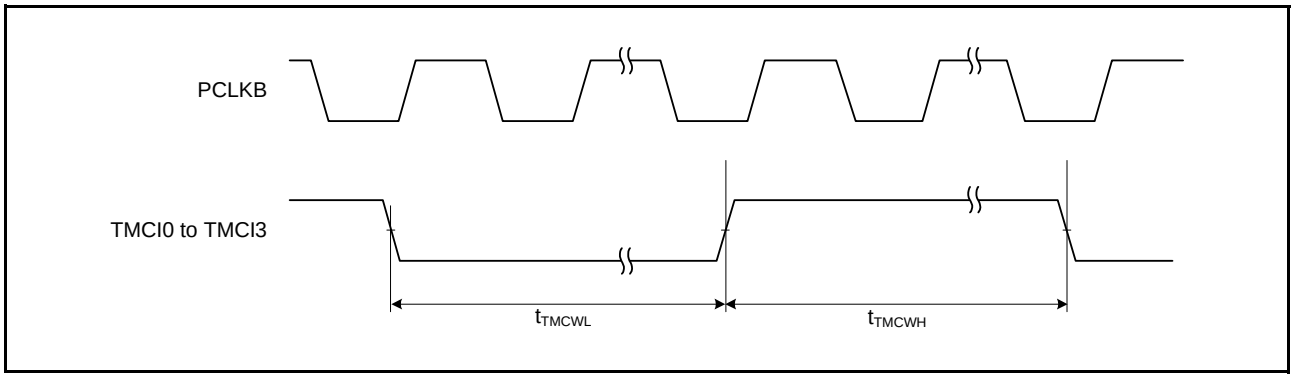



**Figure 5.36 TMR Clock Input Timing**

### Table 5.26 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, C = 30 pF
High-drive output is selected by the driving ability control register.

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| CMTW | Input capture input pulse width | Single-edge setting | $t_{CMTWTICW}$ | 1.5 | — | $t_{PBcyc}$ | Figure 5.37 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. $t_{PBcyc}$: PCLKB cycle

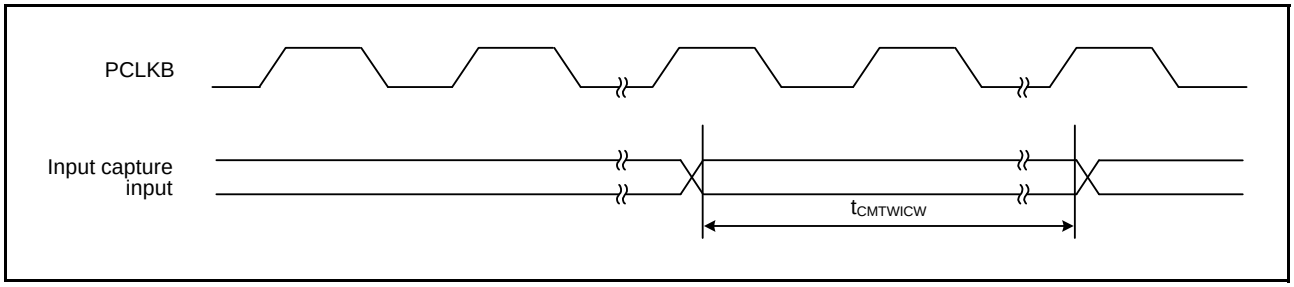



**Figure 5.37 CMTW Input Capture Input Timing**

### Table 5.37 RIIC Timing (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$
High-drive output is selected by the driving ability control register.

| Item | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 240 | — | ns | Figure 5.56 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 120 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 120 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 20 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 550 | pF | |
| Simple IIC (Standard-mode) | SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 250 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| Simple IIC (Fast-mode) | SCL, SDA input rise time | $t_{Sr}$ | — | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 4 × $t_{PBcyc}$ | ns | |
| | Data input setup time | $t_{SDAS}$ | 100 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICϕ) cycle, $t_{PBcyc}$: PCLKB cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

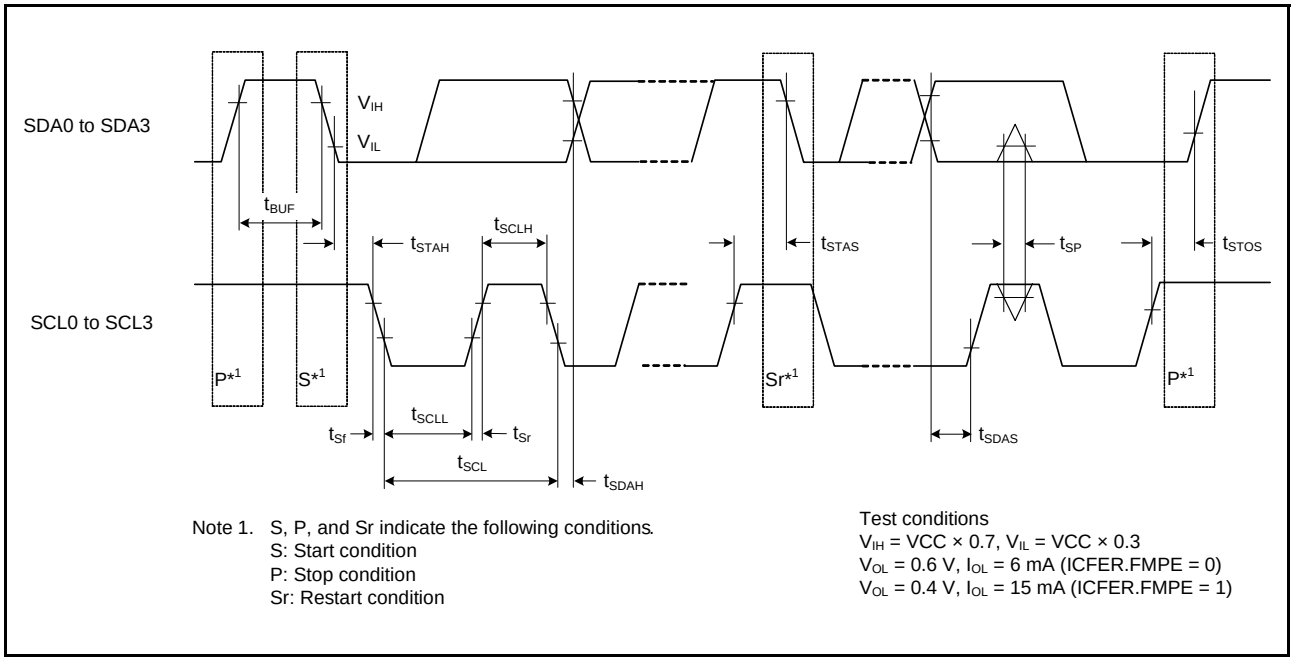



**Figure 5.56 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing**

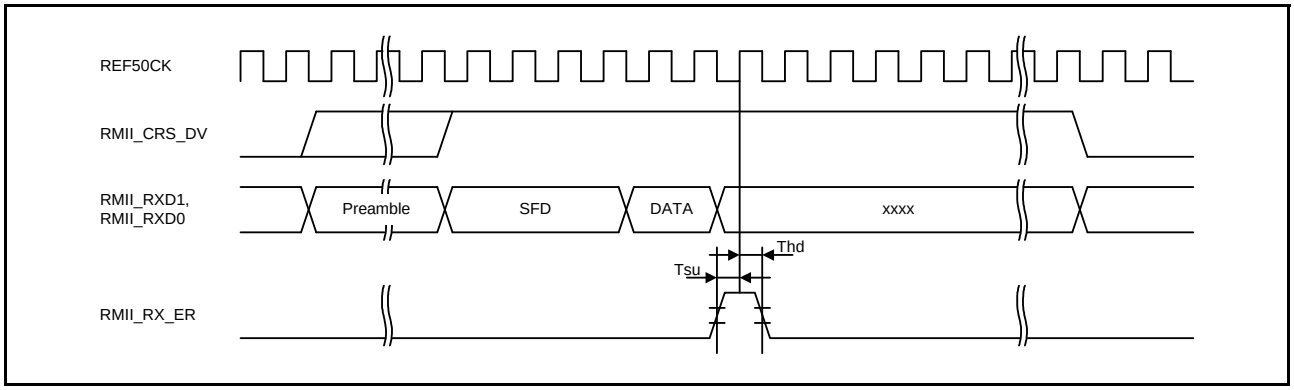



**Figure 5.65 RMII Reception Timing (Error Occurrence)**

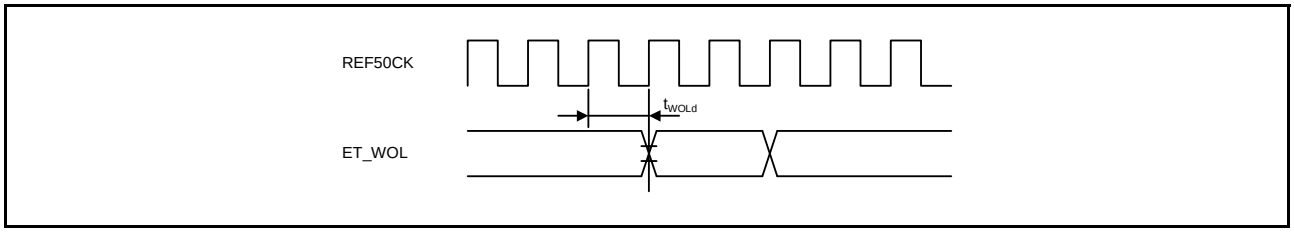



**Figure 5.66 WOL Output Timing (RMII)**

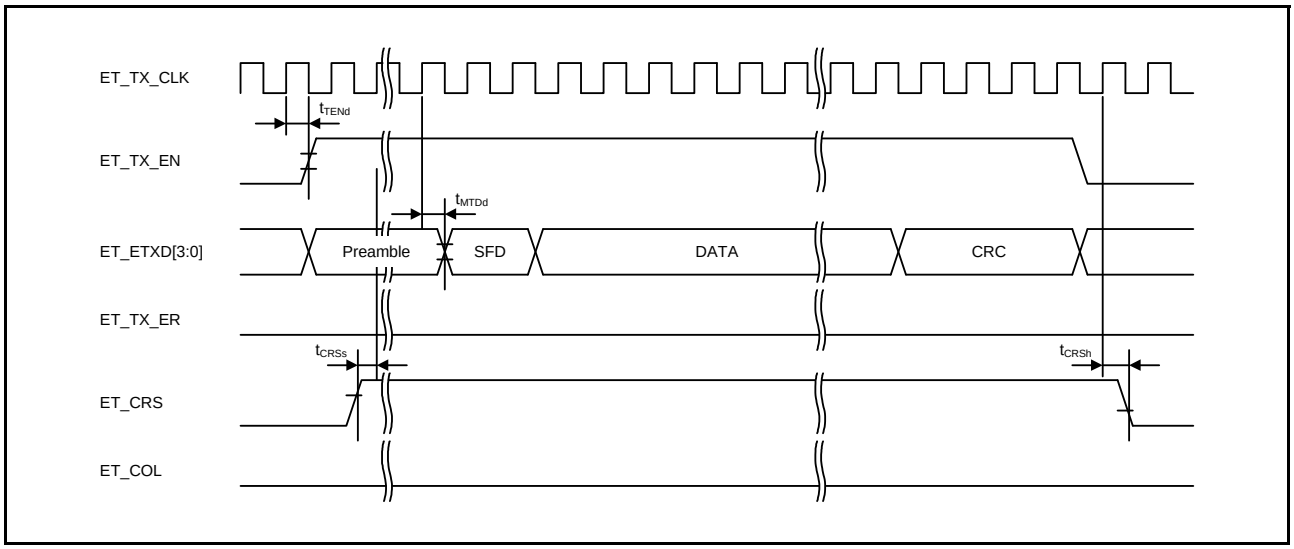



**Figure 5.67 MII Transmission Timing (Normal Operation)**

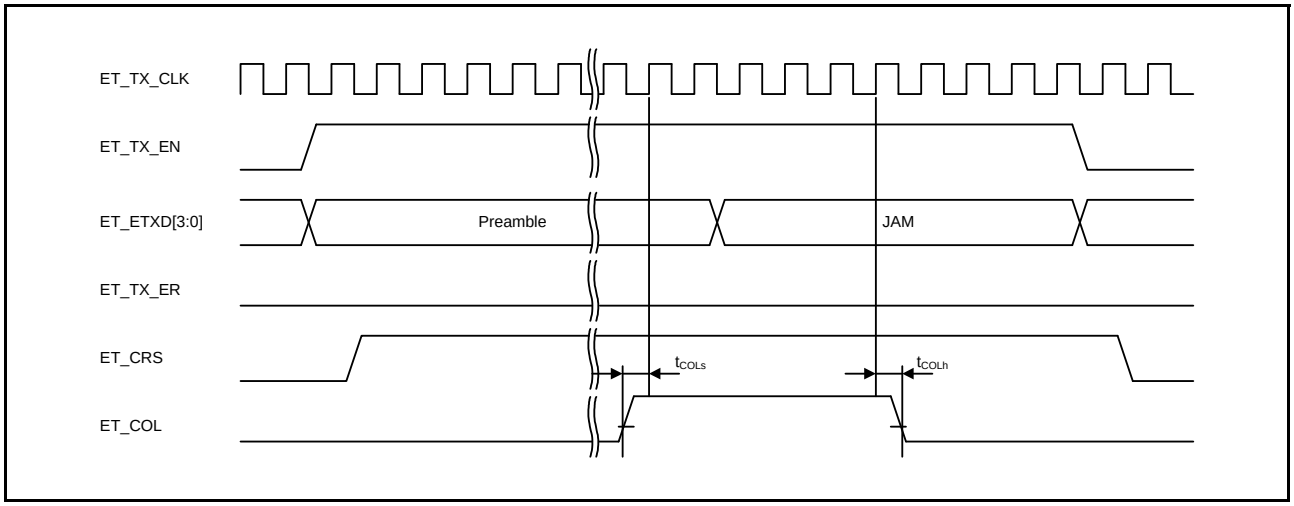



**Figure 5.68 MII Transmission Timing (Conflict Occurrence)**

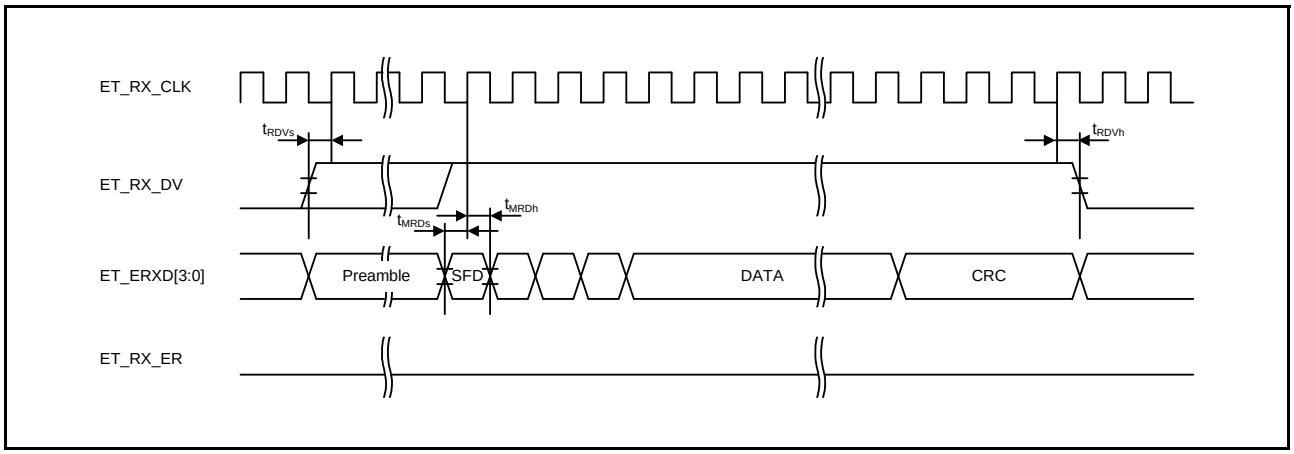



**Figure 5.69 MII Reception Timing (Normal Operation)**

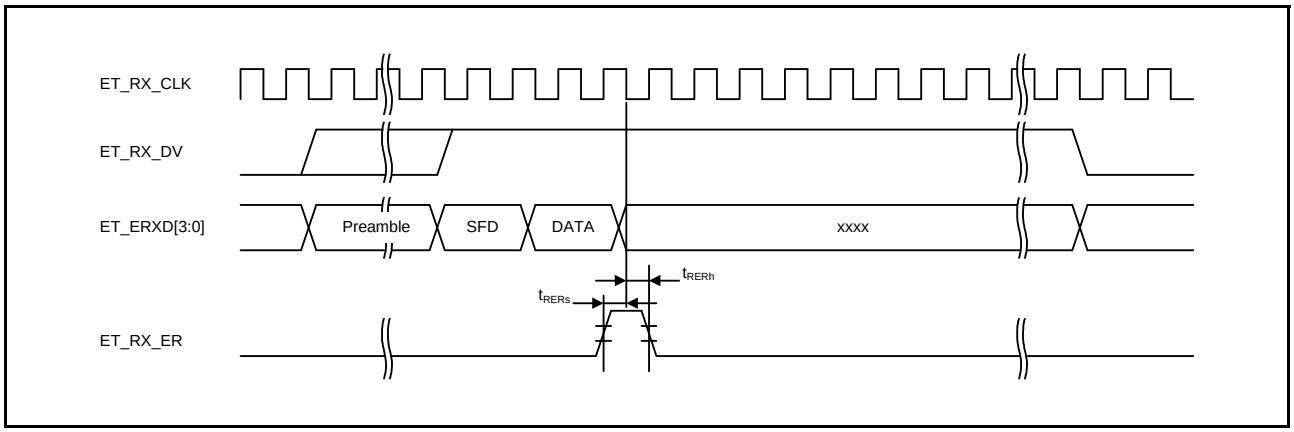



**Figure 5.70 MII Reception Timing (Error Occurrence)**

## 5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

**Table 5.50 Power-on Reset Circuit and Voltage Detection Circuit Characteristics**

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | Low power consumption function disabled*1 | $V_{POR}$ | 2.5 | 2.6 | 2.7 | V | Figure 5.79 |
| | | Low power consumption function enabled*2 | | 2.0 | 2.35 | 2.7 | | |
| | Voltage detection circuit (LVD0) | | $V_{det0\_1}$ | 2.84 | 2.94 | 3.04 | | Figure 5.80 |
| | | | $V_{det0\_2}$ | 2.77 | 2.87 | 2.97 | | |
| | | | $V_{det0\_3}$ | 2.70 | 2.80 | 2.90 | | |
| | Voltage detection circuit (LVD1) | | $V_{det1\_1}$ | 2.89 | 2.99 | 3.09 | | Figure 5.81 |
| | | | $V_{det1\_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det1\_3}$ | 2.75 | 2.85 | 2.95 | | |
| | Voltage detection circuit (LVD2) | | $V_{det2\_1}$ | 2.89 | 2.99 | 3.09 | | Figure 5.82 |
| | | | $V_{det2\_2}$ | 2.82 | 2.92 | 3.02 | | |
| | | | $V_{det2\_3}$ | 2.75 | 2.85 | 2.95 | | |
| Internal reset time | Power-on reset time | | $t_{POR}$ | — | 4.6 | — | ms | Figure 5.79 |
| | LVD0 reset time | | $t_{LVD0}$ | — | 0.70 | — | | Figure 5.80 |
| | LVD1 reset time | | $t_{LVD1}$ | — | 0.57 | — | | Figure 5.81 |
| | LVD2 reset time | | $t_{LVD2}$ | — | 0.57 | — | | Figure 5.82 |
| Minimum VCC down time | | | $t_{VOFF}$ | 200 | — | — | μs | Figure 5.79, Figure 5.80 |
| Response delay time | | | $t_{det}$ | — | — | 200 | μs | Figure 5.79 to Figure 5.82 |
| LVD operation stabilization time (after LVD is enabled)*3 | | | $T_{d(E-A)}$ | — | — | 10 | μs | Figure 5.81, Figure 5.82 |
| Hysteresis width (LVD1 and LVD2) | | | $V_{LVH}$ | — | 80 | — | mV | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, $V_{det1}$, and $V_{det2}$ for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 3. The voltage of VCC = AVCC0 = AVCC1 when LVD1 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 1 level ($V_{det1\_1, 2, 3}$) selected by the LVDLVLR.LVD1LVL[3:0] bits.
Similarly, the voltage of VCC = AVCC0 = AVCC1 when LVD2 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 2 level ($V_{det2\_1, 2, 3}$) selected by the LVDLVLR.LVD2LVL[3:0] bits.

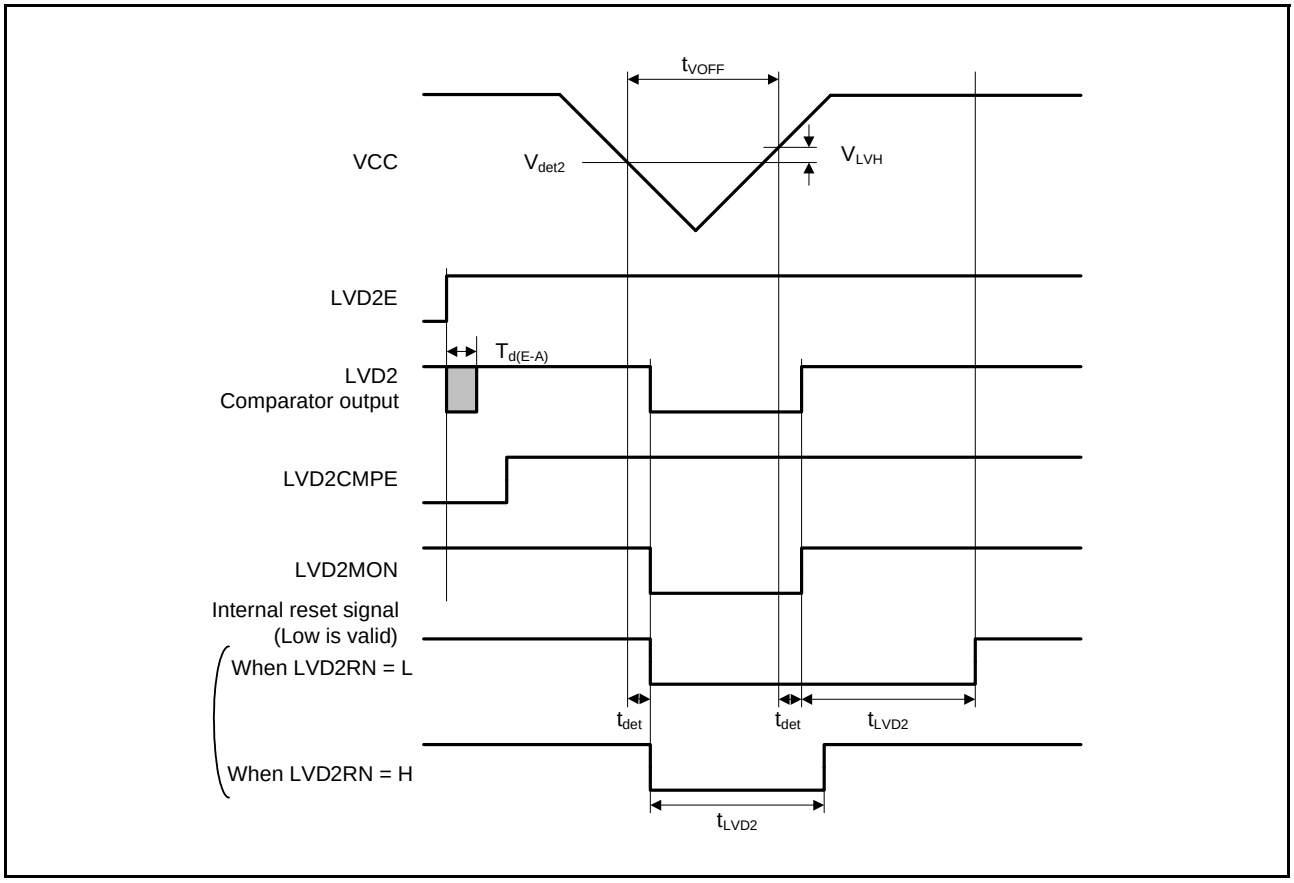



**Figure 5.82 Voltage Detection Circuit Timing ($V_{det2}$)**

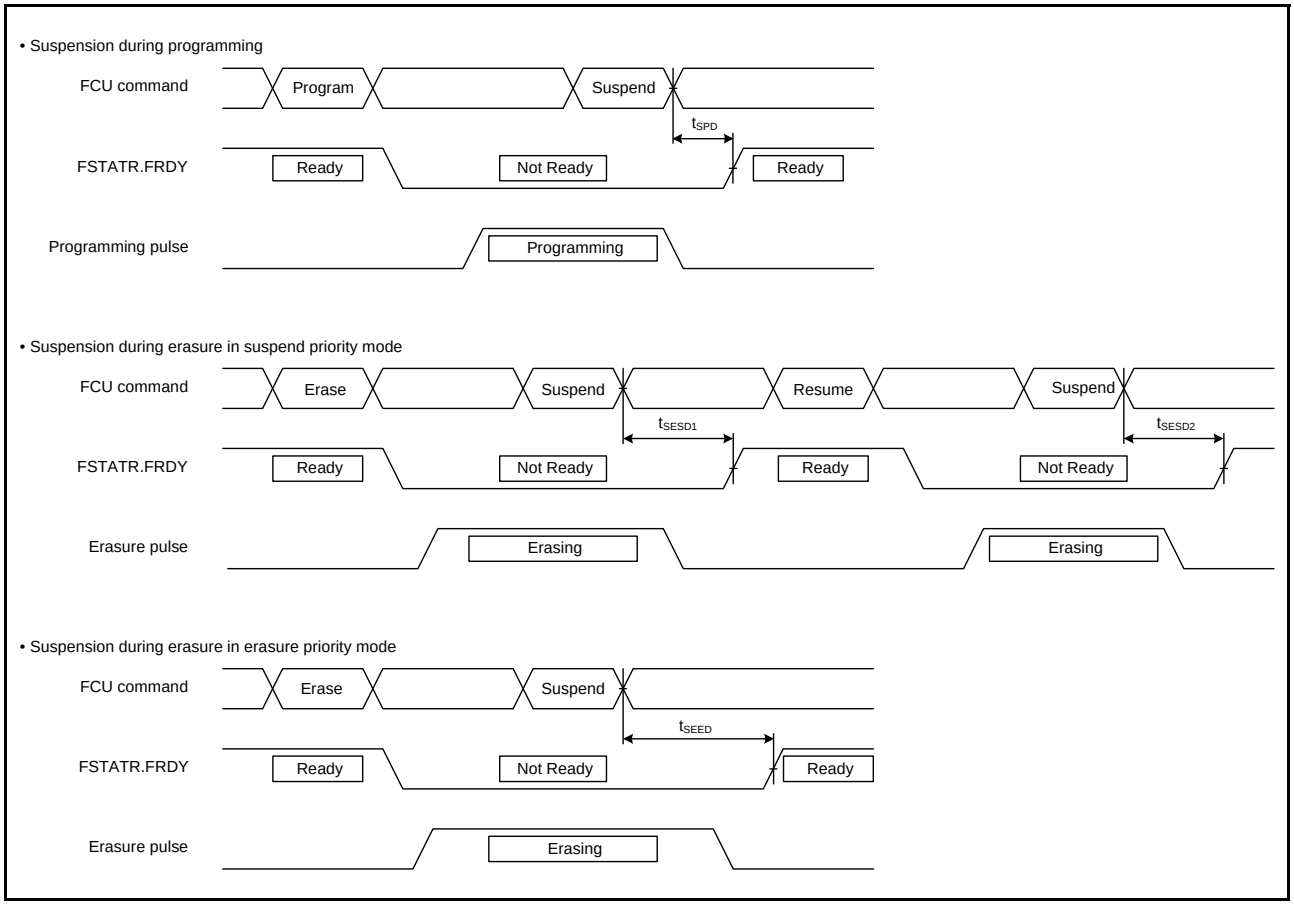
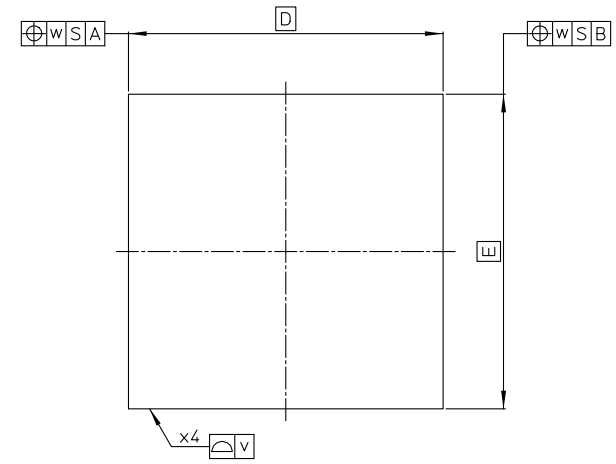
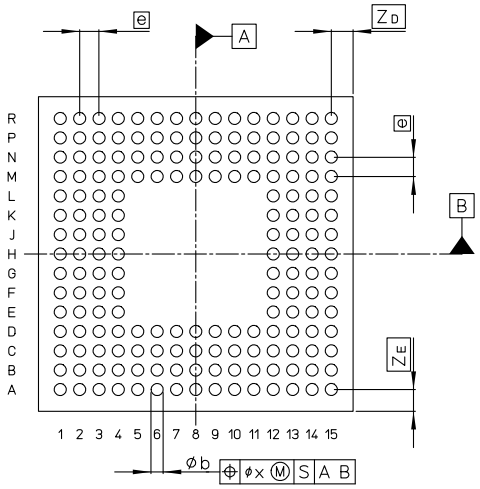



**Figure 5.85 Flash Memory Programming/Erasure Suspension Timing**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-A | BP-176/BP-176V | 0.45g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 13.0 | — |
| E | — | 13.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.90 | — |
| $Z_E$ | — | 0.90 | — |

Figure B 176-Pin LFBGA (PLBG0176GA-A)