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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlgdfc-v1

Table 1.1 Outline of Specifications (4/9)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
Timers	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLKA/32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) • 14 of the signals are available for channel 0, 12 are available for channel 2, 11 are available for channels 1, 3, 4, 6 to 8, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode • Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode • Outputs non-overlapping waveforms for controlling 3-phase inverters • Automatic specification of dead times • PWM duty cycle: Selectable as any value from 0% to 100% • Delay can be applied to requests for A/D conversion. • Non-generation of interrupt requests at peak or trough values of counters can be selected. • Double buffer configuration • Reset synchronous PWM mode • Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU3/GPT's waveform output pins • 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	RX64M Group		
Package	177 Pins, 176 Pins	145 Pins, 144 Pins	100 Pins
DES	Available		
SHA	Available		
RNG	Available		
Event link controller	Available		

Table 1.3 List of Products (3/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX64M	R5F564MFCDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (6/7)

Pin Number				Timer	Communication	Memory Interface Camera Interface		
177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(ETHERC, SCiG, SCiH, RSPI, RIIC, CAN, USB, SSI)	(QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
P2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOC0B/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
P3		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOC0B5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4	
P5					USB0_DP			
P6	AVSS_ USBA							
P7					USBA_DM			
P8		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
P9		P52	RD#		RXD2/SMISO2/ SSCL2			
P10		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR0-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0- A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
P13		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV/	MMC_CD-A/ SDHI_D3-A		
P14		P75	CS5#	PO20	SCK11/RTS11/ ET0_ERXD0/ RMII0_RXD0/	MMC_RES#-A/ SDHI_D2-A		
P15	VCC							
R1		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ USBA_EXICEN/ SSIWS0	PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOC0B3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ USBA_ID/ SSIRXD0	PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOC0B1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
R4		P13	WR2#/BC2#	MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]		IRQ3	ADTRG1#
R5					USB0_DM			
R6	PVSS_ USBA							
R7					USBA_DP			
R8		P11		MTIC5V/TMCI3	SCK2/ USBA_VBUS/ USBA_VBUSEN			
R9		P53*2	BCLK					
R10	VSS							

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMC11	SCK6		IRQ10	AN120
7		P01		TMC10	RXD6/SMISO6/ SSCL6		IRQ9	AN119
8		P00		TMR10	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	NC							
17	TRST#	PF4						
18	MD/FINED							
19	XCIN							
20	XCOUT							
21	RES#							
22	XTAL	P37						
23	VSS							
24	EXTAL	P36						
25	VCC							
26	UPSEL	P35					NMI	
27		P34		MTIOC0A/TMC13/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOC0D/ TMR13/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
30	TMS	PF3						
31	TDI	PF2			RXD1/SMISO1/ SSCL1			
32		P31		MTIOC4D/TMC12/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC		IRQ1-DS	
33		P30		MTIOC4B/TMR13/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ ET1_MDIO		IRQ0-DS	
34	TCK	PF1			SCK1			
35	TDO	PF0			TXD1/SMOSI1/ SSDA1			

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMC1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
K6		P53*1	BCLK					
K7		P51	WR1#/BC1#/ WAIT#		SCK2			
K8	VCC							
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
K10		P76	CS6#	PO22	RXD11/ET0_RX_CLK/ REF50CK0	MMC_CMD-A/ SDHI_CMD-A/ QSSL-A		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
L1		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1	HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ GTIOC0A-B/TIOCD3/ PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SSO#/ SSDA3/SSISCK0	PIXD7		
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
L4		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
L6		P56	EDACK1	MTIOC3C/TIOCA1				
L7		P52	RD#		RXD2/SMISO2/SSCL2			
L8	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRQ-D/TMC11/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
L11		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV	MMC_CD-A/ SDHI_D3-A		
L12		P73	CS3#	PO16	ET0_WOL			
L13	VSS							
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ GTIOC1A-B/TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_MCLK	PIXD6		
M2		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
M3		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (3/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
F6		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D3/TCLKD/ TMO0/PO27/POE11#	SCK6/ET0_RX_ER/ RMII0_RX_ER			
F7		PB2	A10	TIOCC3/TCLKC/ PO26	CTS6#/RTS6#SS6#/ ET0_RX_CLK/ REF50CK0			
F8		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD6/SMISO6/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA-B/ET0_WOL			
F10	VSS							
G1		P33	EDREQ1	MTIOC0D/TIOC0D/ TMR13/PO11/POE4#/ POE11#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS	
G2	TMS	P31		MTIOC4D/TMCI2/ PO9/RTIC1	CTS1#/RTS1#/SS1#		IRQ1-DS	
G3	TDI	P30		MTIOC4B/TMR13/ PO8/RTIC0/POE8#	RXD1/SMISO1/SSCL1		IRQ0-DS	
G4	TCK	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1			
G5		P53*1	BCLK					
G6		P52	RD#		RXD2/SMISO2/SSCL2			
G7		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
G8		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			
G9		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
G10	VCC							
H1	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1			
H2		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/SSIDATA1			ADTRG0#
H3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
H4		P15		MTIOC0B/MTCLKB/ GTETR-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
H6		P54	ALE/ EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#SS2#/ CTX1/ET0_LINKSTA			
H7	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

Table 4.1 List of I/O Registers (Address Order) (4 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK $\geq$ PCLK	ICLK < PCLK	
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 20DFh	DMAC3	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2100h	DMAC4	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2104h	DMAC4	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2108h	DMAC4	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 210Ch	DMAC4	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2110h	DMAC4	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2113h	DMAC4	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2114h	DMAC4	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 211Ch	DMAC4	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 211Dh	DMAC4	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 211Eh	DMAC4	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 211Fh	DMAC4	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2140h	DMAC5	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2144h	DMAC5	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2148h	DMAC5	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 214Ch	DMAC5	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2150h	DMAC5	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2153h	DMAC5	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2154h	DMAC5	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 215Ch	DMAC5	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 215Dh	DMAC5	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 215Eh	DMAC5	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 215Fh	DMAC5	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 2180h	DMAC6	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 2184h	DMAC6	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 2188h	DMAC6	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 218Ch	DMAC6	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 2190h	DMAC6	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 2193h	DMAC6	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 2194h	DMAC6	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA
0008 219Ch	DMAC6	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACaA
0008 219Dh	DMAC6	DMA Software Start Register	DMREQ	8	8	2 ICLK		DMACaA
0008 219Eh	DMAC6	DMA Status Register	DMSTS	8	8	2 ICLK		DMACaA
0008 219Fh	DMAC6	DMA Request Source Flag Control Register	DMCSL	8	8	2 ICLK		DMACaA
0008 21C0h	DMAC7	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACaA
0008 21C4h	DMAC7	DMA Destination Address Register	DMDAR	32	32	2 ICLK		DMACaA
0008 21C8h	DMAC7	DMA Transfer Count Register	DMCRA	32	32	2 ICLK		DMACaA
0008 21CCh	DMAC7	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK		DMACaA
0008 21D0h	DMAC7	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK		DMACaA
0008 21D3h	DMAC7	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK		DMACaA
0008 21D4h	DMAC7	DMA Address Mode Register	DMAMD	16	16	2 ICLK		DMACaA

Table 4.1 List of I/O Registers (Address Order) (20 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9134h	S12AD1	A/D Data Register 10	ADDR10	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9136h	S12AD1	A/D Data Register 11	ADDR11	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9138h	S12AD1	A/D Data Register 12	ADDR12	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ah	S12AD1	A/D Data Register 13	ADDR13	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Ch	S12AD1	A/D Data Register 14	ADDR14	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 913Eh	S12AD1	A/D Data Register 15	ADDR15	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9140h	S12AD1	A/D Data Register 16	ADDR16	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9142h	S12AD1	A/D Data Register 17	ADDR17	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9144h	S12AD1	A/D Data Register 18	ADDR18	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9146h	S12AD1	A/D Data Register 19	ADDR19	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9148h	S12AD1	A/D Data Register 20	ADDR20	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9160h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9161h	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9170h	S12AD1	A/D Sampling State Register T	ADSSTRT	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9171h	S12AD1	A/D Sampling State Register O	ADSSTRO	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9173h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9174h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9175h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9176h	S12AD1	A/D Sampling State Register 4	ADSSTR4	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9177h	S12AD1	A/D Sampling State Register 5	ADSSTR5	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9178h	S12AD1	A/D Sampling State Register 6	ADSSTR6	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9179h	S12AD1	A/D Sampling State Register 7	ADSSTR7	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 917Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9180h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9184h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9186h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9190h	S12AD1	A/D Compare Control Register	ADCMPCR	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9192h	S12AD1	A/D Compare Channel Select Extended Register	ADCMPANSE R	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9193h	S12AD1	A/D Compare Level Extended Register	ADCMPLER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9194h	S12AD1	A/D Compare Channel Select Register 0	ADCMPANSR 0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 9196h	S12AD1	A/D Compare Channel Select Register 1	ADCMPANSR 1	16	16	2, 3 PCLKB	2 ICLK	S12ADC

Table 4.1 List of I/O Registers (Address Order) (48 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 0440h	PTPED MAC	Missed-Frame Counter Register	RMFCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0448h	PTPED MAC	Transmit FIFO Threshold Register	TFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0450h	PTPED MAC	FIFO Depth Register	FDR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0458h	PTPED MAC	Receive Method Control Register	RMCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0464h	PTPED MAC	Transmit FIFO Underflow Counter	TFUCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0468h	PTPED MAC	Receive FIFO Overflow Counter	RFOCR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0470h	PTPED MAC	Flow Control Start FIFO Threshold Setting Register	FCFTR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0478h	PTPED MAC	Receive Data Padding Insert Register	RPADIR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 047Ch	PTPED MAC	Transmit Interrupt Setting Register	TRIMD	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04C8h	PTPED MAC	Receive Buffer Write Address Register	RBWAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04CCh	PTPED MAC	Receive Descriptor Fetch Address Register	RDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D4h	PTPED MAC	Transmit Buffer Read Address Register	TBRAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 04D8h	PTPED MAC	Transmit Descriptor Fetch Address Register	TDFAR	32	32	4, 5 PCLKA	2, 3 ICLK	EDMACa
000C 0500h	EPTPC	PTP Reset Register	PTRSTR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 0504h	EPTPC	STCA Clock Select Register	STCSELR	32	32	3, 4 PCLKA	2, 3 ICLK	EPTPC
000C 1200h	MTU3	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1201h	MTU4	Timer Control Register	TCR	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1202h	MTU3	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1203h	MTU4	Timer Mode Register 1	TMDR1	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1204h	MTU3	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1205h	MTU3	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1206h	MTU4	Timer I/O Control Register H	TIORH	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1207h	MTU4	Timer I/O Control Register L	TIORL	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1208h	MTU3	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1209h	MTU4	Timer Interrupt Enable Register	TIER	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Ah	MTU	Timer Output Master Enable Register A	TOERA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Dh	MTU	Timer Gate Control Register A	TGCRA	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Eh	MTU	Timer Output Control Register 1A	TOCR1A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 120Fh	MTU	Timer Output Control Register 2A	TOCR2A	8	8	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1210h	MTU3	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1212h	MTU4	Timer Counter	TCNT	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1214h	MTU	Timer Cycle Data Register A	TCDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1216h	MTU	Timer Dead Time Data Register A	TDDRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1218h	MTU3	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ah	MTU3	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Ch	MTU4	Timer General Register A	TGRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 121Eh	MTU4	Timer General Register B	TGRB	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1220h	MTU	Timer Subcounter A	TCNTSA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1222h	MTU	Timer Cycle Buffer Register A	TCBRA	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1224h	MTU3	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1226h	MTU3	Timer General Register D	TGRD	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a
000C 1228h	MTU4	Timer General Register C	TGRC	16	16	5, 6 PCLKA	2, 3 ICLK	MTU3a

Table 4.1 List of I/O Registers (Address Order) (55 / 67)

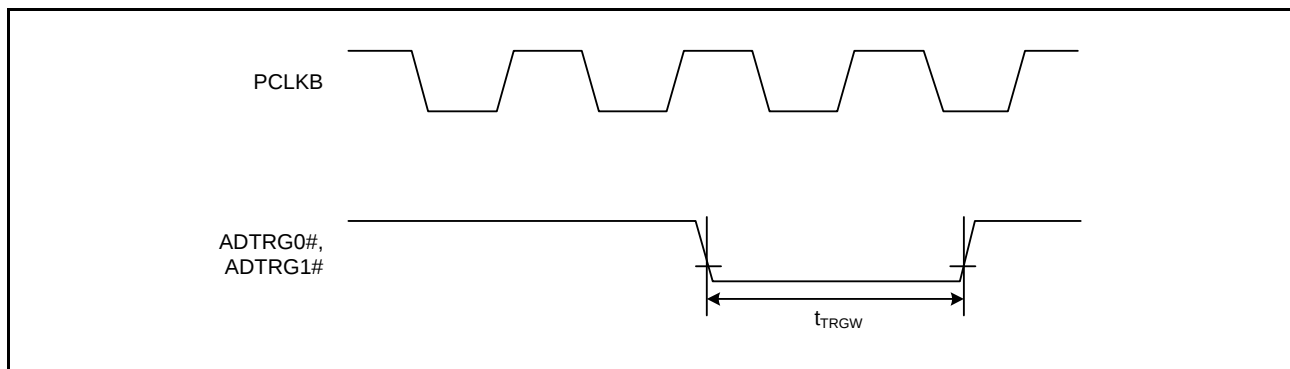
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F	GTCCRF	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 229Ch	GPT3	General PWM Timer Cycle Setting Register	GTPR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 229Eh	GPT3	General PWM Timer Cycle Setting Buffer Register	GTPBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A0h	GPT3	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A	GTADTRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22A8h	GPT3	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B	GTADTRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B0h	GPT3	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register	GTONCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register	GTDTCR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U	GTDVU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D	GTDVD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U	GTDBU	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D	GTDBD	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register	GTSOS	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	16	16	4, 5 PCLKA	2, 3 ICLK	GPTA
000C 4000h	EPTPC	MINT Interrupt Source Status Register	MIESR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4004h	EPTPC	MINT Interrupt Request Permission Register	MIEIPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4010h	EPTPC	ELC Output/IPLS Interrupt Request Permission Register	ELIPPR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4014h	EPTPC	ELC Output/IPLS Interrupt Permission Automatic Clearing Register	ELIPACR	32	32	5, 6 PCLKA	2, 3 ICLK	EPTPC
000C 4040h	EPTPC	STCA Status Register	STSR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4044h	EPTPC	STCA Status Notification Permission Register	STIPR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4050h	EPTPC	STCA Clock Frequency Setting Register	STCFR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4054h	EPTPC	STCA Operating Mode Register	STMR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4058h	EPTPC	Sync Message Reception Timeout Register	SYNTOR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4060h	EPTPC	IPLS Interrupt Request Timer Select Register	IPTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4064h	EPTPC	MINT Interrupt Request Timer Select Register	MITSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4068h	EPTPC	ELC Output Timer Select Register	ELTSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 406Ch	EPTPC	Time Synchronization Channel Select Register	STCHSELR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4080h	EPTPC	Slave Time Synchronization Start Register	SYNSTARTR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4084h	EPTPC	Local Time Counter Initial Value Load Directive Register	LCIVLDR	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4090h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4094h	EPTPC	Synchronization Loss Detection Threshold Register	SYNTDARL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4098h	EPTPC	Synchronization Detection Threshold Register	SYNTDBRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 409Ch	EPTPC	Synchronization Detection Threshold Register	SYNTDBRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B0h	EPTPC	Local Time Counter Initial Value Register	LCIVRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B4h	EPTPC	Local Time Counter Initial Value Register	LCIVRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 40B8h	EPTPC	Local Time Counter Initial Value Register	LCIVRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4124h	EPTPC	Worst 10 Acquisition Directive Register	GETW10R	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4128h	EPTPC	Positive Gradient Limit Register	PLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 412Ch	EPTPC	Positive Gradient Limit Register	PLIMITRM	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4130h	EPTPC	Positive Gradient Limit Register	PLIMITRL	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC
000C 4134h	EPTPC	Negative Gradient Limit Register	MLIMITRU	32	32	8 to 43 PCLKA	2 to 22 ICLK	EPTPC

Table 5.30 A/D Converter Trigger Timing

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 5.43

Note 1. t_{PBcyc} : PCLKB cycle

**Figure 5.43 A/D Converter Trigger Input Timing****Table 5.31 CAC Timing**

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item*1, *2			Symbol	Min.*1	Max.	Unit*1	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$	t_{CACREF}	$4.5 t_{cac} + 3 t_{PBcyc}$	—	ns	
		$t_{PBcyc} > t_{cac}$		$5 t_{cac} + 6.5 t_{PBcyc}$	—		

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. t_{CAC} : CAC count clock source cycle

Table 5.37 RIIC Timing (2)

Conditions: $VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq VREFH0 \leq AVCC0$,
 $VCC_USBA = AVCC_USBA = 3.0$ to 3.6 V,
 $VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min. *1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 20$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle, t_{PBcyc} : PCLKB cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

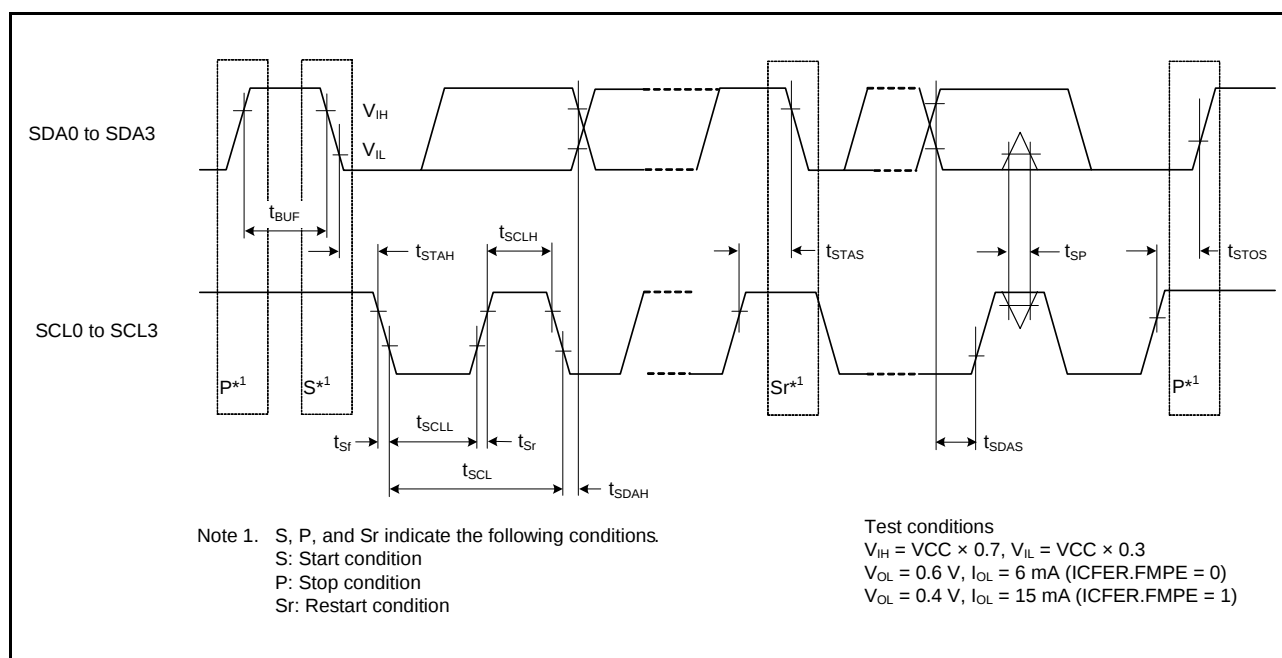


Figure 5.56 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

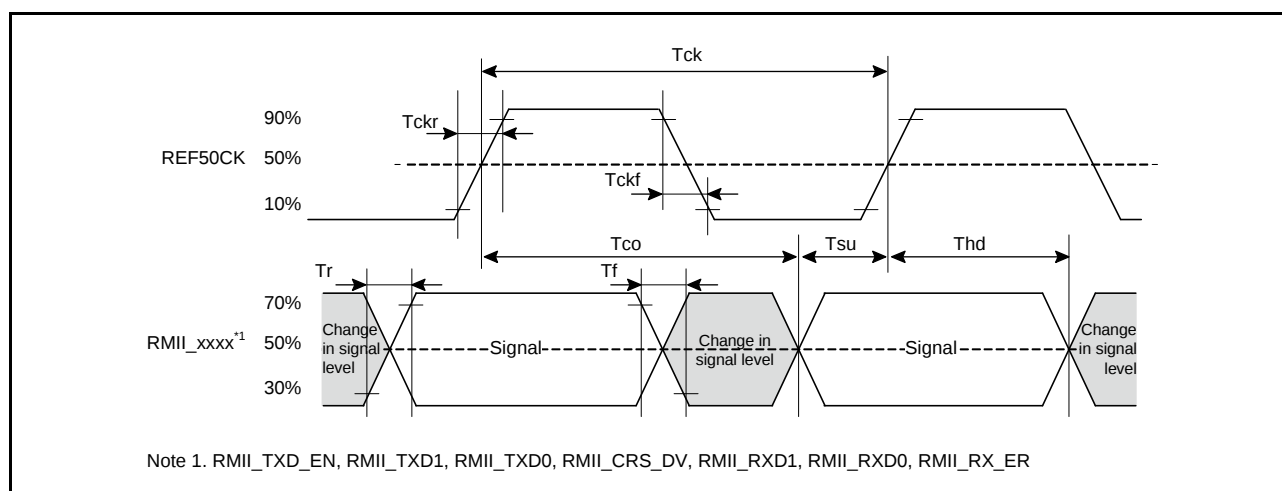


Figure 5.62 Timing with the REF50CK and RMII Signals

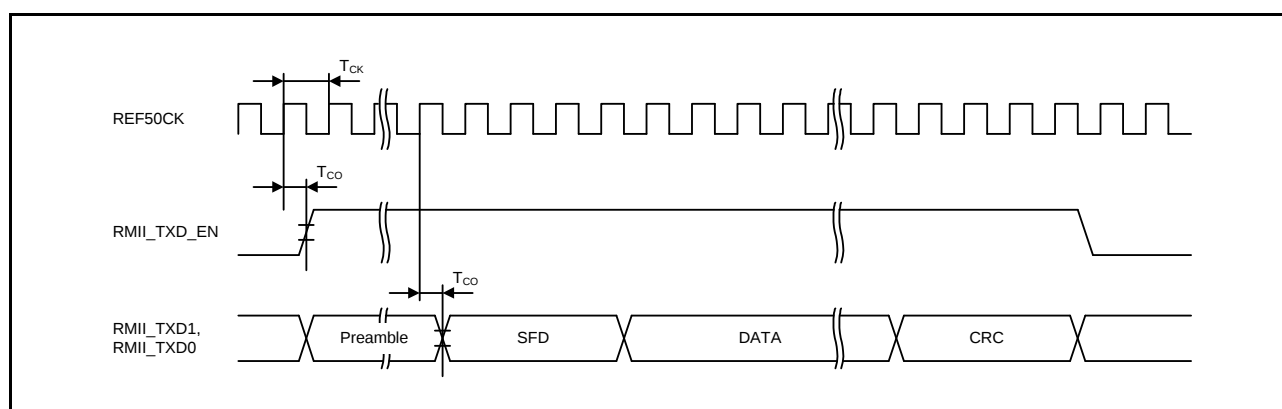


Figure 5.63 RMII Transmission Timing

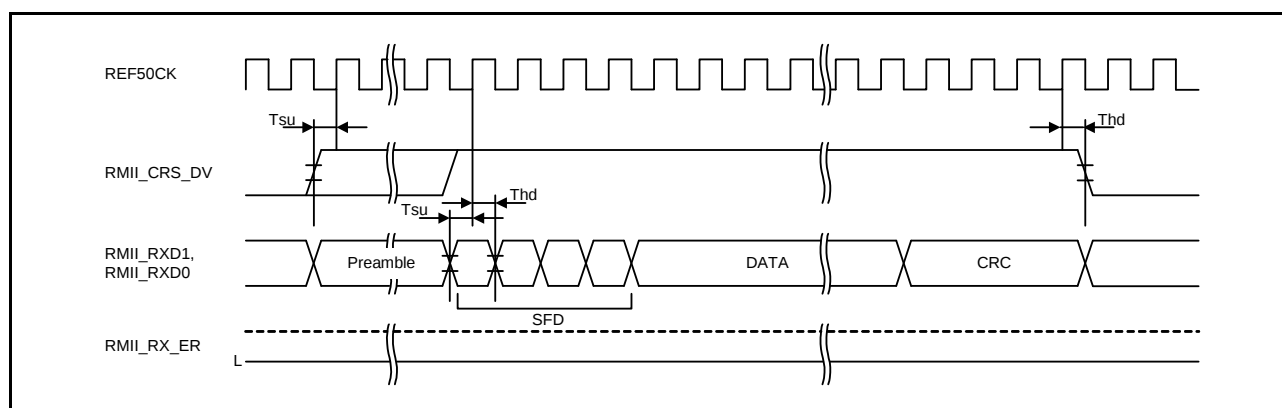


Figure 5.64 RMII Reception Timing (Normal Operation)

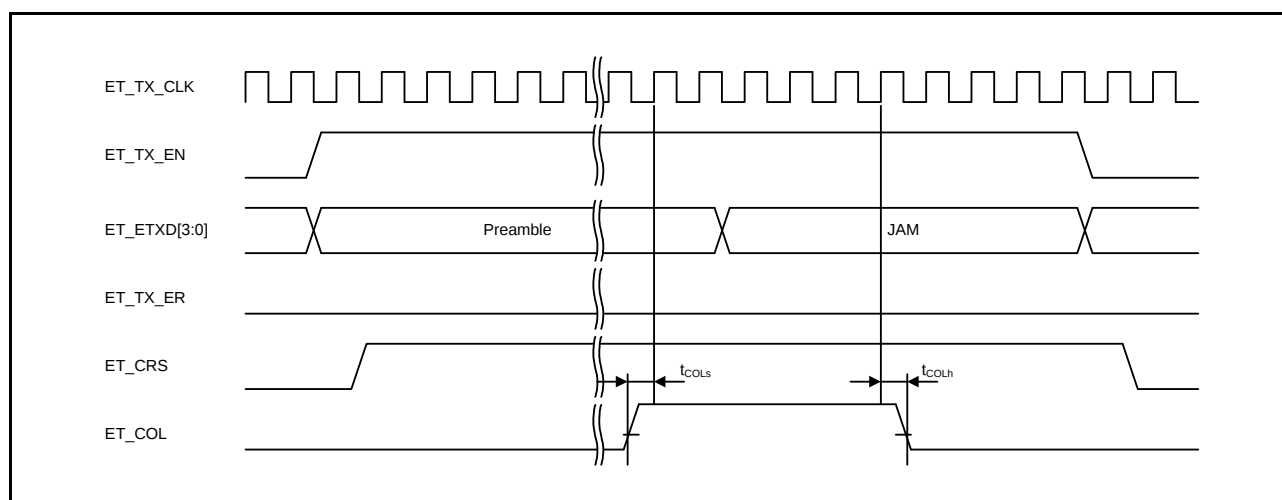


Figure 5.68 MII Transmission Timing (Conflict Occurrence)

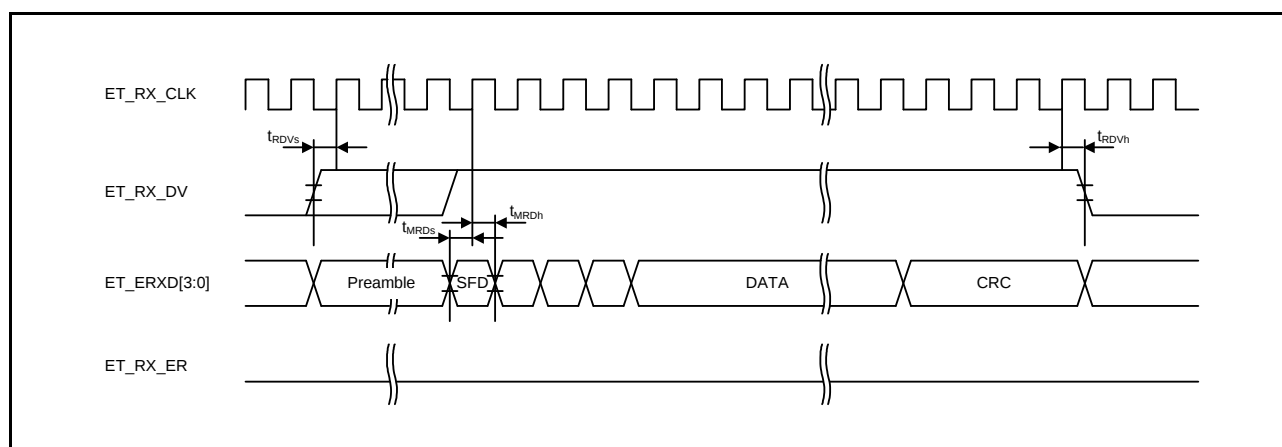


Figure 5.69 MII Reception Timing (Normal Operation)

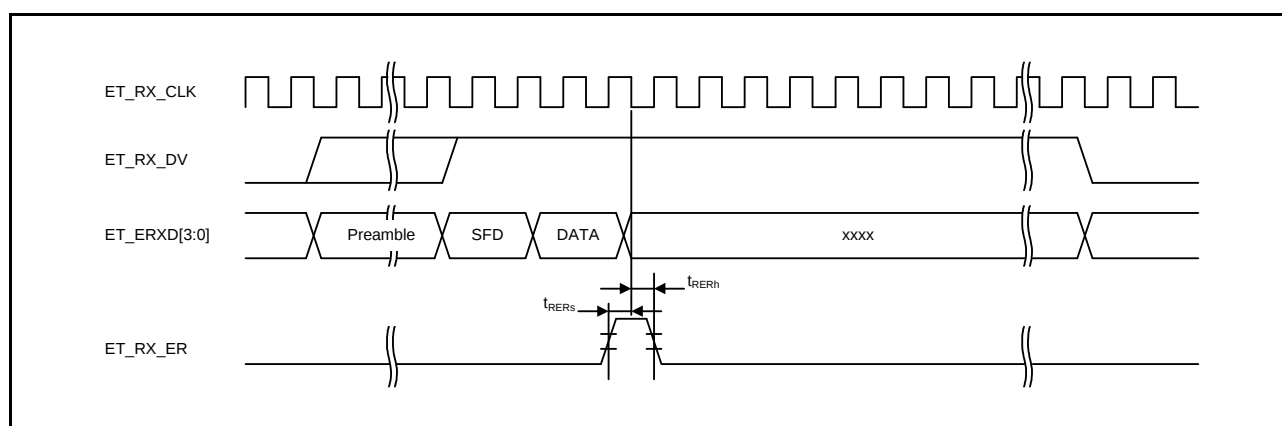


Figure 5.70 MII Reception Timing (Error Occurrence)

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.50 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AVSS_USBA = 0$ V,
 $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V _{POR}	2.5	2.6	2.7	V	Figure 5.79
		Low power consumption function enabled*2		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V _{det0_1}	2.84	2.94	3.04		Figure 5.80
			V _{det0_2}	2.77	2.87	2.97		
			V _{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V _{det1_1}	2.89	2.99	3.09		Figure 5.81
			V _{det1_2}	2.82	2.92	3.02		
			V _{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V _{det2_1}	2.89	2.99	3.09		Figure 5.82
			V _{det2_2}	2.82	2.92	3.02		
			V _{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.79
	LVD0 reset time		t _{LVD0}	—	0.70	—		Figure 5.80
	LVD1 reset time		t _{LVD1}	—	0.57	—		Figure 5.81
	LVD2 reset time		t _{LVD2}	—	0.57	—		Figure 5.82
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.79, Figure 5.80
Response delay time			t _{det}	—	—	200	μs	Figure 5.79 to Figure 5.82
LVD operation stabilization time (after LVD is enabled)*3			T _{d(E-A)}	—	—	10	μs	Figure 5.81, Figure 5.82
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.

Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

Note 3. The voltage of $V_{CC} = AVCC0 = AVCC1$ when LVD1 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 1 level ($V_{det1_1, 2, 3}$) selected by the LVDLVLR.LVD1LVL[3:0] bits.

Similarly, the voltage of $V_{CC} = AVCC0 = AVCC1$ when LVD2 is enabled must be set to at least 80 mV above the maximum value of the voltage detection 2 level ($V_{det2_1, 2, 3}$) selected by the LVDLVLR.LVD2LVL[3:0] bits.

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

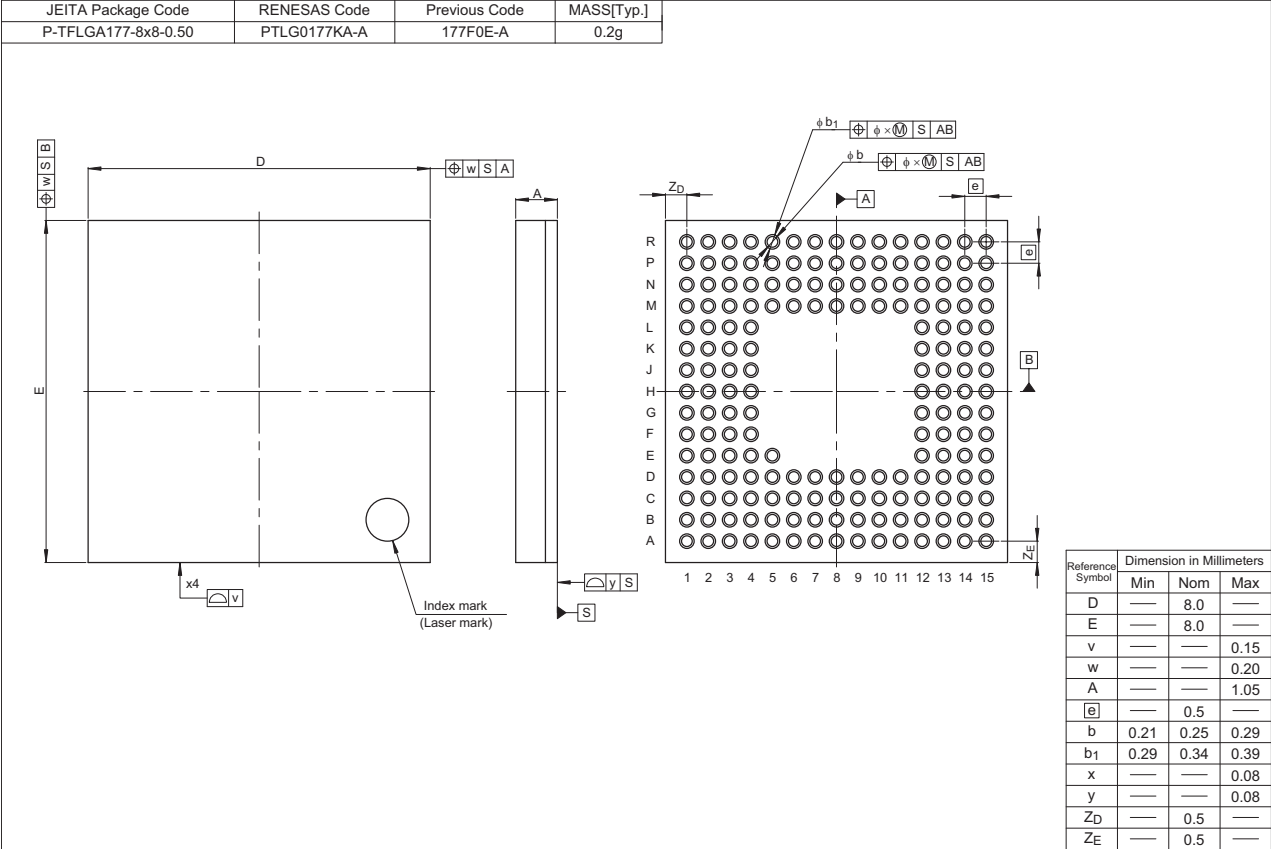


Figure A 177-Pin TFLGA (PTLG0177KA-A)

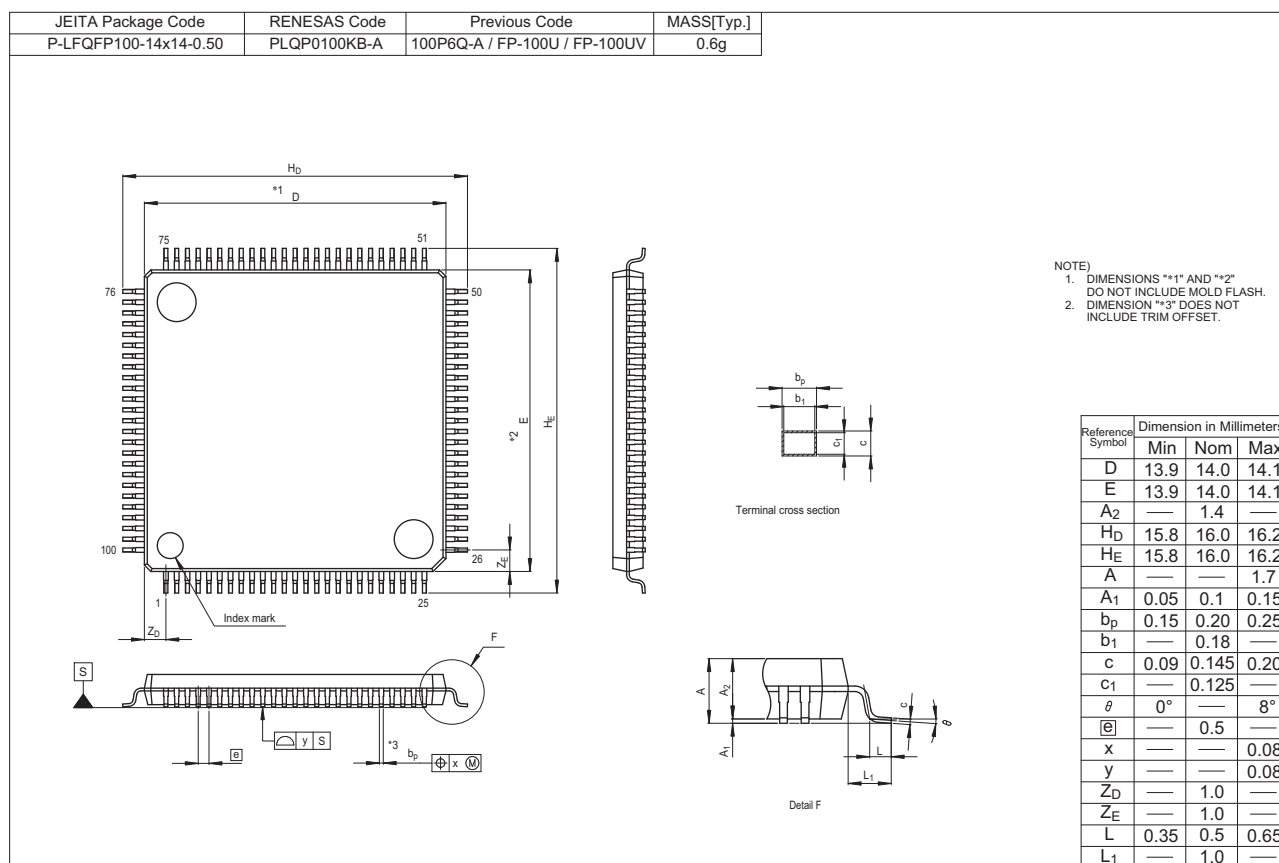


Figure G 100-Pin LFQFP (PLQP0100KB-A)