Renesas Electronics America Inc - R5F564MLHDFC#V1 Datasheet

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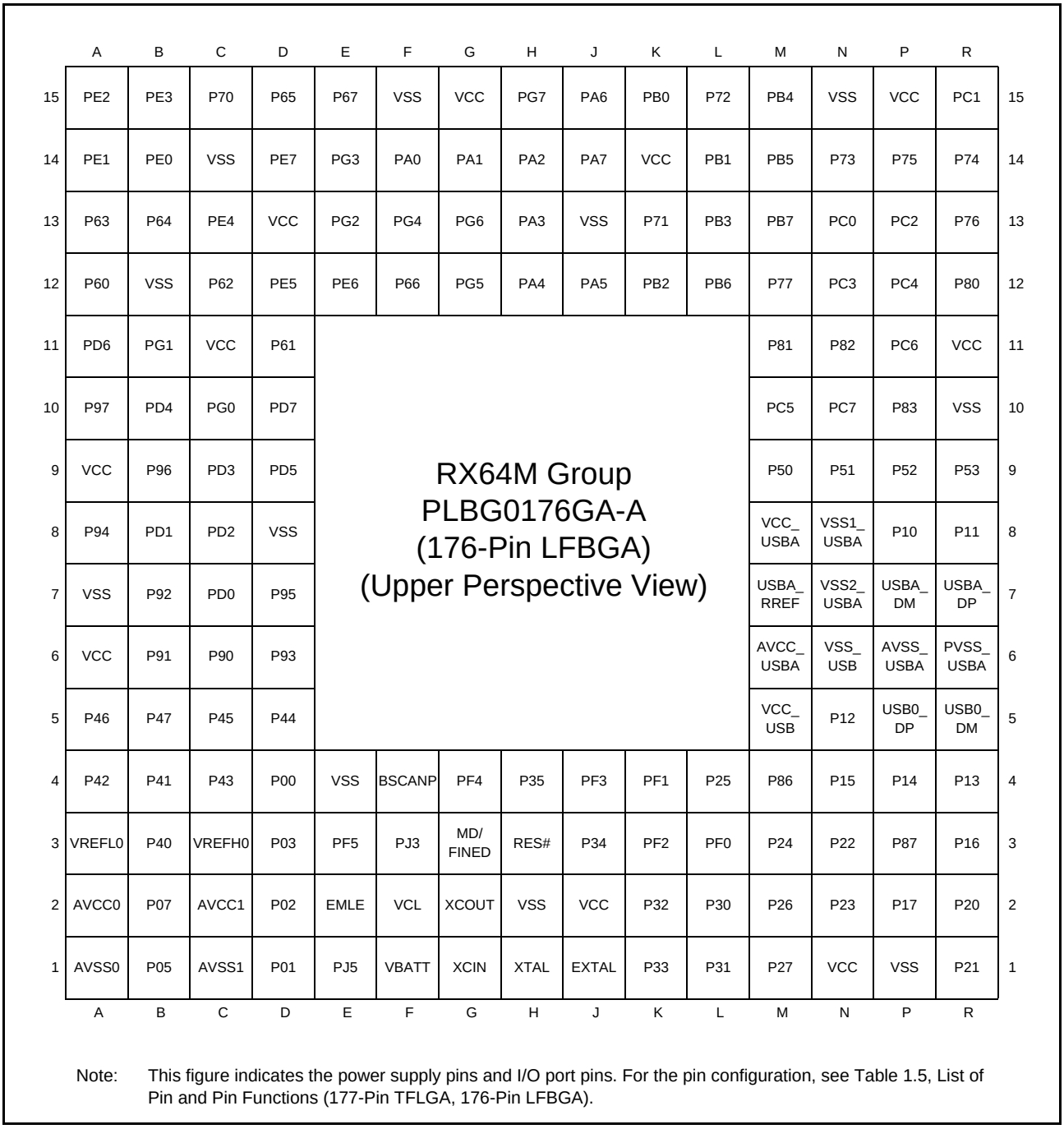
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlhdfc-v1

Table 1.4 Pin Functions (7/8)

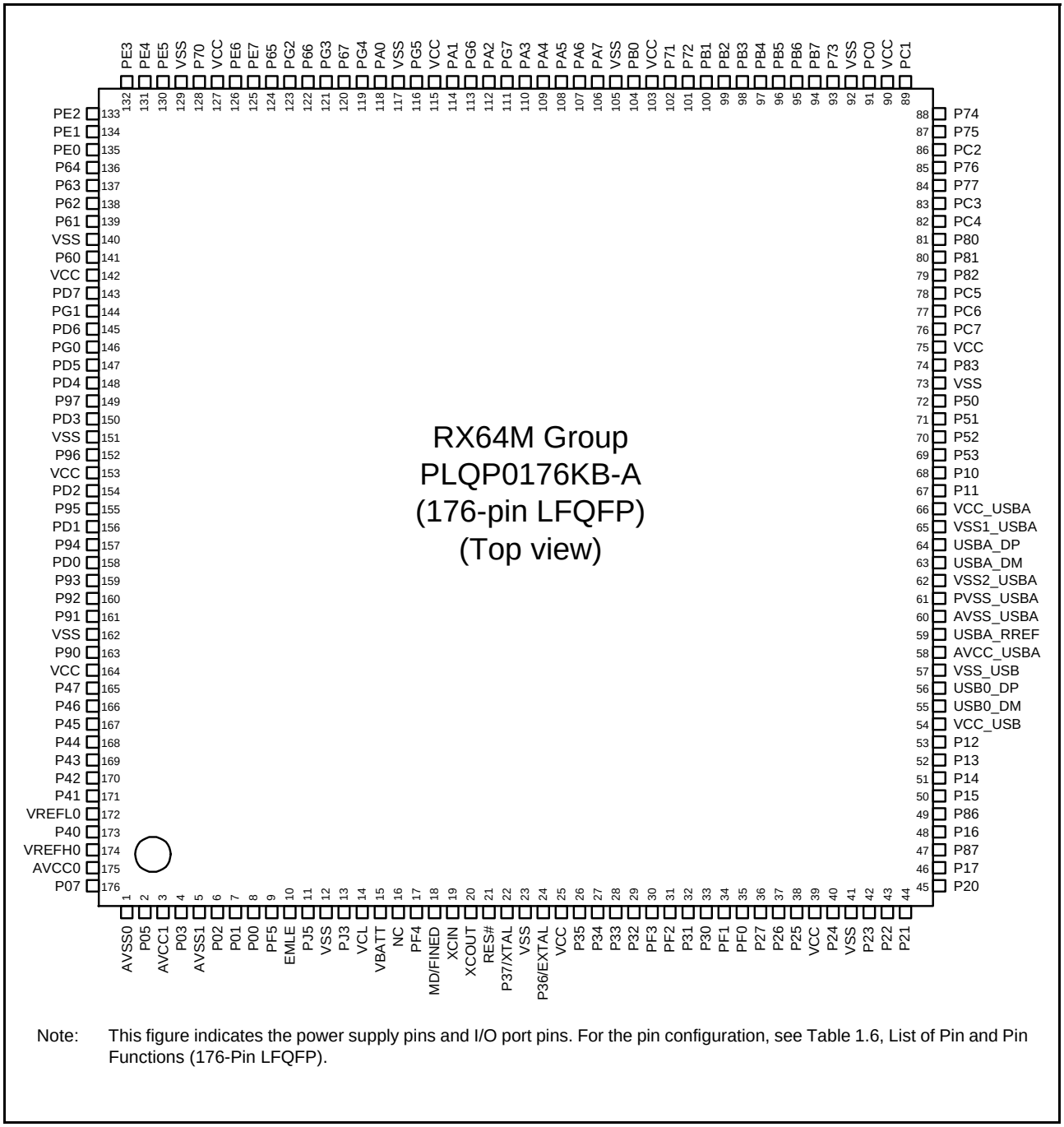
Classifications	Pin Name	I/O	Description
MMC host interface	MMC_CLK-A/ MMC_CLK-B	Output	MMC clock pin
	MMC_CMD-A/ MMC_CMD-B	I/O	Command/response pin
	MMC_D7-A/MMC_D7-B to MMC_D0-A/MMC_D0-B	I/O	Transmit data/receive data
	MMC_CD-A/MMC_CD-B	Input	Card detection pin
	MMC_RES#-A/MMC_RES#-B	Output	MMC reset output pin
SD host interface	SDHI_CLK-A/SDHI_CLK-B	Output	SD clock output pin
	SDHI_CMD-A/SDHI_CMD-B	I/O	SD command output, response input signal pin
	SDHI_D3-A/SDHI_D3-B to SDHI_D0-A/SDHI_D0-B	I/O	SD data bus pins
	SDHI_CD-A/SDHI_CD-B	Input	SD card detection pin
	SDHI_WP-A/SDHI_WP-B	Input	SD write-protect signal
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
12-bit A/D converter	AN000 to AN007, AN100 to AN120	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply.
	AVSS1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1) and D/A converter. This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply.



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61								P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P53	9
8	P94	PD1	PD2	VSS								VCC_ USBA	VSS1_ USBA	P10	P11	8
7	VSS	P92	PD0	P95								USBA_ RREF	VSS2_ USBA	USBA_ DM	USBA_ DP	7
6	VCC	P91	P90	P93								AVCC_ USBA	VSS_ USB	AVSS_ USBA	PVSS_ USBA	6
5	P46	P47	P45	P44								VCC_ USB	P12	USB0_ DP	USB0_ DM	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P13	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/ FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	AVCC1	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	AVSS1	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

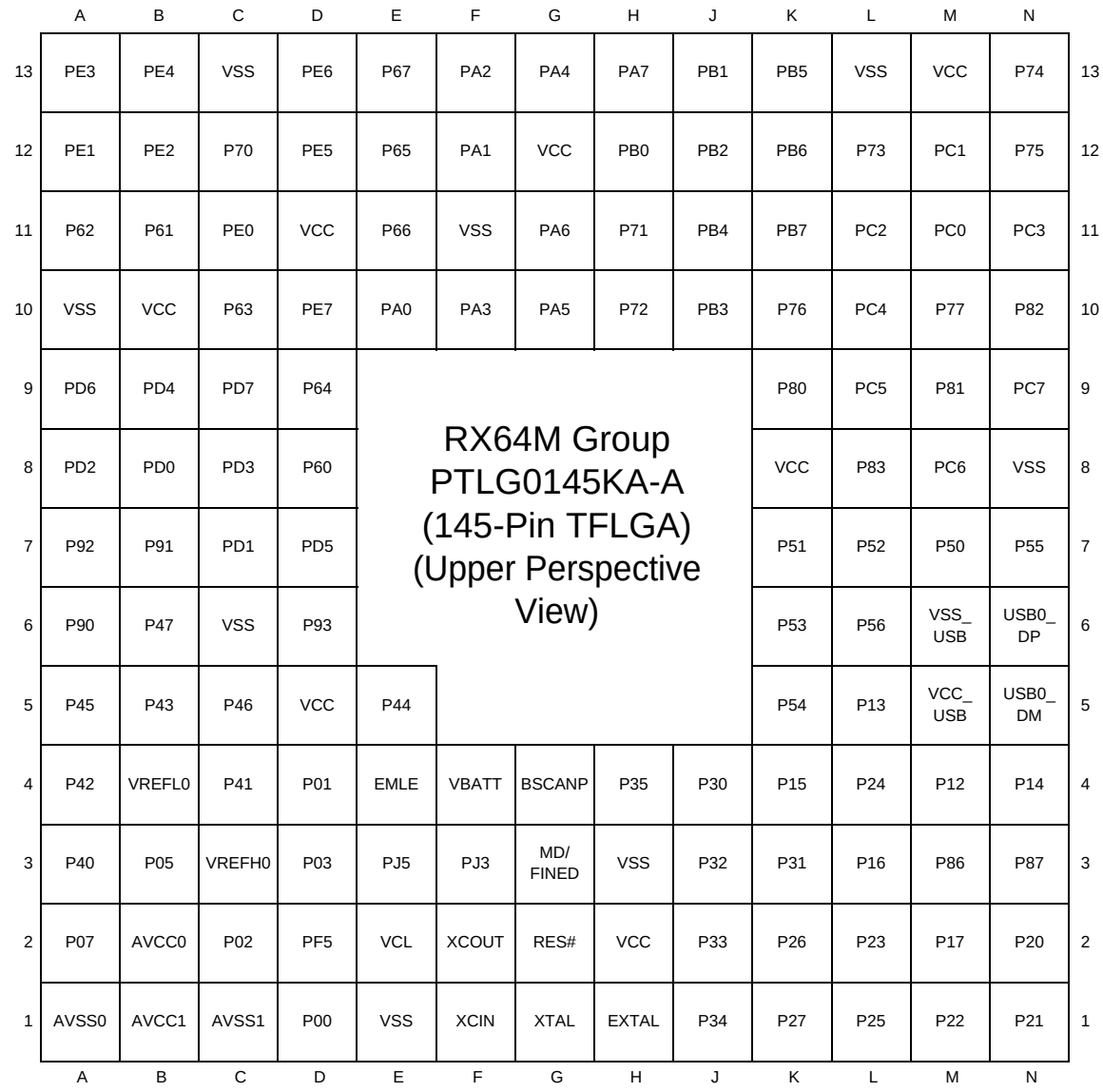
Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LFQFP).

Figure 1.5 Pin Assignment (176-Pin LFQFP)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/7)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
J15		PA6	A6	MTIC5V/MTCLKB/ GTETRG-C/TIOCA2/ TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/ MOSIA-B/ ET0_EXOUT			
K1		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/ SSCL1			
K4	TCK	PF1			SCK1			
K12		PB2	A10	TIOCC3/TCLKC/ PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET0_RX_CLK/ REF50CK0			
K13		P71	A18/CS1#		ET0_MDIO			
K14	VCC							
K15		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/ET0_ERXD1/ RMII0_RXD1		IRQ12	
L1		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC		IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ ET1_MDIO		IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/ SSDA1			
L4		P25	CS5#/ EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ SSIDATA1	HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/ TMO0/PO27/POE11#	SCK4/SCK6/ ET0_RX_ER/ RMII0_RX_ER			
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET0_ERXD0/ RMII0_RXD0		IRQ4-DS	
L15		P72	A19/CS2#		ET0_MDC			
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/ET1_WOL			
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ ET1_EXOUT			
M3		P24	CS4#/ EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/ USB0_VBUSEN/ SSISCK1	PIXCLK		
M4		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
M5	VCC_USB	P12	WR3#/BC3#	MTIC5U/TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]		IRQ2	
M6	AVCC_ USBA							

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (1/7)

Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	NC							
17	TRST#	PF4						
18	MD/FINED							
19	XCIN							
20	XCOUT							
21	RES#							
22	XTAL	P37						
23	VSS							
24	EXTAL	P36						
25	VCC							
26	UPSEL	P35					NMI	
27		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOCD0/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN	VSYNC	IRQ2-DS	
30	TMS	PF3						
31	TDI	PF2			RXD1/SMISO1/ SSCL1			
32		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC		IRQ1-DS	
33		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ ET1_MDIO		IRQ0-DS	
34	TCK	PF1			SCK1			
35	TDO	PF0			TXD1/SMOSI1/ SSDA1			

Table 1.6 List of Pin and Pin Functions (176-Pin LFQFP) (3/7)

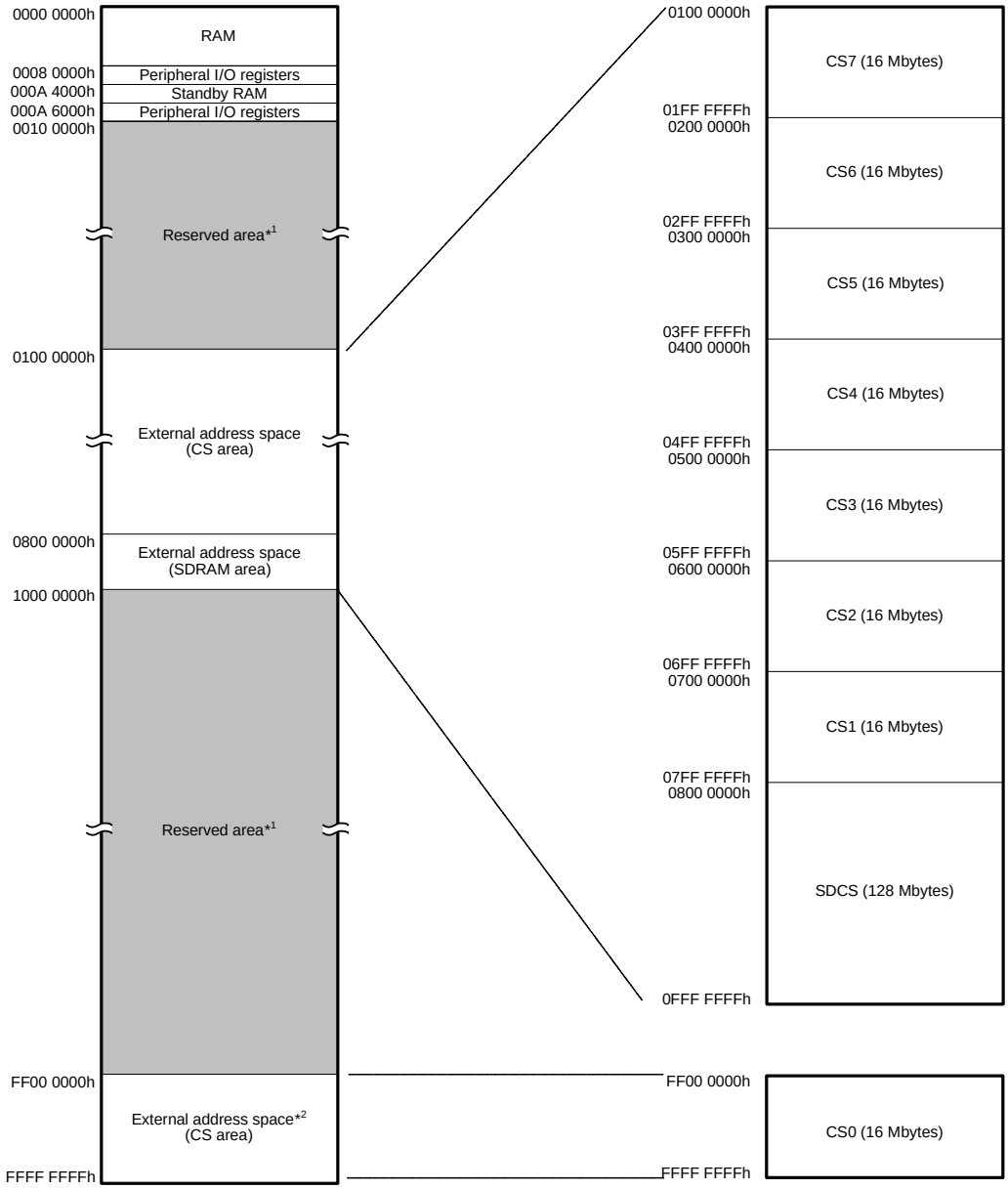
Pin Number 176-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
57	VSS_USB							
58	AVCC_ USBA							
59	USBA_ RREF							
60	AVSS_ USBA							
61	PVSS_ USBA							
62	VSS2_ USBA							
63					USBA_DM			
64					USBA_DP			
65	VSS1_ USBA							
66	VCC_ USBA							
67		P11		MTIC5V/TMCI3	SCK2/USBA_VBUS/ USBA_VBUSEN		IRQ1	
68		P10	ALE	MTIC5W/TMRI3	USBA_OVRCURA		IRQ0	
69		P53*1	BCLK					
70		P52	RD#		RXD2/SMISO2/SSCL2			
71		P51	WR1#/BC1#/ WAIT#		SCK2			
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
73	VSS							
74		P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
75	VCC							
76	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		
79		P82	EDREQ1	MTIOC4A/ GTIOC2A-D/PO28	TXD10/ET0_ETXD1/ RMII0_TXD1	MMC_D4-A		
80		P81	EDACK0	MTIOC3D/ GTIOC0B-D/PO27	RXD10/ET0_ETXD0/ RMII0_TXD0	MMC_D3-A/ SDHI_CD-A/ QIO3-A		
81		P80	EDREQ0	MTIOC3B/PO26	SCK10/RTS10#/ ET0_TX_EN/ RMII0_TXD_EN	MMC_D2-A/ SDHI_WP-A/ QIO2-A		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETRG-D/TMCI1/ PO25/POE0#	SCK5/CTS8#/SSLA0-A/ET0_TX_CLK	MMC_D1-A/ SDHI_D1-A/ QIO1-A/QMI-A		
83		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ ET0_TX_ER	MMC_D0-A/ SDHI_D0-A/ QIO0-A/ QMO-A		
84		P77	CS7#	PO23	TXD11/ET0_RX_ER/ RMII0_RX_ER	MMC_CLK-A/ SDHI_CLK-A/ QSPCLK-A		

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (2/5)

Pin Number 144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIg, SCIh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
36		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
39		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
41		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
42		P15		MTIOC0B/MTCLKB/ GTETRG-B/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
45		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
46	VCC_USB							
47					USB0_DM			
48					USB0_DP			
49	VSS_USB							
50		P56	EDACK1	MTIOC3C/TIOCA1				
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
53		P53*1	BCLK					
54		P52	RD#		RXD2/SMISO2/SSCL2			
55		P51	WR1#/BC1#/ WAIT#		SCK2			
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
57	VSS							
58	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
59	VCC							
60	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		

3.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7) and SDRAM area (SDCS). The CS areas are divided into up to eight areas (CS0 to CS7), each corresponding to the CSn# signal output from a CSn# (n = 0 to 7) pin.
Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM areas (SDCS) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure on this section, Memory Map in Each Operating Mode.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (30 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C00Fh	PORTF	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C010h	PORTG	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C025h	PORT5	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C026h	PORT6	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C027h	PORT7	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C028h	PORT8	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C029h	PORT9	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ah	PORTA	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports

Table 4.1 List of I/O Registers (Address Order) (36 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1BDh	MPC	PF5 Pin Function Control Register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1C7h	MPC	PG7 Pin Function Control Register	PG7PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1D5h	MPC	PJ5 Pin Function Control Register	PJ5PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C280h	SYSTEM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption

Table 4.1 List of I/O Registers (Address Order) (64 / 67)

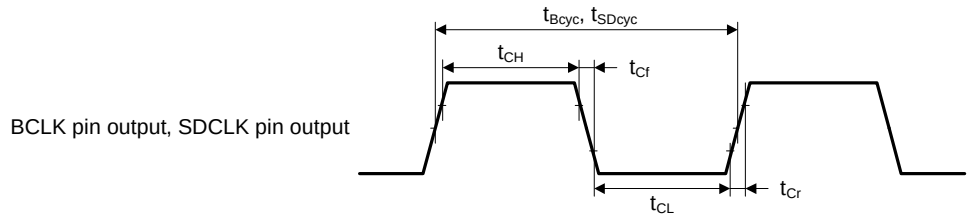
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000D 044Ch	USBA	Frame Number Register	FRMNUM	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 044Eh	USBA	µFrame Number Register	UFRMNUM	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0450h	USBA	USB Address Register	USBADDR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0454h	USBA	USB Request Type Register	USBREQ	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0456h	USBA	USB Request Value Register	USBVAL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0458h	USBA	USB Request Index Register	USBINDX	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 045Ah	USBA	USB Request Length Register	USBLENG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 045Ch	USBA	DCP Configuration Register	DCPCFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 045Eh	USBA	DCP Maximum Packet Size Register	DCPMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0460h	USBA	DCP Control Register	DCPCTR	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0464h	USBA	Pipe Window Select Register	PIPESEL	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 0468h	USBA	Pipe Configuration Register	PIPECFG	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 046Ah	USBA	Pipe Buffer Register	PIPEBUF	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 046Ch	USBA	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA
000D 046Eh	USBA	Pipe Cycle Control Register	PIPEPERI	16	16	(3 + BUSWAIT) PCLKA or more	Rounded up to the nearest integer greater than 1 + (3 + BUSWAIT) × (frequency ratio of ICLK/PCLKB)*5	USBA

5.3.2 Clock Timing

Table 5.11 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Packages with 177 to 144 pins	t_{Bcyc}	16.6	—	—	ns	Figure 5.3
	Packages with 100 pins or less		33.2	—	—	ns	
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Packages with 177 to 144 pins	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, C = 30 pF

Figure 5.3 BCLK Pin and SDCLK Pin Output Timing

Table 5.12 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	ns	

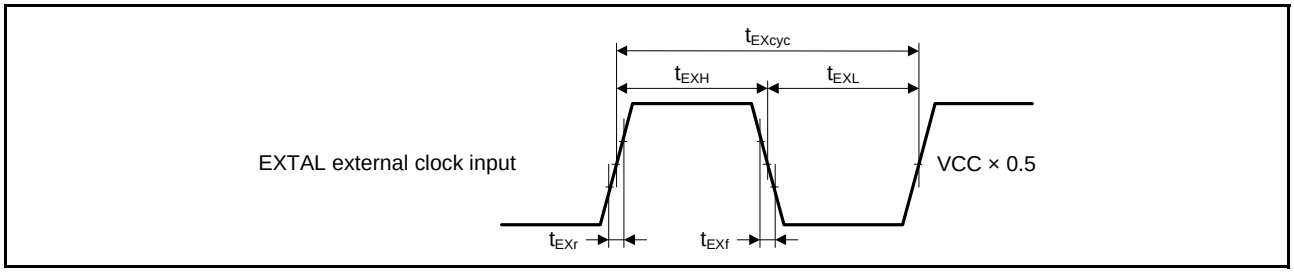


Figure 5.4 EXTAL External Clock Input Timing

Table 5.13 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 5.5
Main clock oscillation stabilization wait time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

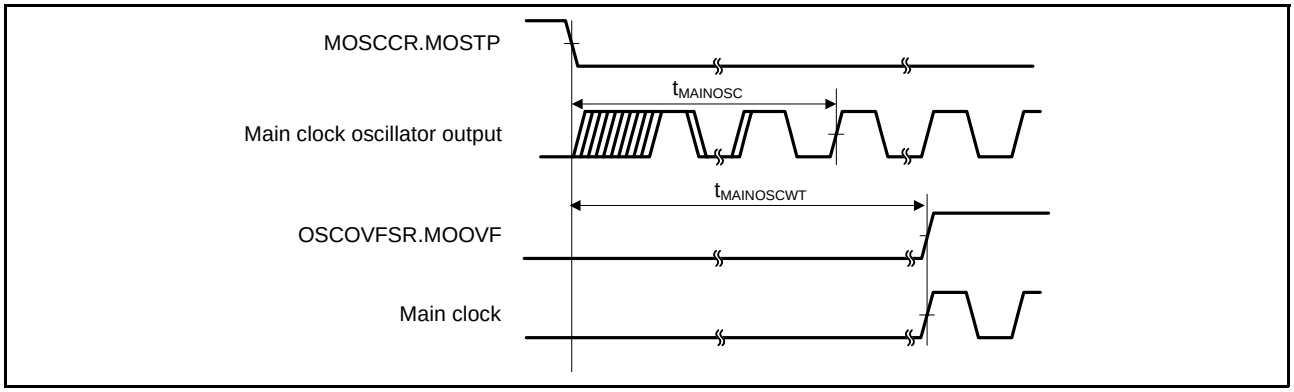


Figure 5.5 Main Clock Oscillation Start Timing

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
$T_a = T_{opr}$

Item	Symbol	min	typ	max	Unit	Test Conditions
Recovery time after cancellation of deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 5.13
Wait time after cancellation of deep software standby mode	t_{DSBYWT}	31	—	32	t_{Lcyc}	

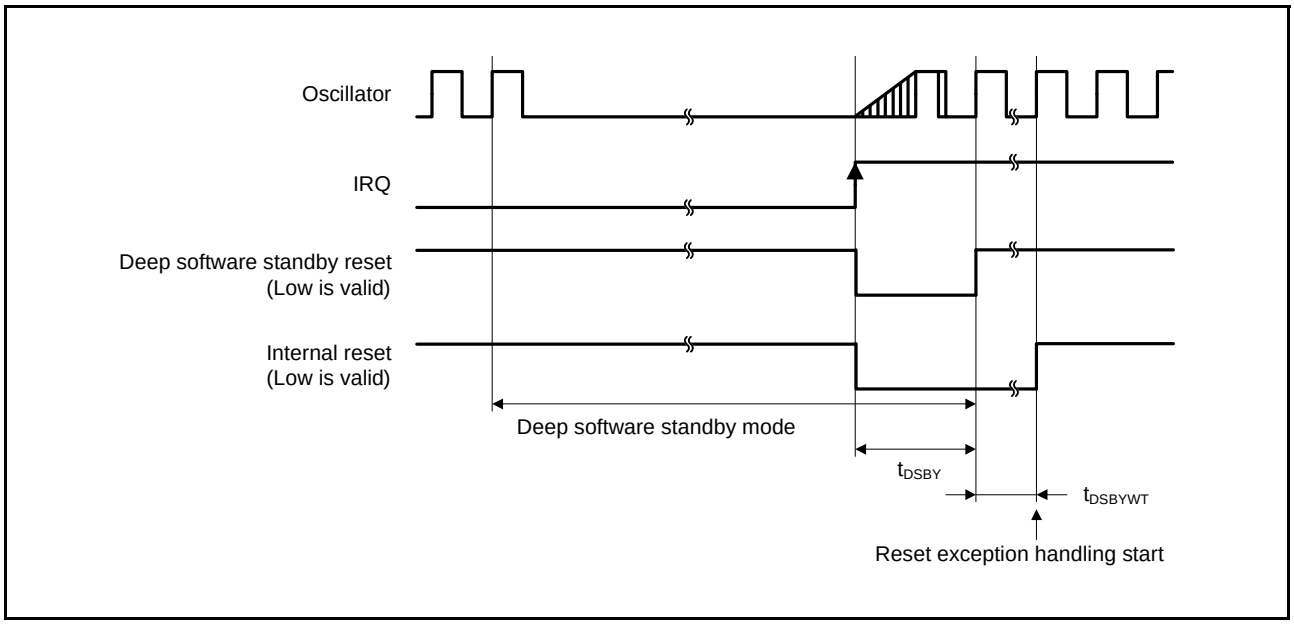
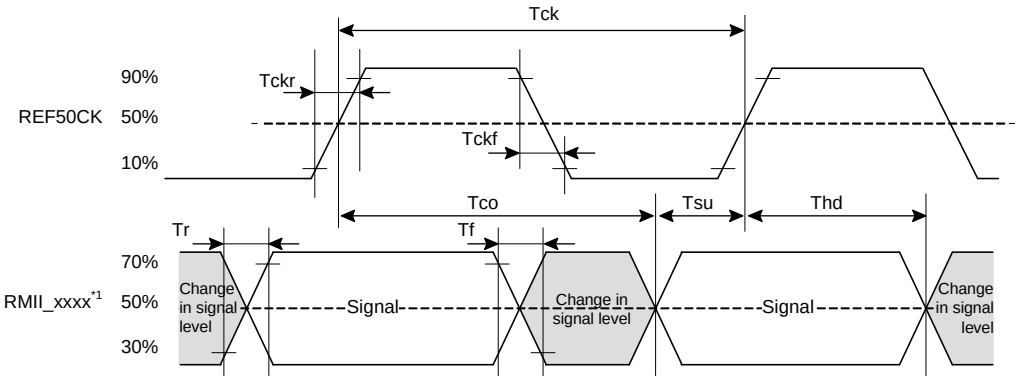


Figure 5.13 Deep Software Standby Mode Cancellation Timing



Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0, RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

Figure 5.62 Timing with the REF50CK and RMII Signals

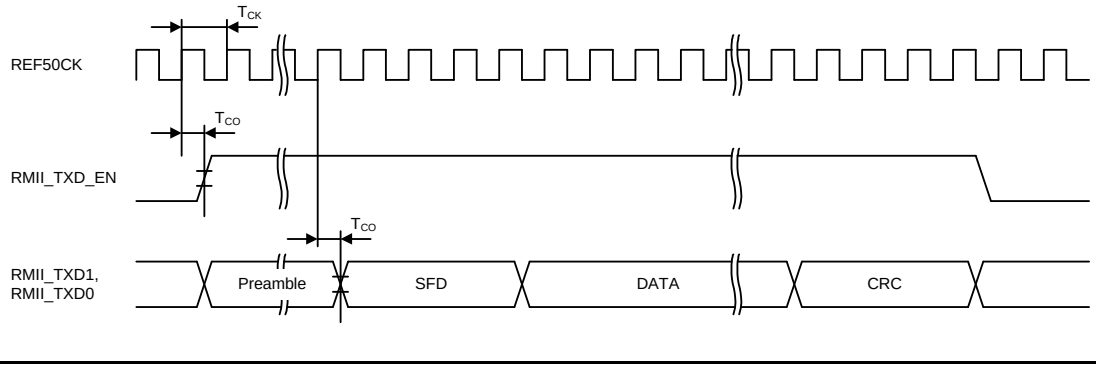


Figure 5.63 RMII Transmission Timing

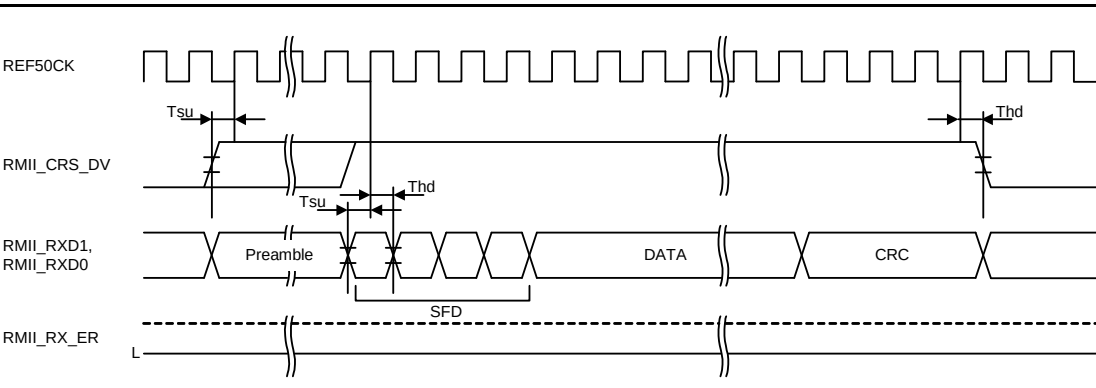


Figure 5.64 RMII Reception Timing (Normal Operation)

Table 5.44 Battery Charge Characteristics (USBA only)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V, USBA_RREF = 2.2 kΩ ±1%, USBMCLK = 20/24 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.	Max.	Unit	Test Conditions
D+ sink current	I_{DP_SINK}	25	175	μA	
D- sink current	I_{DM_SINK}	25	175	μA	
DCD source current	I_{DP_SRC}	7	13	μA	
Data detection voltage	V_{DAT_REF}	0.25	0.4	V	
D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

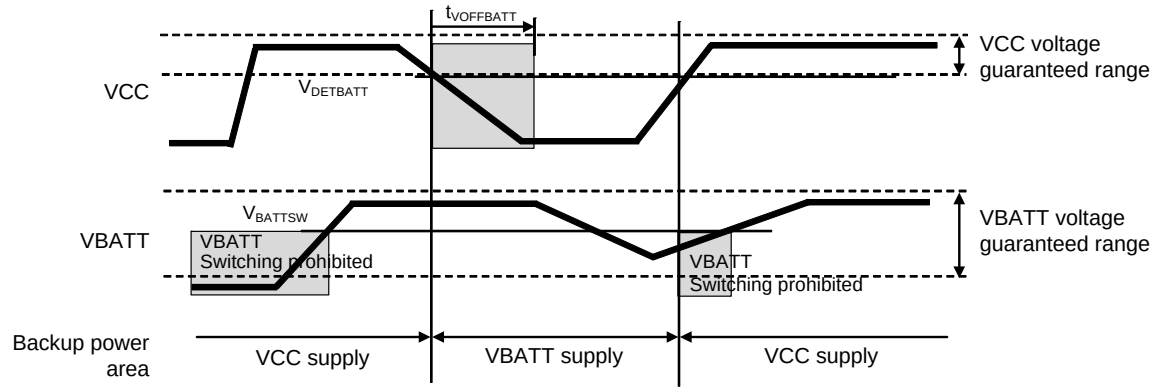
5.10 Battery Backup Function Characteristics

Table 5.52 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V,
V_{BATT} = 2.0 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 5.84
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.70	—	—		
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	—	—	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).



Note. The VBATT voltage when the supplied power source switches from Vcc to V_{BATT} should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 5.84 Battery Backup Function Characteristics

5.11 Flash Memory Characteristics

Table 5.53 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0,
VCC_USBA = AVCC_USBA = 3.0 to 3.6 V,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = VSS1_USBA = VSS2_USBA = PVSS_USBA = AVSS_USBA = 0 V
Temperature range for programming/erasure: $T_a = T_{opr}$

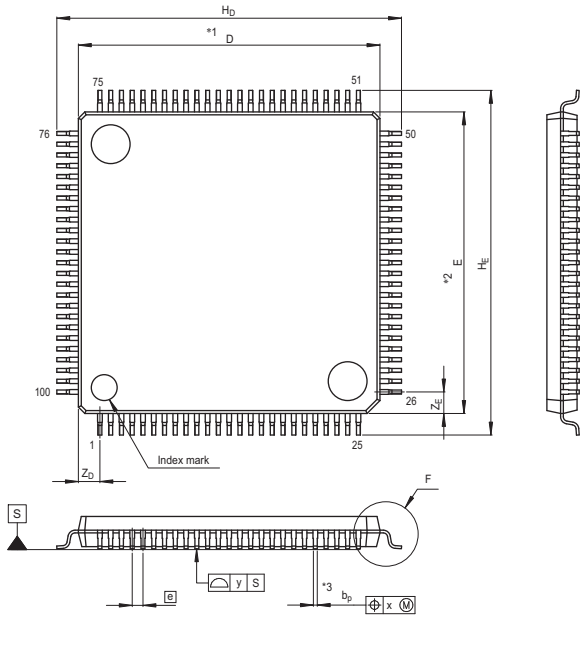
Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N_{PEC} ≤ 100 times	256 bytes	t_{P256}	—	0.9	13.2	—	0.4	6	ms
	8 Kbytes	t_{P8K}	—	29	176	—	13	80	ms
	32 Kbytes	t_{P32K}	—	116	704	—	52	320	ms
Programming time N_{PEC} > 100 times	256 bytes	t_{P256}	—	1.1	15.8	—	0.5	7.2	ms
	8 Kbytes	t_{P8K}	—	35	212	—	16	96	ms
	32 Kbytes	t_{P32K}	—	140	848	—	64	384	ms
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	71	216	—	39	120	ms
	32 Kbytes	t_{E32K}	—	254	864	—	141	480	ms
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	85	260	—	47	144	ms
	32 Kbytes	t_{E32K}	—	304	1040	—	169	576	ms
Reprogramming/erasure cycle*1		N_{PEC}	1000*2	—	—	1000*2	—	—	Times
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	120	µs
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	120	µs
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	ms
Forced stop command		t_{FD}	—	—	32	—	—	20	µs
Data hold time*3		t_{DRP}	10	—	—	10	—	—	Year
FCU reset time		t_{FCUR}	35	—	—	35	—	—	µs

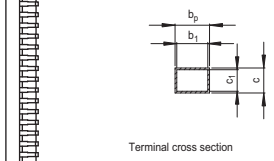
Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 32 times for different addresses in 8-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

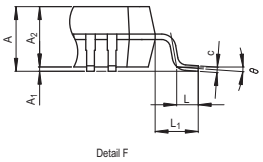
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure G 100-Pin LFQFP (PLQP0100KB-A)