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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	552K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 29x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f564mlhdlc-21

Table 1.1 Outline of Specifications (9/9)

Classification	Module/Function	Description
Encryption function	AES* ³	<ul style="list-style-type: none"> • Key lengths: 128, 192, and 256 bits • Support for CBC, ECB, CFB, OFB, CTR, and CMAC operating modes • Speed of calculations: 128-bit key length in 22 cycles 192-bit key length in 26 cycles 256-bit key length in 30 cycles • Compliant with FIPS PUB 197
	DES* ³	<ul style="list-style-type: none"> • Key lengths: 56 bits (DES)/3 × 56 bits (T-DES) • Support for DES and triple DES • Support for ECB and CBC operating modes • Speed of calculations: 6 clock cycles in single DES mode 14 clock cycles in triple DES mode • Compliant with FIPS PUB 46-3 • Compliant with FIPS PUB 81
	SHA* ³	<ul style="list-style-type: none"> • Support for SHA-1 (128), SHA-2 (224 or 256), and HMAC (160, 224, or 256) • Speed of calculations: 50 clock cycles in SHA-1 mode 42 clock cycles in SHA-224 mode 42 clock cycles in SHA-256 mode • Compliant with SHA as defined in FIPS PUB 180-1 and -2 • Compliant with HMAC as defined in FIPS PUB 198
	True random number generator (RNG)* ³	<ul style="list-style-type: none"> • Length of random numbers: 16 bits • Generation of random-number-generated interrupts after a number is generated • Random number generation time: 3.6 ms (typ)
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, VCC_USBA = AVCC_USBA = 2.7 to 3.6 V, V _{BATT} = 2.0 to 3.6 V
Operating temperature		D-version: -40 to +85°C G-version: -40 to +105°C (in planning)
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) 100-pin LQFP (PLQP0100KB-A)
On-chip debugging system		<ul style="list-style-type: none"> • E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.

Note 2. Setting is only possible when the input sampling rate 44.1 kHz is selected.

Note 3. The product part number differs according to whether or not it supports encryption.

Note 4. The product part number differs according to whether or not it includes an SDHI (SD host interface).

Table 1.3 List of Products (3/3)

Group	Part No.	Package	Code Flash Memory Capacity	RAM Capacity	Data Flash Memory Capacity	Operating Frequency (Max.)	Encryption Module	SDHI
RX64M	R5F564MFCDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDLK	PTLG0145KA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MLCDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MLDDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MLGDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MLHDLJ	PTLG0100JA-A	4 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MJCDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MJDDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MJGDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MJHDLJ	PTLG0100JA-A	3 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MGCDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MGDDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MGGDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MGHDLJ	PTLG0100JA-A	2.5 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available
	R5F564MFCDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Not supported
	R5F564MFDDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Not supported	Available
	R5F564MFGDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Not supported
	R5F564MFHDLJ	PTLG0100JA-A	2 Mbytes	512 Kbytes	64 Kbytes	120 MHz	Available	Available

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (1/7)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
1	AVSS0							
2		P05					IRQ13	DA1
3	AVCC1							
4		P03					IRQ11	DA0
5	AVSS1							
6		P02		TMCI1	SCK6		IRQ10	AN120
7		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN119
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN118
9		PF5					IRQ4	
10	EMLE							
11		PJ5		POE8#	CTS2#/RTS2#/SS2#			
12	VSS							
13		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/ CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#			
14	VCL							
15	VBATT							
16	NC							
17	TRST#	PF4						
18	MD/FINED							
19	XCIN							
20	XCOUT							
21	RES#							
22	XTAL	P37						
23	VSS							
24	EXTAL	P36						
25	VCC							
26	UPSEL	P35					NMI	
27		P34		MTIOC0A/TMCI3/ PO12/POE10#	SCK6/SCK0/ ET0_LINKSTA		IRQ4	
28		P33	EDREQ1	MTIOC0D/TIOC0D/ TMRI3/PO11/POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0	PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOC0C/ TMO3/PO10/ RTCOUT/RTCIC2/ POE0#/POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB_VBUSEN	VSYNC	IRQ2-DS	
30	TMS	PF3						
31	TDI	PF2			RXD1/SMISO1/ SSCL1			
32		P31		MTIOC4D/TMCI2/ PO9/RTCIC1	CTS1#/RTS1#/ SS1#/ET1_MDC		IRQ1-DS	
33		P30		MTIOC4B/TMRI3/ PO8/RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/ ET1_MDIO		IRQ0-DS	
34	TCK	PF1			SCK1			
35	TDO	PF0			TXD1/SMOSI1/ SSDA1			

Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA) (2/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
C9		PD7	D7[A7/D7]	MTIC5U/POE0#		MMC_D1-B/ SDHI_D1-B/ QIO1-B/QMI-B	IRQ7	AN107
C10		P63	CS3#/CAS#					
C11		PE0	D8[A8/D8]	MTIOC3D/ GTIOC2B-A	SCK12	MMC_D4-B		ANEX0
C12		P70	SDCLK					
C13	VSS							
D1		P00		TMR10	TXD6/SMOSI6/SSDA6		IRQ8	AN118
D2		PF5					IRQ4	
D3		P03					IRQ11	DA0
D4		P01		TMC10	RXD6/SMISO6/SSCL6		IRQ9	AN119
D5	VCC							
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#			AN117
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/ POE10#		MMC_CLK-B/ SDHI_CLK-B/ QSPCLK-B	IRQ5	AN113
D8		P60	CS0#					
D9		P64	CS4#/WE#					
D10		PE7	D15[A15/D15]	MTIOC6A/ GTIOC3A-E/TOC1		MMC_RES#-B/ SDHI_WP-B	IRQ7	AN105
D11	VCC							
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ GTIOC0A-A	ET0_RX_CLK/ REF50CK0		IRQ5	AN103
D13		PE6	D14[A14/D14]	MTIOC6C/GTIOC3B- E/TIC1		MMC_CD-B/ SDHI_CD-B	IRQ6	AN104
E1	VSS							
E2	VCL							
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#			
E4	EMLE							
E5		P44					IRQ12- DS	AN004
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/ GTIOC0B-C/TIOCA0/ CACREF/PO16	SSLA1-B/ ET0_TX_EN/ RMII0_TXD_EN			
E11		P66	CS6#/DQM0	MTIOC7D/ GTIOC2B-C	CTX2			
E12		P65	CS5#/CKE					
E13		P67	CS7#/DQM1	MTIOC7C/ GTIOC1B-C	CRX2		IRQ15	
F1	XCIN							
F2	XCOU							
F3		PJ3	EDACK1	MTIOC3C	ET0_EXOUT/CTS6#/ RTS6#/CTS0#/RTS0#/ SS6#/SS0#			
F4	VBATT							
F10		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET0_MDIO		IRQ6-DS	
F11	VSS							
F12		PA1	A1	MTIOC0B/MTCLKC/ MTIOC7B/ GTIOC2A-C/TIOC0B/ PO17	SCK5/SSLA2-B/ ET0_WOL		IRQ11	

Table 1.8 List of Pin and Pin Functions (144-Pin LFQFP) (2/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SC1g, SC1h, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
36		P21		MTIOC1B/MTIOC4A/ GTIOC2A-B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN/ SSIWS0	PIXD5	IRQ9	
37		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/USB0_ID/ SSIRXD0	PIXD4	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ MTIOC4B/ GTIOC0B-B/TIOCB0/ TCLKD/TMO1/PO15/ POE8#	SCK1/TXD3/SMOSI3/ SSDA3/SDA2-DS/ SSITXD0	PIXD3	IRQ7	ADTRG1#
39		P87		MTIOC4C/ GTIOC1B-B/TIOCA2	TXD10	PIXD2		
40		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
41		P86		MTIOC4D/ GTIOC2B-B/TIOCA0	RXD10	PIXD1		
42		P15		MTIOC0B/MTCLKB/ GTETR-G/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1	PIXD0	IRQ5	
43		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
44		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
45		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
46	VCC_USB							
47					USB0_DM			
48					USB0_DP			
49	VSS_USB							
50		P56	EDACK1	MTIOC3C/TIOCA1				
51	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
52	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
53		P53*1	BCLK					
54		P52	RD#		RXD2/SMISO2/SSCL2			
55		P51	WR1#/BC1#/ WAIT#		SCK2			
56		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
57	VSS							
58	TRCLK	P83	EDACK1	MTIOC4C/ GTIOC0A-D	CTS10#/ET0_CRS/ RMII0_CRS_DV/ SCK10			
59	VCC							
60	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL	MMC_D7-A	IRQ14	
61		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3	MMC_D6-A	IRQ13	
62		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2	MMC_D5-A		

Table 1.9 List of Pin and Pin Functions (100-Pin TFLGA) (4/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SCIG, SCIH, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
H9		PB6	A14	MTIOC3D/TIOCA5/PO30	RXD9/ET0_ETXD1/RMII0_TXD1			
H10		PB7	A15	MTIOC3B/TIOCB5/PO31	TXD9/ET0_CRS/RMII0_CRS_DV			
J1		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/SSISCK1			
J2		P21		MTIOC1B/MTIOC4A/GTIOC2A-B/TIOCA3/TMCI0/PO1	RXD0/SMISO0/SSCL0/USB0_EXICEN/SSIWS0		IRQ9	
J3		P17		MTIOC3A/MTIOC3B/MTIOC4B/GTIOC0B-B/TIOCB0/TCLKD/TMO1/PO15/POE8#	SCK1/TXD3/SMOSI3/SSDA3/SDA2-DS/SSITXD0		IRQ7	ADTRG1#
J4		P13		MTIOC0B/TIOCA5/TMO3/PO13	TXD2/SMOSI2/SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
J5	VSS_USB							
J6	VCC_USB							
J7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
J8		PC4	A20/CS3#	MTIOC3D/MTCLKC/GTETR-D/TMCI1/PO25/POE0#	SCK5/CTS8#/SSLA0-A/ET0_TX_CLK			
J9		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/SSLA1-A/ET0_ERXD3		IRQ14	
J10		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2-A/ET0_ERXD2		IRQ12	
K1		P23	EDACK0	MTIOC3D/MTCLKD/GTIOC0A-B/TIOCD3/PO3	TXD3/CTS0#/RTS0#/SMOSI3/SS0#/SSDA3/SSISCK0			
K2		P22	EDREQ0	MTIOC3B/MTCLKC/GTIOC1A-B/TIOCC3/TMO0/PO2	SCK0/USB0_OVRCURB/AUDIO_MCLK			
K3		P20		MTIOC1A/TIOCB3/TMRI0/PO0	TXD0/SMOSI0/SSDA0/USB0_ID/SSIRXD0		IRQ8	
K4		P14		MTIOC3A/MTCLKA/TIOCB5/TCLKA/TMRI2/PO15	CTS1#/RTS1#/SS1#/CTX1/USB0_OVRCURA		IRQ4	
K5					USB0_DM			
K6					USB0_DP			
K7		P51	WR1#/BC1#/WAIT#		SCK2			
K8		PC5	A21/CS2#/WAIT#	MTIOC3B/MTCLKD/GTIOC1A-D/TMRI2/PO29	SCK8/RSPCKA-A/RTS8#/ET0_ETXD2			
K9		PC3	A19	MTIOC4D/GTIOC1B-D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ET0_TX_ER			
K10		PC2	A18	MTIOC4B/GTIOC2B-D/TCLKA/PO21	RXD5/SMISO5/SSCL5/SSLA3-A/ET0_RX_DV			

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.10 List of Pin and Pin Functions (100-Pin LQFP) (2/4)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timer (MTU, GPT, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	Communication (ETHERC, SClg, SClh, RSPI, RIIC, CAN, USB, SSI)	Memory Interface Camera Interface (QSPI, SDHI, MMCIF, PDC)	Interrupt	S12ADC, R12DA
30		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#
31		P15		MTIOC0B/MTCLKB/ GTETR-G/TIOCB2/ TCLKB/TMCI2/PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ SSIWS1		IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/ TMRI2/PO15	CTS1#/RTS1#/SS1#/ CTX1/ USB0_OVRCURA		IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]		IRQ3	ADTRG1#
34		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]		IRQ2	
35	VCC_USB							
36					USB0_DM			
37					USB0_DP			
38	VSS_USB							
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET0_EXOUT		IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET0_LINKSTA			
41		P53*1	BCLK					
42		P52	RD#		RXD2/SMISO2/SSCL2			
43		P51	WR1#/BC1#/ WAIT#		SCK2			
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2			
45	UB	PC7	A23/CS0#	MTIOC3A/MTCLKB/ GTIOC3A-D/TMO2/ TOC0/PO31/CACREF	TXD8/MISOA-A/ ET0_COL		IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ GTIOC3B-D/TMCI2/ TIC0/PO30	RXD8/MOSIA-A/ ET0_ETXD3		IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ GTIOC1A-D/TMRI2/ PO29	SCK8/RSPCKA-A/ RTS8#/ET0_ETXD2			
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ GTETR-G/TMCI1/ PO25/POE0#	SCK5/CTS8#/ SSLA0-A/ ET0_TX_CLK			
49		PC3	A19	MTIOC4D/ GTIOC1B-D/TCLKB/ PO24	TXD5/SMOSI5/ SSDA5/ET0_TX_ER			
50		PC2	A18	MTIOC4B/ GTIOC2B-D/TCLKA/ PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ ET0_RX_DV			
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2-A/ ET0_ERXD2		IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1-A/ET0_ERXD3		IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/ET0_CRS/ RMII0_CRS_DV			
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/ET0_ETXD1/ RMII0_TXD1			
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE4#	SCK9/RTS9#/ ET0_ETXD0/ RMII0_TXD0			
56		PB4	A12	TIOCA4/PO28	CTS9#/ET0_TX_EN/ RMII0_TXD_EN			

Table 4.1 List of I/O Registers (Address Order) (8 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK		MPU
0008 7010h to 0008 70FFh	ICU	Interrupt Request Registers 016 to 255	IR016 to 255	8	8	2 ICLK		ICUA
0008 711Ah to 0008 71FFh	ICU	DTC Transfer Request Enable Registers 026 to 255	DTCE026 to DTCE255	8	8	2 ICLK		ICUA
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Registers 02 to 1F	IER02 to IER1F	8	8	2 ICLK		ICUA
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8	2 ICLK		ICUA
0008 72E1h	ICU	Software Interrupt 2 Generation Register	SWINT2R	8	8	2 ICLK		ICUA
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16	2 ICLK		ICUA
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Registers 000 to 255	IPR000 to IPR255	8	8	2 ICLK		ICUA
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8	2 ICLK		ICUA
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8	2 ICLK		ICUA
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8	2 ICLK		ICUA
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8	2 ICLK		ICUA
0008 7410h	ICU	DMAC Trigger Select Register 4	DMRSR4	8	8	2 ICLK		ICUA
0008 7414h	ICU	DMAC Trigger Select Register 5	DMRSR5	8	8	2 ICLK		ICUA
0008 7418h	ICU	DMAC Trigger Select Register 6	DMRSR6	8	8	2 ICLK		ICUA
0008 741Ch	ICU	DMAC Trigger Select Register 7	DMRSR7	8	8	2 ICLK		ICUA
0008 7500h to 0008 750Fh	ICU	IRQ Control Registers 0 to 15	IRQCR0 to 15	8	8	2 ICLK		ICUA
0008 7520h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUA
0008 7521h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK		ICUA
0008 7528h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK		ICUA
0008 752Ah	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK		ICUA
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK		ICUA
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK		ICUA
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK		ICUA
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK		ICUA
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK		ICUA
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK		ICUA
0008 7600h	ICU	Group BE0 Interrupt Request Register	GRPBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7630h	ICU	Group BL0 Interrupt Request Register	GRPBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7634h	ICU	Group BL1 Interrupt Request Register	GRPBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7640h	ICU	Group BE0 Interrupt Request Enable Register	GENBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7670h	ICU	Group BL0 Interrupt Request Enable Register	GENBL0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7674h	ICU	Group BL1 Interrupt Request Enable Register	GENBL1	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7680h	ICU	Group BE0 Interrupt Clear Register	GCRBE0	32	32	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7700h	ICU	Software Configurable Interrupt B Request Register 0	PIBR0	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7701h	ICU	Software Configurable Interrupt B Request Register 1	PIBR1	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7702h	ICU	Software Configurable Interrupt B Request Register 2	PIBR2	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7703h	ICU	Software Configurable Interrupt B Request Register 3	PIBR3	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7704h	ICU	Software Configurable Interrupt B Request Register 4	PIBR4	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7705h	ICU	Software Configurable Interrupt B Request Register 5	PIBR5	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA
0008 7706h	ICU	Software Configurable Interrupt B Request Register 6	PIBR6	8	8	2 ICLK to 1 PCLKB	2 ICLK	ICUA

Table 4.1 List of I/O Registers (Address Order) (17 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8310h	RIIC0	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8311h	RIIC0	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8312h	RIIC0	I ² C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8313h	RIIC0	I ² C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8340h	RIIC2	I ² C-Bus Control Register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8341h	RIIC2	I ² C-Bus Control Register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8342h	RIIC2	I ² C-Bus Mode Register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8343h	RIIC2	I ² C-Bus Mode Register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8344h	RIIC2	I ² C-Bus Mode Register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8345h	RIIC2	I ² C-Bus Function Enable Register	ICFER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8346h	RIIC2	I ² C-Bus Status Enable Register	ICSER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8347h	RIIC2	I ² C-Bus Interrupt Enable Register	ICIER	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8348h	RIIC2	I ² C-Bus Status Register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8349h	RIIC2	I ² C-Bus Status Register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ah	RIIC2	Slave Address Register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Bh	RIIC2	Slave Address Register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Ch	RIIC2	Slave Address Register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Dh	RIIC2	Slave Address Register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Eh	RIIC2	Slave Address Register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 834Fh	RIIC2	Slave Address Register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8350h	RIIC2	I ² C-Bus Bit Rate Low-Level Register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8351h	RIIC2	I ² C-Bus Bit Rate High-Level Register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8352h	RIIC2	I ² C-Bus Transmit Data Register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8353h	RIIC2	I ² C-Bus Receive Data Register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	RIICa
0008 8500h	MMCIF	Command Setting Register	CECMDSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8508h	MMCIF	Argument Register	CEARG	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 850Ch	MMCIF	Automatically Issued CMD12 Argument Register	CEARGCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8510h	MMCIF	Command Control Register	CECMDCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8514h	MMCIF	Transfer Block Setting Register	CEBLOCKSET	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8518h	MMCIF	Clock Control Register	CECLKCTRL	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 851Ch	MMCIF	Buffer Access Setting Register	CEBUFACC	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8520h	MMCIF	Response Register 3	CERESP3	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8524h	MMCIF	Response Register 2	CERESP2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8528h	MMCIF	Response Register 1	CERESP1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 852Ch	MMCIF	Response Register 0	CERESP0	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8530h	MMCIF	Automatically Issued CMD12 Response Register	CERESPCMD12	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8534h	MMCIF	Data Register	CEDATA	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 853Ch	MMCIF	Boot Operation Setting Register	CEBOOT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8540h	MMCIF	Interrupt status Flag Register	CEINT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8544h	MMCIF	Interrupt request Enable Register	CEINTEN	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8548h	MMCIF	Status Register 1	CEHOSTSTS1	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 854Ch	MMCIF	Status Register 2	CEHOSTSTS2	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8570h	MMCIF	MMC Detection and Port Control Register	CEDETECT	32	32	2, 3 PCLKB	2 ICLK	MMCIF
0008 8574h	MMCIF	Special Mode Setting Register	CEADDMODE	32	32	2, 3 PCLKB	2 ICLK	MMCIF

Table 4.1 List of I/O Registers (Address Order) (21 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 9198h	S12AD1	A/D Compare Level Register 0	ADCMPLR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ah	S12AD1	A/D Compare Level Register 1	ADCMPLR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Ch	S12AD1	A/D Compare Data Register 0	ADCMPDR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 919Eh	S12AD1	A/D Compare Data Register 1	ADCMPDR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A0h	S12AD1	A/D Compare Status Register 0	ADCMPSR0	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A2h	S12AD1	A/D Compare Status Register 1	ADCMPSR1	16	16	2, 3 PCLKB	2 ICLK	S12ADC
0008 91A4h	S12AD1	A/D Compare Status Extended Register	ADCMPSER	8	8	2, 3 PCLKB	2 ICLK	S12ADC
0008 9E00h	QSPI	QSPI Control Register	SPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E01h	QSPI	QSPI Slave Select Polarity Register	SSLP	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E02h	QSPI	QSPI Pin Control Register	SPPCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E03h	QSPI	QSPI Status Register	SPSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E04h	QSPI	QSPI Data Register	SPDR	32	8, 16, 32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E08h	QSPI	QSPI Sequence Control Register	SPSCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E09h	QSPI	QSPI Sequence Status Register	SPSSR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ah	QSPI	QSPI Bit Rate Register	SPBR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Bh	QSPI	QSPI Data Control Register	SPDCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Ch	QSPI	QSPI Clock Delay Register	SPCKD	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Dh	QSPI	QSPI Slave Select Negation Delay Register	SSLND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E0Eh	QSPI	QSPI Next-Access Delay Register	SPND	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E10h	QSPI	QSPI Command Register 0	SPCMD0	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E12h	QSPI	QSPI Command Register 1	SPCMD1	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E14h	QSPI	QSPI Command Register 2	SPCMD2	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E16h	QSPI	QSPI Command Register 3	SPCMD3	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E18h	QSPI	QSPI Buffer Control Register	SPBFCR	8	8	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ah	QSPI	QSPI Buffer Data Count Set Register	SPBDCR	16	16	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E1Ch	QSPI	QSPI Transfer Data Length Multiplier Setting Register 0	SPBMUL0	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E20h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 1	SPBMUL1	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E24h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 2	SPBMUL2	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 9E28h	QSPI	QSPI Transfer Data Length Multiplier Setting Register 3	SPBMUL3	32	32	4, 5 PCLKB	2, 3 ICLK	QSPI
0008 A000h	SCIO	Serial Mode Register	SMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A001h	SCIO	Bit Rate Register	BRR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A002h	SCIO	Serial Control Register	SCR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A003h	SCIO	Transmit Data Register	TDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A004h	SCIO	Serial Status Register	SSR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A005h	SCIO	Receive Data Register	RDR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A006h	SMCIO	Smart Card Mode Register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A007h	SCIO	Serial Extended Mode Register	SEMR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh
0008 A008h	SCIO	Noise Filter Setting Register	SNFR	8	8	2, 3 PCLKB	2 ICLK	SClg, SClh

Table 4.1 List of I/O Registers (Address Order) (36 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
0008 C197h	MPC	PA7 Pin Function Control Register	PA7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Ah	MPC	PB2 Pin Function Control Register	PB2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Ch	MPC	PB4 Pin Function Control Register	PB4PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Eh	MPC	PB6 Pin Function Control Register	PB6PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A1h	MPC	PC1 Pin Function Control Register	PC1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A8h	MPC	PD0 Pin Function Control Register	PD0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1A9h	MPC	PD1 Pin Function Control Register	PD1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1AAh	MPC	PD2 Pin Function Control Register	PD2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1ACh	MPC	PD4 Pin Function Control Register	PD4PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1ADh	MPC	PD5 Pin Function Control Register	PD5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1AEh	MPC	PD6 Pin Function Control Register	PD6PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1AFh	MPC	PD7 Pin Function Control Register	PD7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B5h	MPC	PE5 Pin Function Control Register	PE5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B6h	MPC	PE6 Pin Function Control Register	PE6PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B7h	MPC	PE7 Pin Function Control Register	PE7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B8h	MPC	PF0 Pin Function Control Register	PF0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1B9h	MPC	PF1 Pin Function Control Register	PF1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1BAh	MPC	PF2 Pin Function Control Register	PF2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1BDh	MPC	PF5 Pin Function Control Register	PF5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C0h	MPC	PG0 Pin Function Control Register	PG0PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C1h	MPC	PG1 Pin Function Control Register	PG1PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C2h	MPC	PG2 Pin Function Control Register	PG2PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C3h	MPC	PG3 Pin Function Control Register	PG3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C4h	MPC	PG4 Pin Function Control Register	PG4PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C5h	MPC	PG5 Pin Function Control Register	PG5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C6h	MPC	PG6 Pin Function Control Register	PG6PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1C7h	MPC	PG7 Pin Function Control Register	PG7PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C1D5h	MPC	PJ5 Pin Function Control Register	PJ5PFS	8	8	2, 3 PCLK	2 ICLK	MPC
0008 C280h	SYSTM	Deep Standby Control Register	DPSBYCR	8	8	4, 5 PCLK	2, 3 ICLK	Low Power Consumption

Table 4.1 List of I/O Registers (Address Order) (59 / 67)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function
						ICLK ≥ PCLK	ICLK < PCLK	
000C 4C50h	EPTPC 1	Announce Message Flag Field Setting Register	ANFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C54h	EPTPC 1	Sync Message Flag Field Setting Register	SYNFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C58h	EPTPC 1	Delay_Req Message Flag Field Setting Register	DYRQFR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C5Ch	EPTPC 1	Delay_Resp Message Flag Field Setting Register	DYRPFRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C60h	EPTPC 1	SYNFP Local Clock ID Registers	SYCIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C64h	EPTPC 1	SYNFP Local Clock ID Registers	SYCIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C68h	EPTPC 1	SYNFP Local Port Number Register	SYPNUMR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C80h	EPTPC 1	SYNFP Register Value Load Directive Register	SYRVLDR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C90h	EPTPC 1	SYNFP Reception Filter Register 1	SYRFL1R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C94h	EPTPC 1	SYNFP Reception Filter Register 2	SYRFL2R	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4C98h	EPTPC 1	SYNFP Transmission Enable Register	SYTRENRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CA0h	EPTPC 1	Master Clock ID Register	MTCIDU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CA4h	EPTPC 1	Master Clock ID Register	MTCIDL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CA8h	EPTPC 1	Master Clock Port Number Register	MTPID	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CC0h	EPTPC 1	SYNFP Transmission Interval Setting Register	SYTLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CC4h	EPTPC 1	SYNFP Received logMessageInterval Value Indication Register	SYRLIR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CC8h	EPTPC 1	offsetFromMaster Value Register	OFMRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CCCh	EPTPC 1	offsetFromMaster Value Register	OFMRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CD0h	EPTPC 1	meanPathDelay Value Register	MPDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CD4h	EPTPC 1	meanPathDelay Value Register	MPDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CE0h	EPTPC 1	grandmasterPriority Field Setting Register	GMPR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CE4h	EPTPC 1	grandmasterClockQuality Field Setting Register	GMCQR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CE8h	EPTPC 1	grandmasterIdentity Field Setting Registers	GMIDRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CECh	EPTPC 1	grandmasterIdentity Field Setting Registers	GMIDRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CF0h	EPTPC 1	currentUtcOffset/timeSource Field Setting Register	CUOTSR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4CF4h	EPTPC 1	stepsRemoved Field Setting Register	SRR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D00h	EPTPC 1	PTP-primary Message Destination MAC Address Setting Registers	PPMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D04h	EPTPC 1	PTP-primary Message Destination MAC Address Setting Registers	PPMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D08h	EPTPC 1	PTP-pdelay Message MAC Address Setting Registers	PDMACRU	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D0Ch	EPTPC 1	PTP-pdelay Message MAC Address Setting Registers	PDMACRL	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC
000C 4D10h	EPTPC 1	PTP Message EtherType Setting Register	PETYPERR	32	32	9 to 211 PCLKA	2 to 106 ICLK	EPTPC

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V $I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins and ETHERC output pin)	V_{OL}	—	—	0.5	V $I_{OL} = 1.0$ mA
	RIIC output pin		—	—	0.4	$I_{OL} = 3.0$ mA
			—	—	0.6	$I_{OL} = 6.0$ mA
	RIIC output pin (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V $I_{OL} = 15.0$ mA (ICFER.FMPE = 1)
	—		0.4	—	$I_{OL} = 20.0$ mA (ICFER.FMPE = 1)	
	ETHERC output pin	V_{OL}	—	—	0.4	V $I_{OL} = 1.0$ mA
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	$ I_{in} $	—	—	1.0	μ A $V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$ I_{TSI} $	—	—	1.0	μ A $V_{in} = 0$ V $V_{in} = V_{CC}$
	Ports for 5 V tolerant		—	—	5.0	$V_{in} = 0$ V $V_{in} = 5.5$ V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	-300	—	-10	μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μ A $V_{in} = V_{CC}$
Input capacitance	All input pins (except for ports 03, 05, 12, 13, 16, 17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM)	C_{in}	—	—	8	μ F $V_{bias} = 0$ V $V_{amp} = 20$ mV $f = 1$ MHz $T_a = 25^\circ$ C
	Ports 03, 05, 12, 13, 16, 17, EMLE, BSCANP, USB0_DP, USB0_DM, USBA_DP, and USBA_DM		—	—	16	

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when $V_{in} = 0$ V.

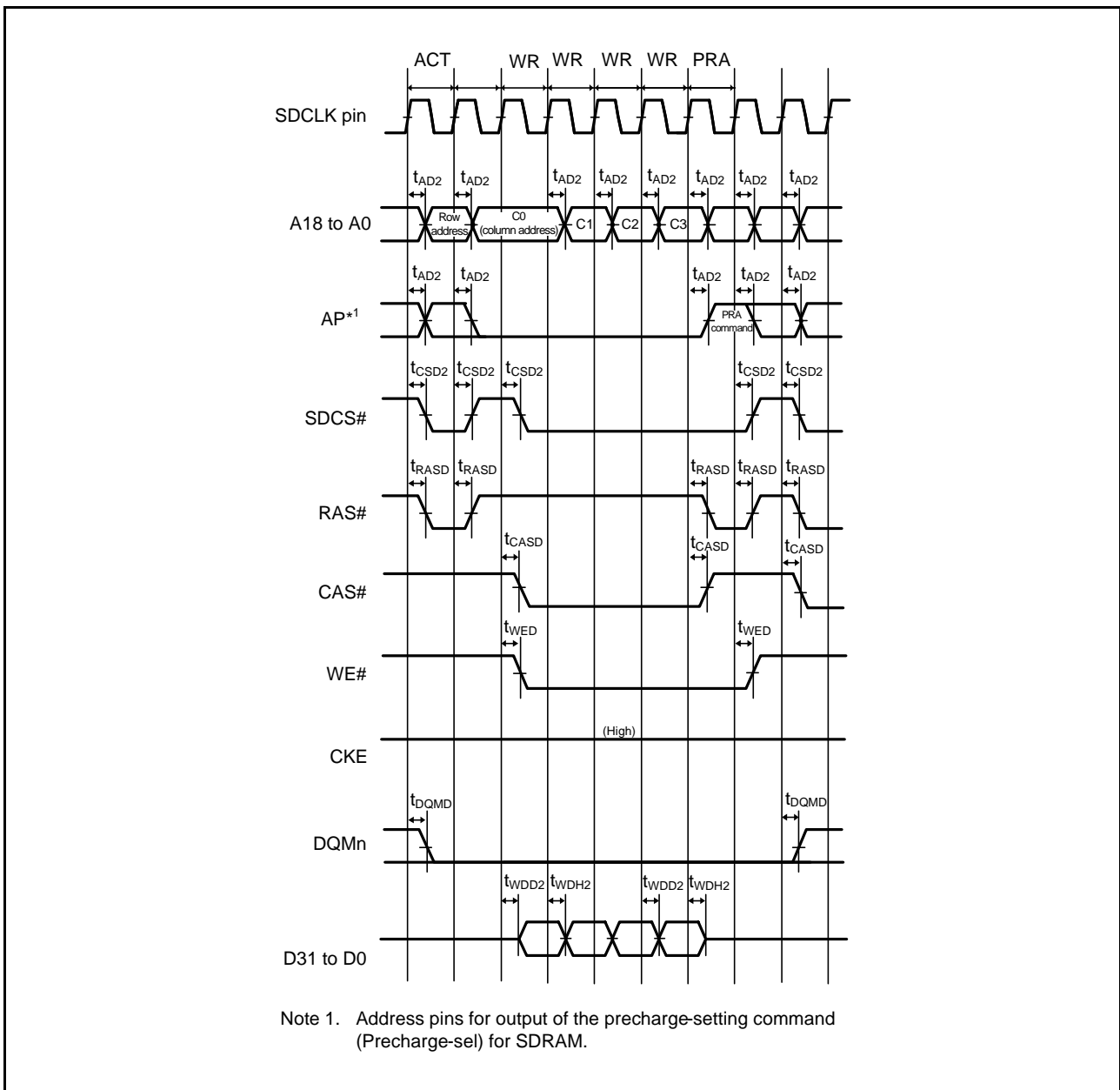


Figure 5.26 SDRAM Space Multiple Write Bus Timing

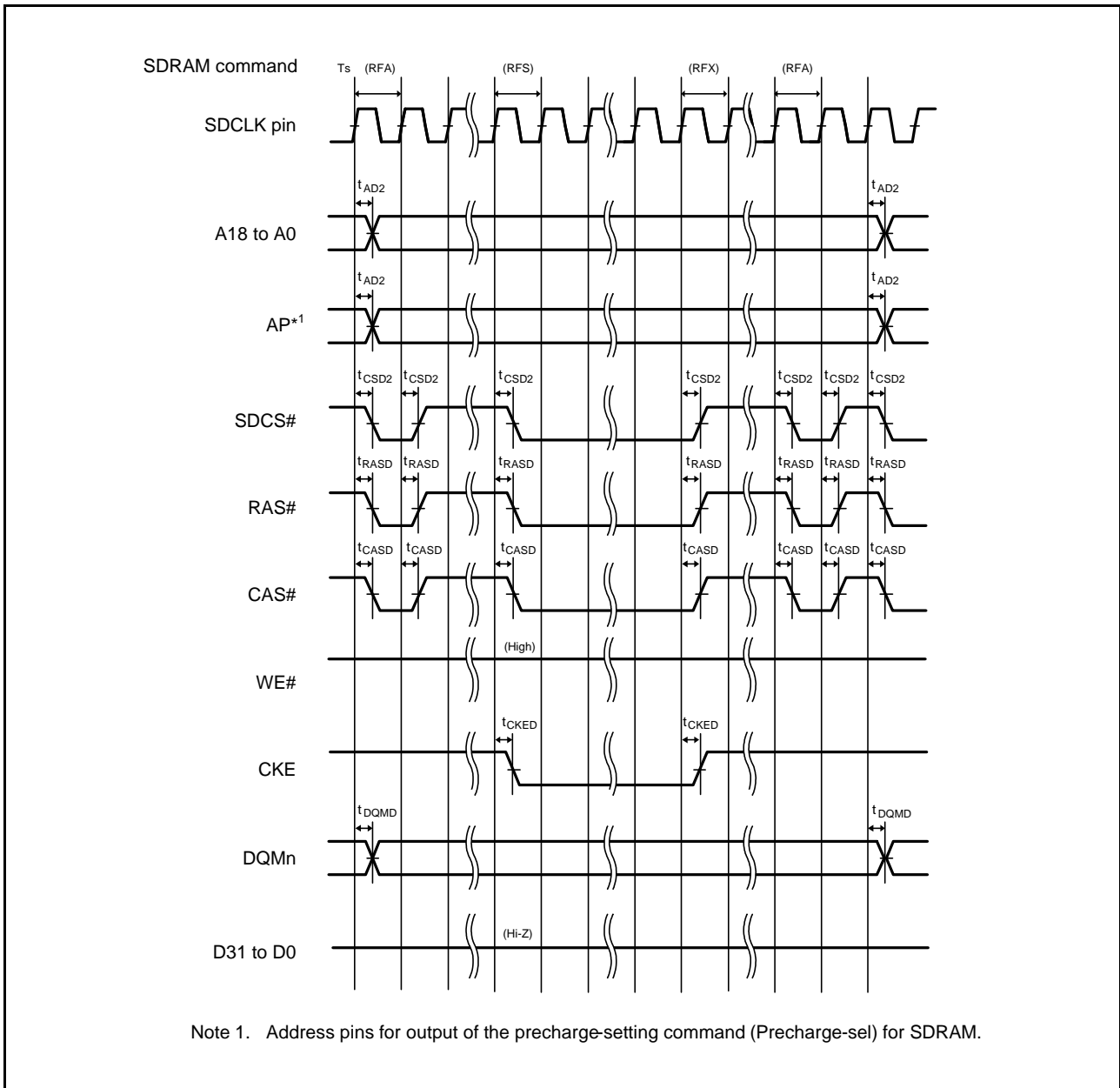


Figure 5.29 SDRAM Space Self-Refresh Bus Timing

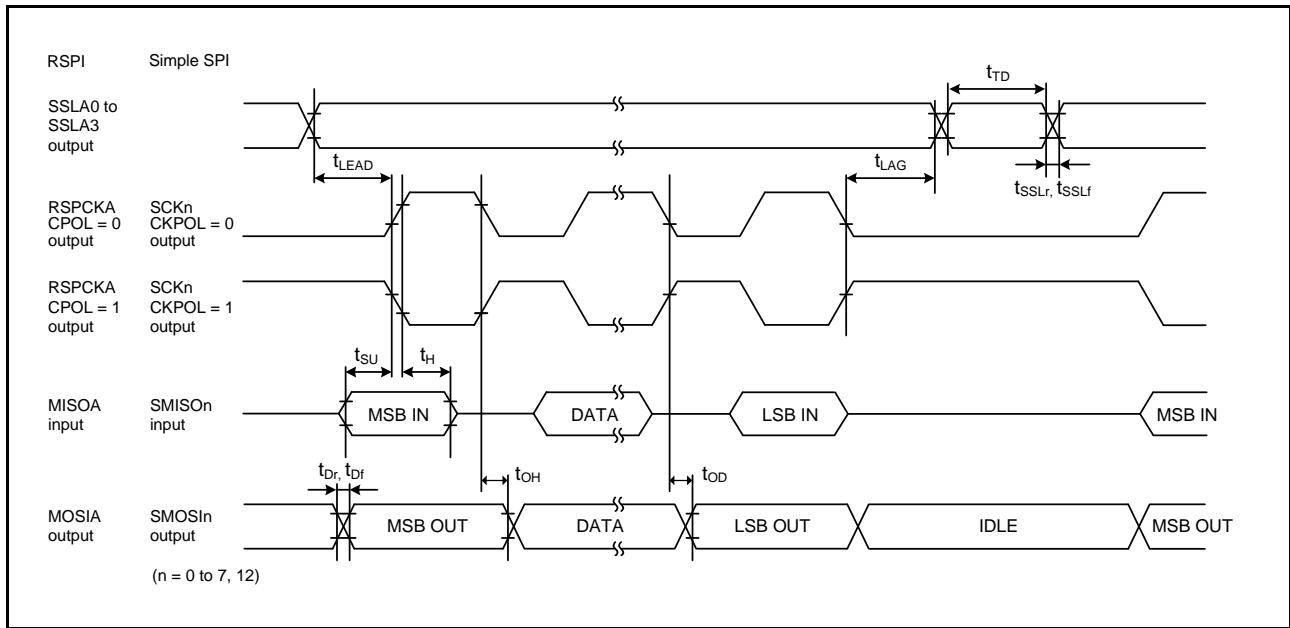


Figure 5.47 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

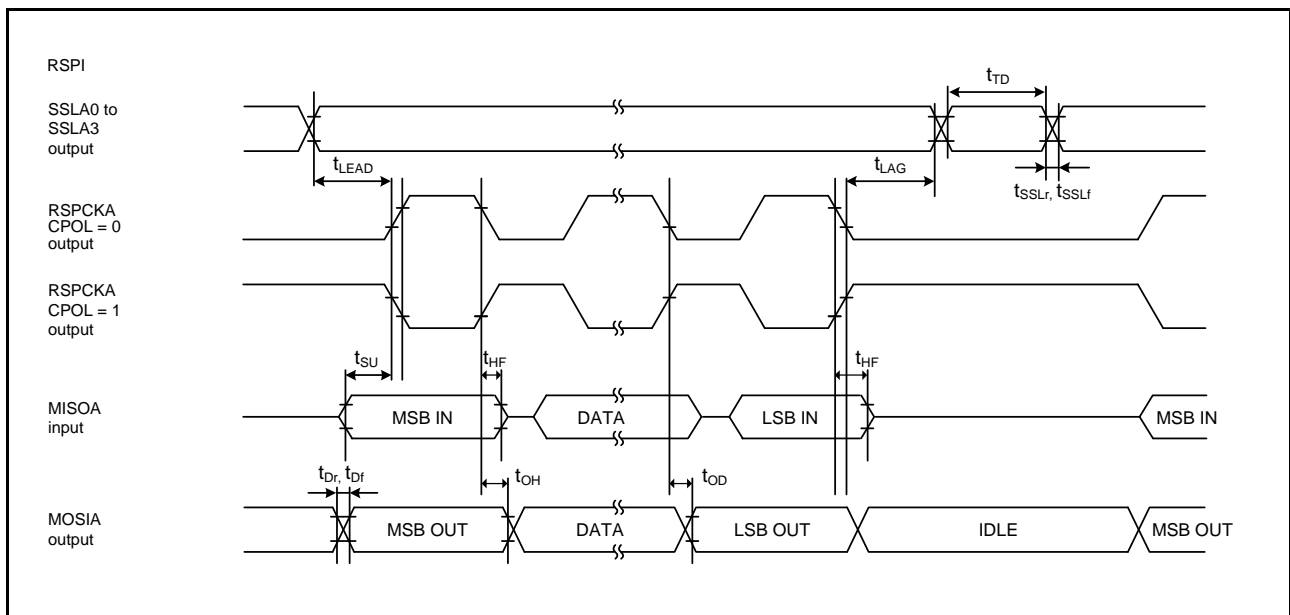


Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Division Ratio Set to 1/2)

Table 5.37 RIIC Timing (2)

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V,
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $T_a = T_{opr}$
 High-drive output is selected by the driving ability control register.

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.56
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 20$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{PBcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle, t_{PBcyc} : PCLKB cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

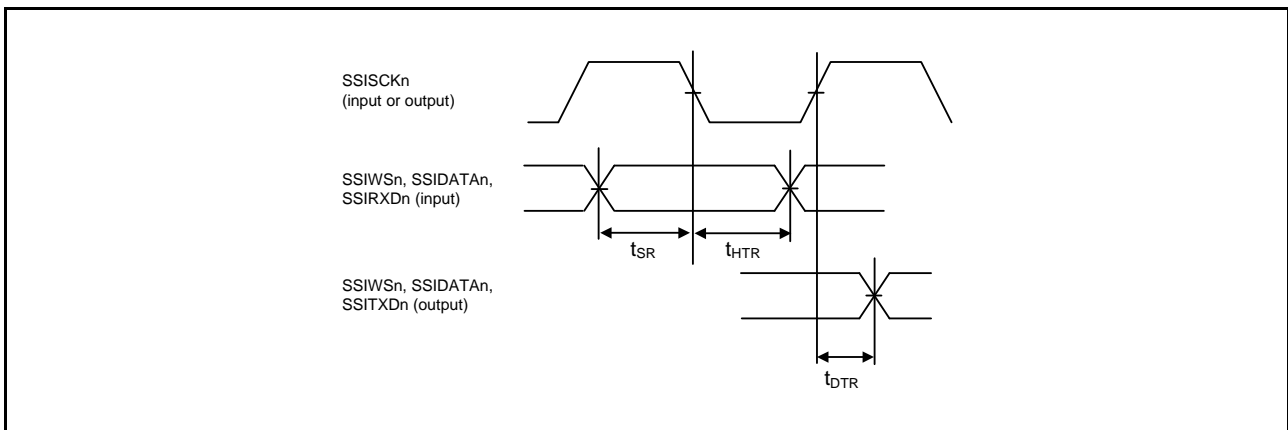


Figure 5.59 Transmit/Receive Timing (SSISCKn Falling Synchronous)

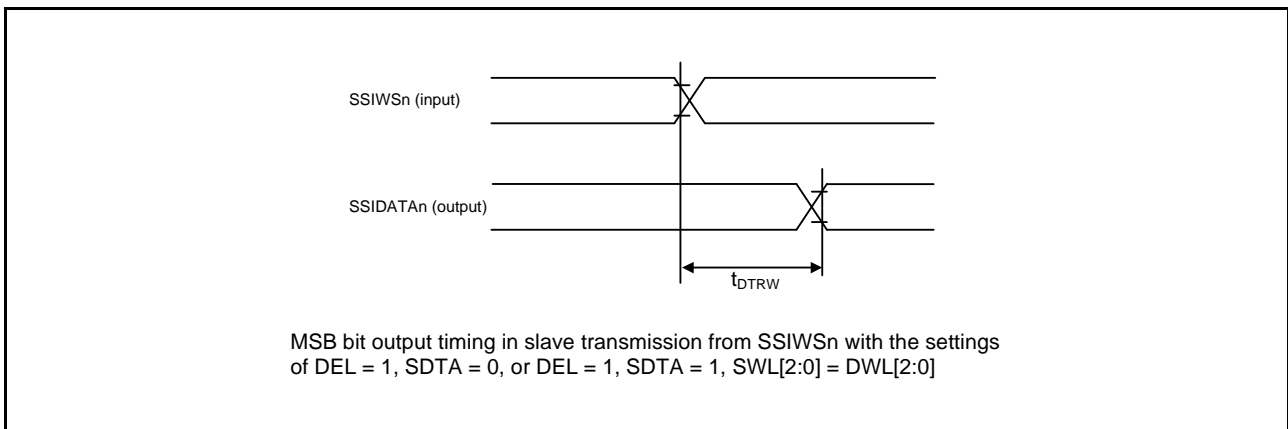


Figure 5.60 SSIDATA Output Delay from SSIWSn Change Edge

Table 5.54 Data Flash Memory Characteristics

Conditions: $V_{CC} = AVCC0 = AVCC1 = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AVCC0$,
 $V_{CC_USBA} = AVCC_USBA = 3.0$ to 3.6 V
 $V_{SS} = AVSS0 = AVSS1 = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms
Erasure time	64 bytes	t_{DE64}	—	3.1	18	—	1.7	10	ms
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	30	μs
	64 bytes	t_{DBC64}	—	—	280	—	—	100	μs
	2 Kbytes	t_{DBC2K}	—	—	6169	—	—	2200	μs
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	—
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t_{DSESD1}	—	—	216	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t_{DSESD2}	—	—	300	—	—	300	μs
Suspend delay time during erasing (in erasure priority mode)		t_{DSEED}	—	—	300	—	—	300	μs
Forced stop command		t_{FD}	—	—	32	—	—	20	μs
Data hold time*3		t_{DDRP}	10	—	—	10	—	—	—

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times ($n = 100000$), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming (guaranteed range is from 1 to the value of the minimum value).

Note 3. This shows the characteristics when reprogramming is performed within the specified range, including the minimum value.

5.12 Boundary Scan

Table 5.55 Boundary Scan Characteristics

Conditions: $V_{CC} = AV_{CC0} = AV_{CC1} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $2.7 \leq V_{REFH0} \leq AV_{CC0}$,
 $V_{CC_USBA} = AV_{CC_USBA} = 3.0$ to 3.6 V,
 $V_{SS} = AV_{SS0} = AV_{SS1} = V_{REFL0} = V_{SS_USB} = V_{SS1_USBA} = V_{SS2_USBA} = PV_{SS_USBA} = AV_{SS_USBA} = 0$ V,
 $T_a = T_{opr}$
 Output load conditions: $V_{OH} = V_{CC} \times 0.5$, $V_{OL} = V_{CC} \times 0.5$, $C = 30$ pF
 High-drive output is selected by the driving ability control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.86
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.87
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.88
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

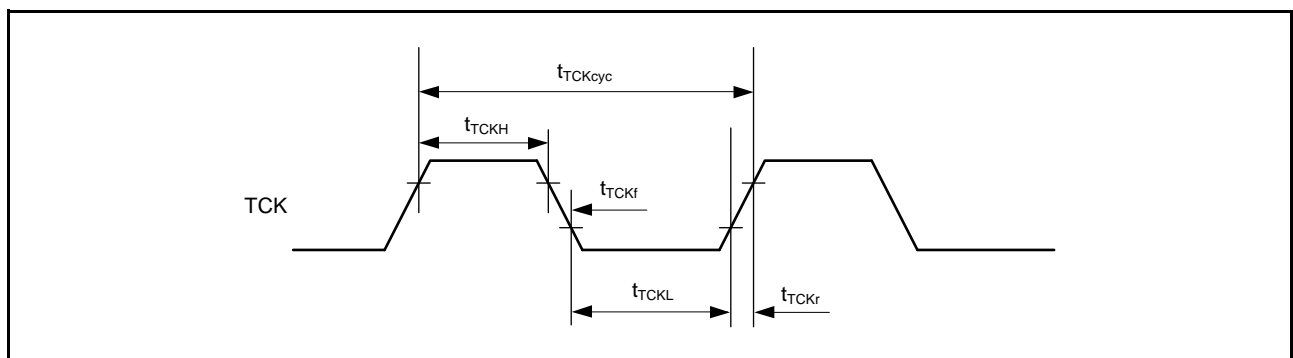


Figure 5.86 Boundary Scan TCK Timing

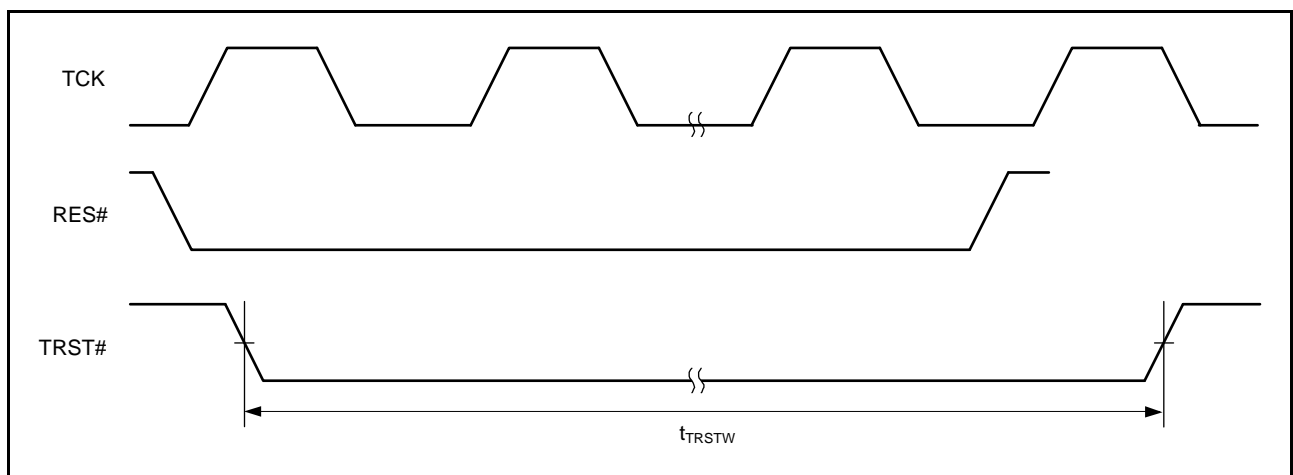


Figure 5.87 Boundary Scan TRST# Timing