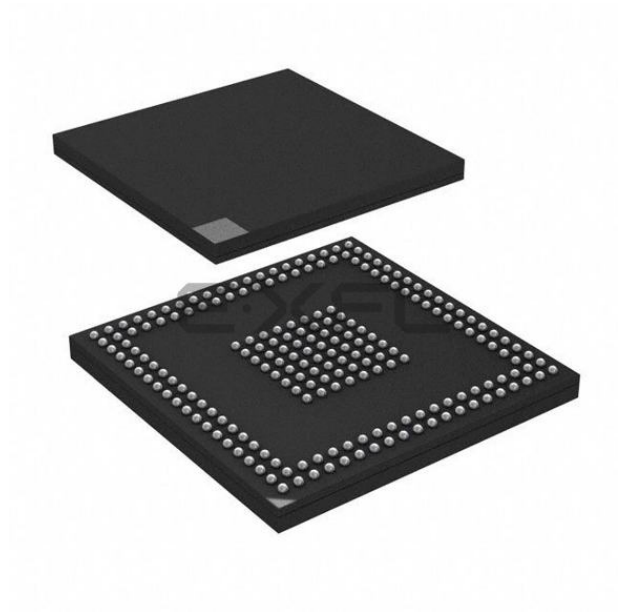

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf534wybcz4b03

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost, and performance off-chip memory systems. (See Figure 3).

The on-chip L1 memory system is the highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 516M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have three blocks of on-chip memory providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 64K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM, and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank, and the SDRAM controller supports up to 4 internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The Blackfin processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the Blackfin processor is configured to boot from boot ROM

Table 3. System Interrupt Controller (SIC) (Continued)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
DMA Channels 12 and 13 (Memory DMA Stream 0)	IVG13	29
DMA Channels 14 and 15 (Memory DMA Stream 1)	IVG13	30
Software Watchdog Timer	IVG13	31
Port F Interrupt B	IVG13	31

Event Control

The Blackfin processor provides a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC interrupt mask register (SIC_IMASK) – Controls the masking and unmasking of each peripheral interrupt event. When a bit is set in the register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wake-up enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. (For more information, see Dynamic Power Management on Page 13.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The Blackfin processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC (ADSP-BF536 and ADSP-BF537 only), SPORTs, SPI port, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors also have an external DMA controller capability via dual external DMA request pins when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals such as USB 2.0. It allows control of the number of data transfers for memDMA. The number of transfers per edge is programmable. This feature can be programmed to allow memDMA to have an increased priority on the external bus relative to the core.

REAL-TIME CLOCK

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day, while the second alarm is for a day and time of that day.

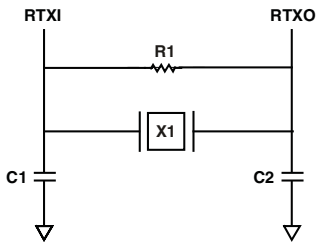
The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wake-up event. Additionally, an RTC wake-up event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from the hibernate operating mode.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 4.

WATCHDOG TIMER

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 4. External Components for RTC

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the processor. Eight timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic interrupts in an operating system.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

CONTROLLER AREA NETWORK (CAN)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors offer a CAN controller that is a communication controller implementing the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well-suited for control applications due to its capability to communicate reliably over a network, since the protocol incorporates CRC checking message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (eight receive only, eight transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wake-up from hibernation mode (lowest static power consumption mode).
- Interrupts, including: Tx complete, Rx complete, error, global.

The electrical characteristics of each network connection are very demanding so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high-speed, fault-tolerant, single-wire transceivers.

TWI CONTROLLER INTERFACE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

10/100 ETHERNET MAC

The ADSP-BF536 and ADSP-BF537 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet Media Access Controller (MAC) that supports both 10-BaseT (10 Mbps) and 100-BaseT (100 Mbps) operation. The 10/100 Ethernet MAC peripheral is fully compliant to the IEEE 802.3-2002 standard, and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are

- Support of MII and RMII protocols for external PHYs.
- Full duplex and half duplex modes.
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS.
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing.
- Flow control (in full-duplex operation): generation and detection of PAUSE frames.
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers.
- SCLK operating range down to 25 MHz (active and sleep operating modes).
- Internal loopback from Tx to Rx.

Some advanced features are

- Buffered crystal output to external PHY for support of a single crystal system.
- Automatic checksum computation of IP header and IP payload fields of Rx frames.
- Independent 32-bit descriptor-driven Rx and Tx DMA channels.
- Frame status delivery to memory via DMA, including frame completion semaphores, for efficient buffer queue management in software.
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations.
- Convenient frame alignment modes support even 32-bit alignment of encapsulated Rx or Tx IP packet data in memory after the 14-byte MAC header.
- Programmable Ethernet event interrupt supports any combination of
  - Any selected Rx or Tx frame status conditions.
  - PHY interrupt condition.
  - Wake-up frame detected.
  - Any selected MAC management counter(s) at half-full.
  - DMA descriptor error.
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value.

(VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO:SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0110	6:1	300	50
1010	10:1	500	50

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO:CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Ordering Guide on Page 67), it also depends on the applied V_{DDINT} voltage (see Table 10, Table 11, and Table 12 on Page 24 for details). The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDEXT} voltage (see Table 14 on Page 24).

BOOTING MODES

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processor has six mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. A seventh mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE2–0	Description
000	Execute from 16-bit external memory (bypass boot ROM)
001	Boot from 8-bit or 16-bit memory (EPROM/flash)
010	Reserved
011	Boot from serial SPI memory (EEPROM/flash)
100	Boot from SPI host (slave mode)
101	Boot from serial TWI memory (EEPROM/flash)
110	Boot from TWI host (slave mode)
111	Boot from UART host (slave mode)

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit and 16-bit external flash memory – The 8-bit or 16-bit flash boot routine located in Boot ROM memory space is set up using asynchronous memory bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup). The Boot ROM evaluates the first byte of the boot stream at address 0x2000 0000. If it is 0x40, 8-bit boot is performed. A 0x60 byte assumes a 16-bit memory device and performs 8-bit DMA. A 0x20 byte also assumes 16-bit memory but performs 16-bit DMA.
- Boot from serial SPI memory (EEPROM or flash) – 8-, 16-, or 24-bit addressable devices are supported as well as AT45DB041, AT45DB081, AT45DB161, AT45DB321, AT45DB642, and AT45DB1282 DataFlash® devices from Atmel. The SPI uses the PF10/SPI SSEL1 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit, or Atmel addressable device is detected, and begins clocking data into the processor.
- Boot from SPI host device – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the .LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any more bytes until the flag is deasserted. The flag is chosen by the user and this information is transferred to the Blackfin processor via bits 10:5 of the FLAG header.
- Boot from UART – Using an autobaud handshake sequence, a boot-stream-formatted program is downloaded by the host. The host agent selects a baud rate within the UART's clocking capabilities. When performing the autobaud, the UART expects an "@" (boot stream) character (8 bits data, 1 start bit, 1 stop bit, no parity bit) on the RXD pin to determine the bit rate. It then replies with an acknowledgement that is composed of 4 bytes: 0xBF, the value of UART_DLL, the value of UART_DLH, and 0x00. The host can then download the boot stream. When the processor needs to hold off the host, it deasserts CTS. Therefore, the host must monitor this signal.

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/UART1–0/Timer7–0/SPI/ External DMA Request/PPI (= High Source/High Sink Pin)*			
PF0* – GPIO/*UART0 TX/DMAR0*	I/O	GPIO/*UART0 Transmit/DMA Request 0*	C
PF1* – GPIO/*UART0 RX/DMAR1/TACI1*	I/O	GPIO/*UART0 Receive/DMA Request 1/Timer1 Alternate Input Capture*	C
PF2* – GPIO/*UART1 TX/TMR7*	I/O	GPIO/*UART1 Transmit/Timer7*	C
PF3* – GPIO/*UART1 RX/TMR6/TACI6*	I/O	GPIO/*UART1 Receive/Timer6/Timer6 Alternate Input Capture*	C
PF4* – GPIO/*TMR5/SPI SSEL6*	I/O	GPIO/*Timer5/SPI Slave Select Enable 6*	C
PF5* – GPIO/*TMR4/SPI SSEL5*	I/O	GPIO/*Timer4/SPI Slave Select Enable 5*	C
PF6* – GPIO/*TMR3/SPI SSEL4*	I/O	GPIO/*Timer3/SPI Slave Select Enable 4*	C
PF7* – GPIO/*TMR2/PPI FS3*	I/O	GPIO/*Timer2/PPI Frame Sync 3*	C
PF8 – GPIO/*TMR1/PPI FS2*	I/O	GPIO/*Timer1/PPI Frame Sync 2*	C
PF9 – GPIO/*TMR0/PPI FS1*	I/O	GPIO/*Timer0/PPI Frame Sync 1*	C
PF10 – GPIO/*SPI SSEL1*	I/O	GPIO/*SPI Slave Select Enable 1*	C
PF11 – GPIO/*SPI MOSI*	I/O	GPIO/*SPI Master Out Slave In*	C
PF12 – GPIO/*SPI MISO*	I/O	GPIO/*SPI Master In Slave Out* (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
PF13 – GPIO/*SPI SCK*	I/O	GPIO/*SPI Clock*	D
PF14 – GPIO/*SPI SS/TACLK0*	I/O	GPIO/*SPI Slave Select/Alternate Timer0 Clock Input*	C
PF15 – GPIO/*PPI CLK/TMRCLK*	I/O	GPIO/*PPI Clock/External Timer Reference*	C
Port G: GPIO/PPI/SPORT1			
PG0 – GPIO/*PPI D0*	I/O	GPIO/*PPI Data 0*	C
PG1 – GPIO/*PPI D1*	I/O	GPIO/*PPI Data 1*	C
PG2 – GPIO/*PPI D2*	I/O	GPIO/*PPI Data 2*	C
PG3 – GPIO/*PPI D3*	I/O	GPIO/*PPI Data 3*	C
PG4 – GPIO/*PPI D4*	I/O	GPIO/*PPI Data 4*	C
PG5 – GPIO/*PPI D5*	I/O	GPIO/*PPI Data 5*	C
PG6 – GPIO/*PPI D6*	I/O	GPIO/*PPI Data 6*	C
PG7 – GPIO/*PPI D7*	I/O	GPIO/*PPI Data 7*	C
PG8 – GPIO/*PPI D8/DR1SEC*	I/O	GPIO/*PPI Data 8/SPORT1 Receive Data Secondary*	C
PG9 – GPIO/*PPI D9/DT1SEC*	I/O	GPIO/*PPI Data 9/SPORT1 Transmit Data Secondary*	C
PG10 – GPIO/*PPI D10/RSCLK1*	I/O	GPIO/*PPI Data 10/SPORT1 Receive Serial Clock*	D
PG11 – GPIO/*PPI D11/RFS1*	I/O	GPIO/*PPI Data 11/SPORT1 Receive Frame Sync*	C
PG12 – GPIO/*PPI D12/DR1PRI*	I/O	GPIO/*PPI Data 12/SPORT1 Receive Data Primary*	C
PG13 – GPIO/*PPI D13/TSCLK1*	I/O	GPIO/*PPI Data 13/SPORT1 Transmit Serial Clock*	D
PG14 – GPIO/*PPI D14/TFS1*	I/O	GPIO/*PPI Data 14/SPORT1 Transmit Frame Sync*	C
PG15 – GPIO/*PPI D15/DT1PRI*	I/O	GPIO/*PPI Data 15/SPORT1 Transmit Data Primary*	C

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port H: GPIO/10/100 Ethernet MAC (On ADSP-BF534, these pins are GPIO only)			
PH0 – GPIO/*ETxD0*	I/O	GPIO/*Ethernet MII or RMII Transmit D0*	E
PH1 – GPIO/*ETxD1*	I/O	GPIO/*Ethernet MII or RMII Transmit D1*	E
PH2 – GPIO/*ETxD2*	I/O	GPIO/*Ethernet MII Transmit D2*	E
PH3 – GPIO/*ETxD3*	I/O	GPIO/*Ethernet MII Transmit D3*	E
PH4 – GPIO/*ETxEN*	I/O	GPIO/*Ethernet MII or RMII Transmit Enable*	E
PH5 – GPIO/*MII TxCLK/RMII REF_CLK*	I/O	GPIO/*Ethernet MII Transmit Clock/RMII Reference Clock*	E
PH6 – GPIO/*MII* $\overline{PHYINT}$/*RMII* $\overline{MDINT}$	I/O	GPIO/*Ethernet MII PHY Interrupt/RMII Management Data Interrupt* (This pin should be pulled high when used as a hibernate wake-up.)	E
PH7 – GPIO/*COL*	I/O	GPIO/*Ethernet Collision*	E
PH8 – GPIO/*ERxD0*	I/O	GPIO/*Ethernet MII or RMII Receive D0*	E
PH9 – GPIO/*ERxD1*	I/O	GPIO/*Ethernet MII or RMII Receive D1*	E
PH10 – GPIO/*ERxD2*	I/O	GPIO/*Ethernet MII Receive D2*	E
PH11 – GPIO/*ERxD3*	I/O	GPIO/*Ethernet MII Receive D3*	E
PH12 – GPIO/*ERxDV/TACLK5*	I/O	GPIO/*Ethernet MII Receive Data Valid/Alternate Timer5 Input Clock*	E
PH13 – GPIO/*ERxCLK/TACLK6*	I/O	GPIO/*Ethernet MII Receive Clock/Alternate Timer6 Input Clock*	E
PH14 – GPIO/*ERxER/TACLK7*	I/O	GPIO/*Ethernet MII or RMII Receive Error/Alternate Timer7 Input Clock*	E
PH15 – GPIO/*MII CRS/RMII CRS_DV*	I/O	GPIO/*Ethernet MII Carrier Sense/Ethernet RMII Carrier Sense and Receive Data Valid*	E
Port J: SPORT0/TWI/SPI Select/CAN			
PJ0 – MDC	O	Ethernet Management Channel Clock (On ADSP-BF534 processors, do not connect this pin.)	E
PJ1 – MDIO	I/O	Ethernet Management Channel Serial Data (On ADSP-BF534 processors, tie this pin to ground.)	E
PJ2 – SCL	I/O	TWI Serial Clock (This pin is an open-drain output and requires a pull-up resistor.)	F
PJ3 – SDA	I/O	TWI Serial Data (This pin is an open-drain output and requires a pull-up resistor.)	F
PJ4 – DR0SEC/*CANRX/TACI0*	I	SPORT0 Receive Data Secondary/*CAN Receive/Timer0 Alternate Input Capture*	
PJ5 – DT0SEC/*CANTX/SPI SSEL7*	O	SPORT0 Transmit Data Secondary/*CAN Transmit/SPI Slave Select Enable 7*	C
PJ6 – RSCLK0/*TACLK2*	I/O	SPORT0 Receive Serial Clock/*Alternate Timer2 Clock Input*	D
PJ7 – RFS0/*TACLK3*	I/O	SPORT0 Receive Frame Sync/*Alternate Timer3 Clock Input*	C
PJ8 – DR0PRI/*TACLK4*	I	SPORT0 Receive Data Primary/*Alternate Timer4 Clock Input*	
PJ9 – TSCLK0/*TACLK1*	I/O	SPORT0 Transmit Serial Clock/*Alternate Timer1 Clock Input*	D
PJ10 – TFS0/*SPI SSEL3*	I/O	SPORT0 Transmit Frame Sync/*SPI Slave Select Enable 3*	C
PJ11 – DT0PRI/*SPI SSEL2*	O	SPORT0 Transmit Data Primary/*SPI Slave Select Enable 2*	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{TRST}$	I	JTAG Reset (This pin should be pulled low if the JTAG port is not used.)	
$\overline{EMU}$	O	Emulation Output	C

Table 17. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.33
$I_{DD-HIGH}$	1.29
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.43

[1] See EE-297 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 18. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})													
Frequency (MHz)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
50	11.0	13.7	19.13	18.2	18.67	19.13	19.6	21.2	24.1	25.5	28.5	28.6	28.85	29.2
100	27.9	22.7	30.8	28.4	29.3	30.8	32.9	35.3	37.8	40.6	43.5	43.7	44.1	45.8
200	36.9	42.6	55.0	49.2	51.5	55.0	58.3	62.9	67.0	69.7	73.0	74.0	75.7	80.7
300	N/A	61.5	79.2	70.4	74.6	79.2	84.4	90.7	94.3	99.1	103.9	105.5	108.0	113.4
400	N/A	N/A	N/A	92.4	97.2	104.3	109.8	116.5	121.9	128.0	134.6	136.6	139.8	145.1
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	142.3	149.3	157.5	164.7	166.7	169.8	176.9
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	158.6	167.0	174.3	176.6	180.1	187.9
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	193.7	196.5	200.7	210.0

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

Table 32. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2]		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only. TSCLKx is tied to RSCLKx.

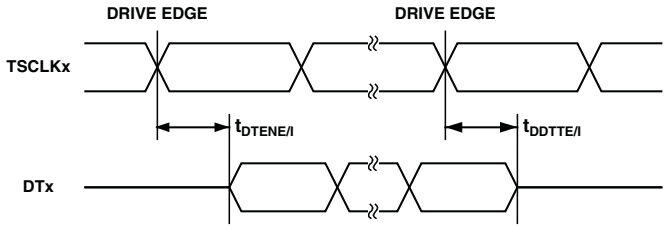


Figure 22. Enable and Three-State

Serial Peripheral Interface Port—Slave Timing

Table 35 and Figure 25 describe SPI port slave operations.

Table 35. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		ns

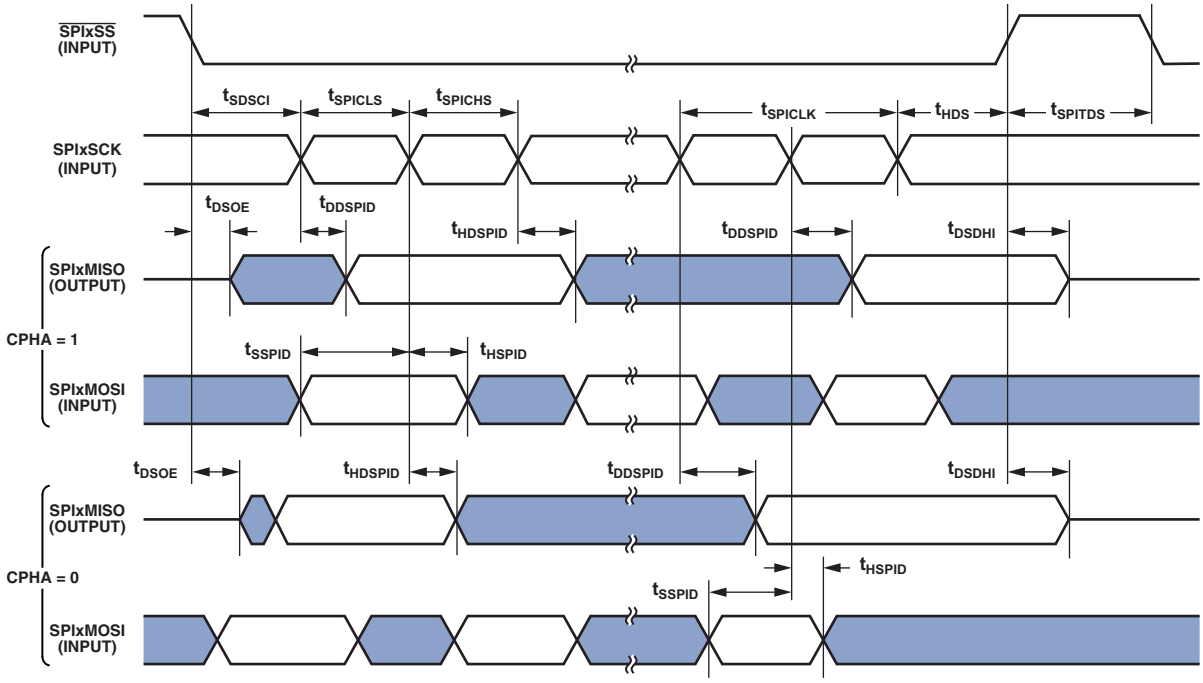


Figure 25. Serial Peripheral Interface (SPI) Port—Slave Timing

General-Purpose Port Timing

Table 36 and Figure 26 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	0	6	ns

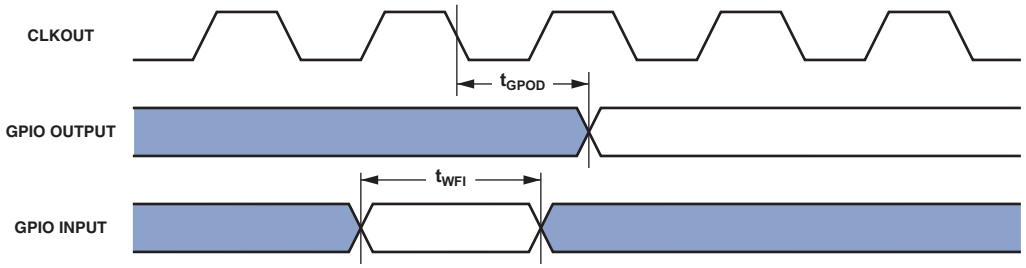


Figure 26. General-Purpose Port Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF537 Blackfin Processor Hardware Reference*.

JTAG Test and Emulation Port Timing

Table 39 and Figure 29 describe JTAG port operations.

Table 39. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay From TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA15–0, $\overline{\text{BR}}$, ARDY, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH15–0, MDIO, TCK, $\overline{\text{TRST}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, RTXI, BMODE2–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{\text{ABE1–0}}$, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, SCL, SDA, MDC, MDIO, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH15–0, RTXO, TDO, $\overline{\text{EMU}}$, XTAL, VROUT1–0.

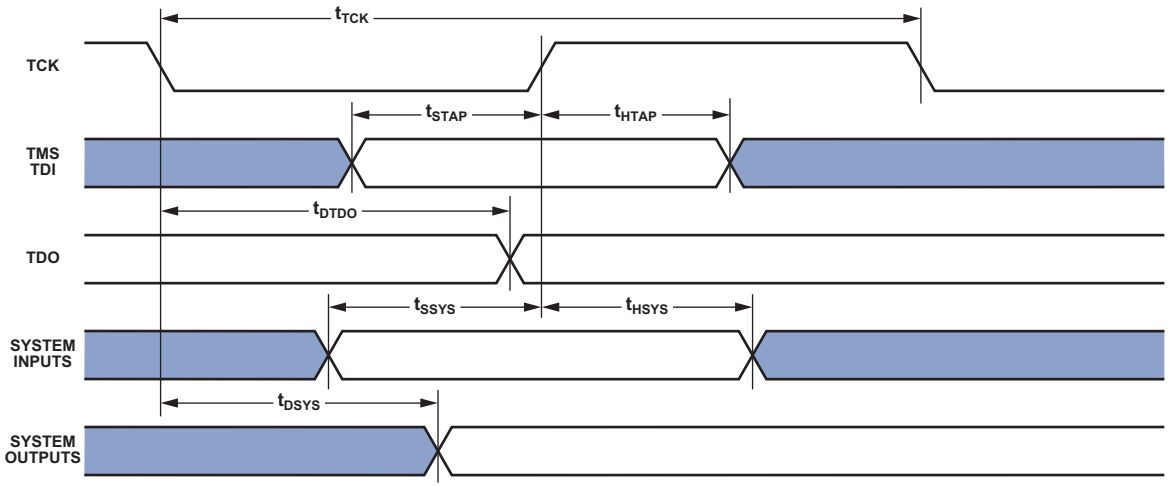


Figure 29. JTAG Port Timing

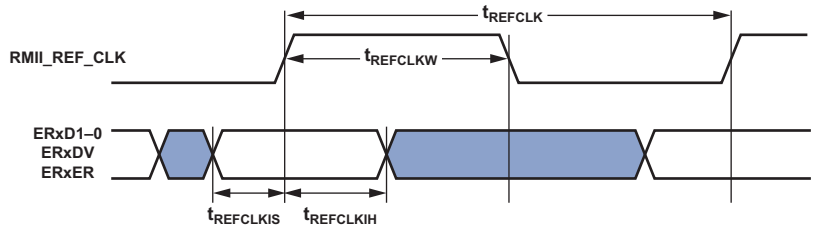


Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

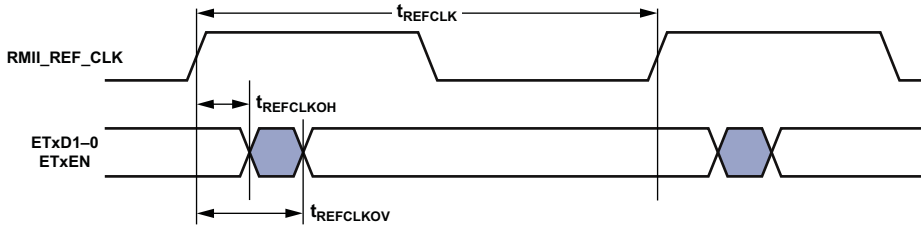


Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

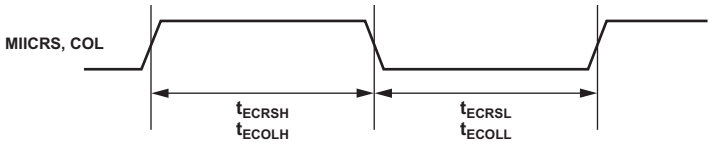


Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

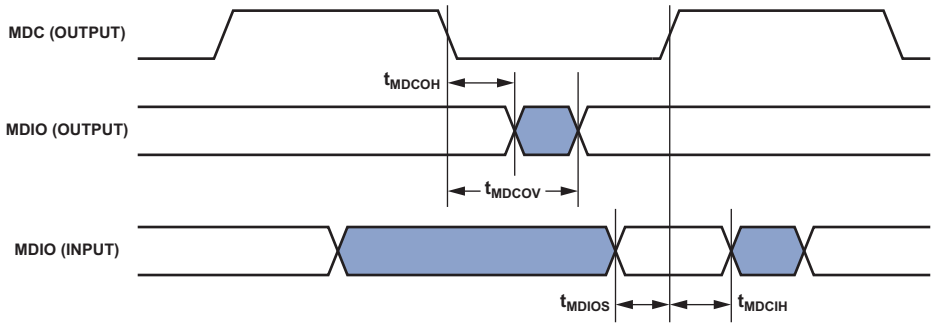


Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management

OUTPUT DRIVE CURRENTS

Figure 36 through Figure 47 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage. See Table 9 on Page 19 for information about which driver type corresponds to a particular pin.

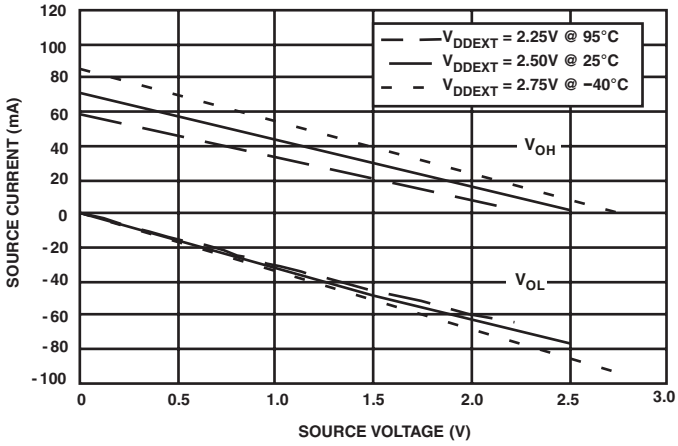


Figure 36. Drive Current A (Low V_{DDEXT})

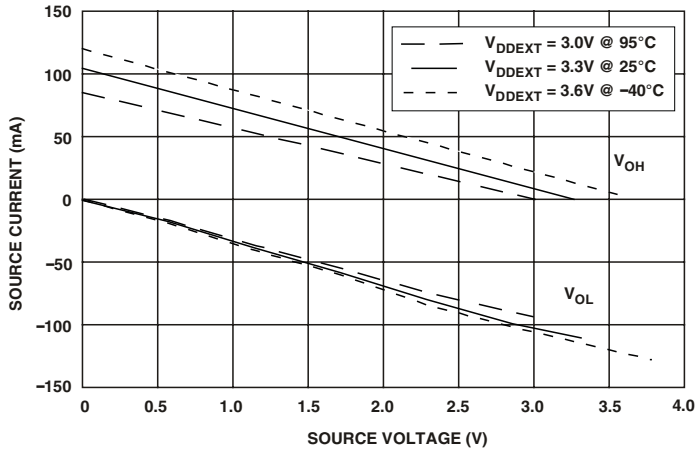


Figure 37. Drive Current A (High V_{DDEXT})

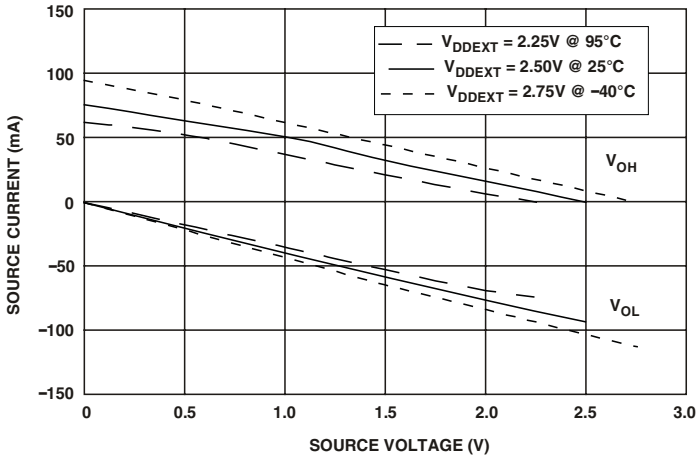


Figure 38. Drive Current B (Low V_{DDEXT})

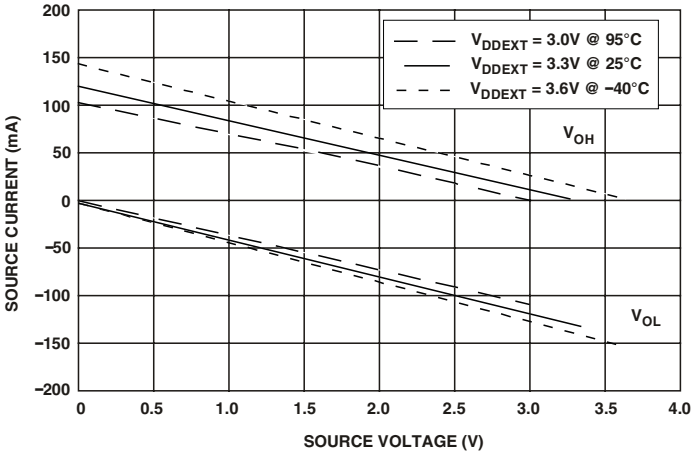


Figure 39. Drive Current B (High V_{DDEXT})

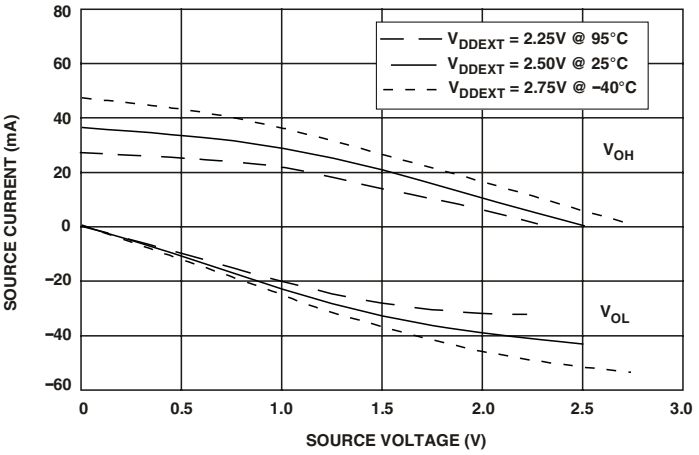


Figure 40. Drive Current C (Low V_{DDEXT})

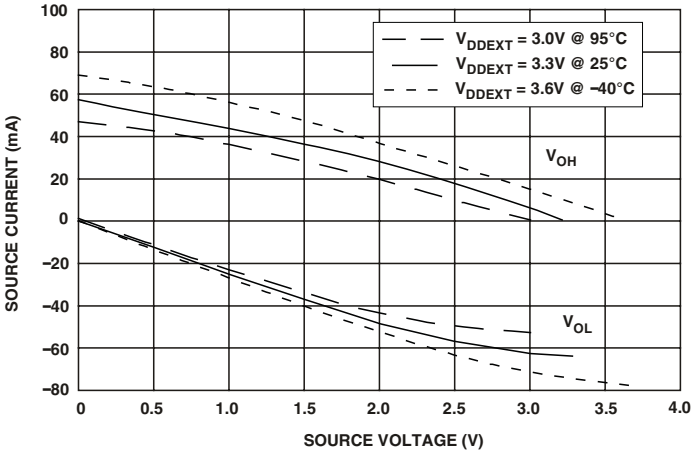


Figure 41. Drive Current C (High V_{DDEXT})

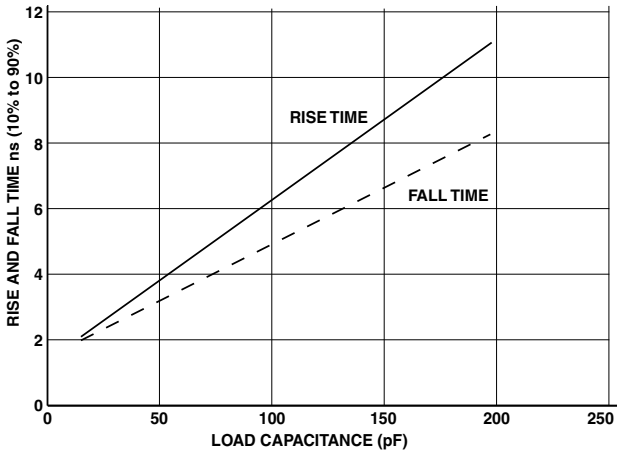


Figure 53. Typical Output Delay or Hold for Driver B at V_{DDEXT} Min

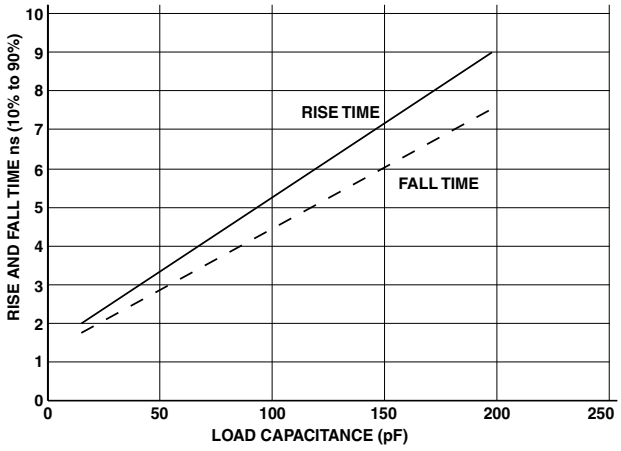


Figure 54. Typical Output Delay or Hold for Driver B at V_{DDEXT} Max

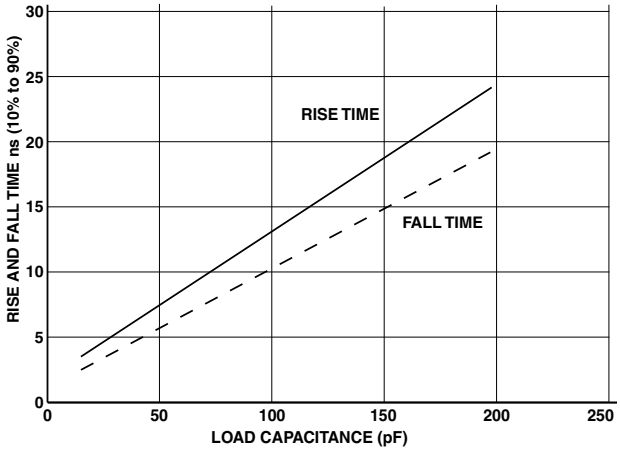


Figure 55. Typical Output Delay or Hold for Driver C at V_{DDEXT} Min

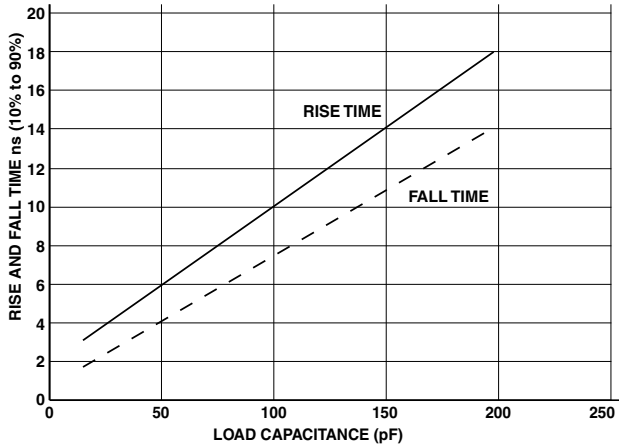


Figure 56. Typical Output Delay or Hold for Driver C at V_{DDEXT} Max

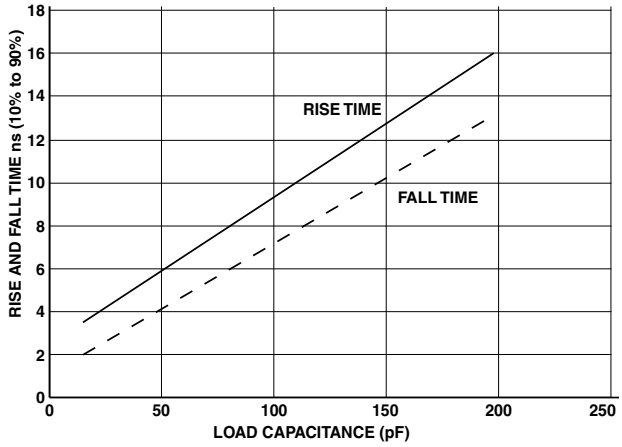


Figure 57. Typical Output Delay or Hold for Driver D at V_{DDEXT} Min

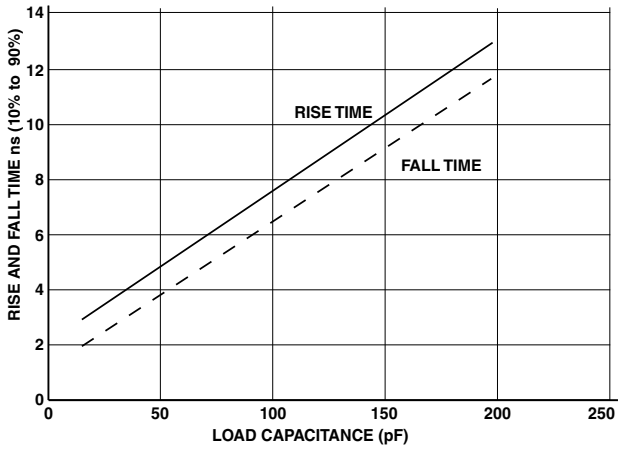


Figure 58. Typical Output Delay or Hold for Driver D at V_{DDEXT} Max

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 46

P_D = Power dissipation (see the power dissipation discussion and the tables on Page 27 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 46 through Table 48, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA). The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Industrial applications using the 208-ball BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Table 46. Thermal Characteristics (182-Ball BGA)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	32.80	°C/W
θ_{JMA}	1 Linear m/s Airflow	29.30	°C/W
θ_{JMA}	2 Linear m/s Airflow	28.00	°C/W
θ_{JB}		20.10	°C/W
θ_{JC}		7.92	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.19	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

Table 47. Thermal Characteristics (208-Ball BGA without Thermal Vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	23.30	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.20	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.20	°C/W
θ_{JB}		13.05	°C/W
θ_{JC}		6.92	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.27	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.32	°C/W

Table 48. Thermal Characteristics (208-Ball BGA with Thermal Vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.60	°C/W
θ_{JMA}	1 Linear m/s Airflow	19.40	°C/W
θ_{JMA}	2 Linear m/s Airflow	18.40	°C/W
θ_{JB}		13.20	°C/W
θ_{JC}		6.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.16	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.27	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.32	°C/W

182-BALL CSP_BGA BALL ASSIGNMENT

Table 49 lists the CSP_BGA ball assignment by signal mnemonic. Table 50 on Page 58 lists the CSP_BGA ball assignment by ball number.

Table 49. 182-Ball CSP_BGA Ball Assignment (Alphabetically by Signal Mnemonic)

Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.
$\overline{ABE0}$	H13	CLKOUT	B14	GND	L6	PG8	E3	$\overline{SRAS}$	D13
$\overline{ABE1}$	H12	DATA0	M9	GND	L8	PG9	E4	$\overline{SWE}$	D12
ADDR1	J14	DATA1	N9	GND	L10	PH0	C2	TCK	P2
ADDR10	M13	DATA10	N6	GND	M4	PH1	C3	TDI	M3
ADDR11	M14	DATA11	P6	GND	M10	PH10	B6	TDO	N3
ADDR12	N14	DATA12	M5	GND	P14	PH11	A2	TMS	N2
ADDR13	N13	DATA13	N5	$\overline{NMI}$	B10	PH12	A3	$\overline{TRST}$	N1
ADDR14	N12	DATA14	P5	PF0	M1	PH13	A4	V_{DDEXT}	A1
ADDR15	M11	DATA15	P4	PF1	L1	PH14	A5	V_{DDEXT}	C12
ADDR16	N11	DATA2	P9	PF10	J2	PH15	A6	V_{DDEXT}	E6
ADDR17	P13	DATA3	M8	PF11	J3	PH2	C4	V_{DDEXT}	E11
ADDR18	P12	DATA4	N8	PF12	H1	PH3	C5	V_{DDEXT}	F4
ADDR19	P11	DATA5	P8	PF13	H2	PH4	C6	V_{DDEXT}	F12
ADDR2	K14	DATA6	M7	PF14	H3	PH5	B1	V_{DDEXT}	H5
ADDR3	L14	DATA7	N7	PF15	H4	PH6	B2	V_{DDEXT}	H10
ADDR4	J13	DATA8	P7	PF2	L2	PH7	B3	V_{DDEXT}	J11
ADDR5	K13	DATA9	M6	PF3	L3	PH8	B4	V_{DDEXT}	J12
ADDR6	L13	$\overline{EMU}$	M2	PF4	L4	PH9	B5	V_{DDEXT}	K7
ADDR7	K12	GND	A10	PF5	K1	PJ0	C7	V_{DDEXT}	K9
ADDR8	L12	GND	A14	PF6	K2	PJ1	B7	V_{DDEXT}	L7
ADDR9	M12	GND	D4	PF7	K3	PJ10	D10	V_{DDEXT}	L9
$\overline{AMS0}$	E14	GND	E7	PF8	K4	PJ11	D11	V_{DDEXT}	L11
$\overline{AMS1}$	F14	GND	E9	PF9	J1	PJ2	B11	V_{DDEXT}	P1
$\overline{AMS2}$	F13	GND	F5	PG0	G1	PJ3	C11	V_{DDINT}	E5
$\overline{AMS3}$	G12	GND	F6	PG1	G2	PJ4	D7	V_{DDINT}	E8
$\overline{AOE}$	G13	GND	F10	PG10	D1	PJ5	D8	V_{DDINT}	E10
ARDY	E13	GND	F11	PG11	D2	PJ6	C8	V_{DDINT}	G10
$\overline{ARE}$	G14	GND	G4	PG12	D3	PJ7	B8	V_{DDINT}	K5
$\overline{AWE}$	H14	GND	G5	PG13	D5	PJ8	D9	V_{DDINT}	K8
$\overline{BG}$	P10	GND	G11	PG14	D6	PJ9	C9	V_{DDINT}	K10
$\overline{BGH}$	N10	GND	H11	PG15	C1	$\overline{RESET}$	C10	V_{DDRTC}	B9
BMODE0	N4	GND	J4	PG2	G3	RTXO	A8	VROUT0	A13
BMODE1	P3	GND	J5	PG3	F1	RTXI	A9	VROUT1	B12
BMODE2	L5	GND	J9	PG4	F2	SA10	E12	XTAL	A11
$\overline{BR}$	D14	GND	J10	PG5	F3	$\overline{SCAS}$	C14		
CLKBUF	A7	GND	K6	PG6	E1	SCKE	B13		
CLKIN	A12	GND	K11	PG7	E2	$\overline{SMS}$	C13		

OUTLINE DIMENSIONS

Dimensions in Figure 67 and Figure 68 are shown in millimeters.

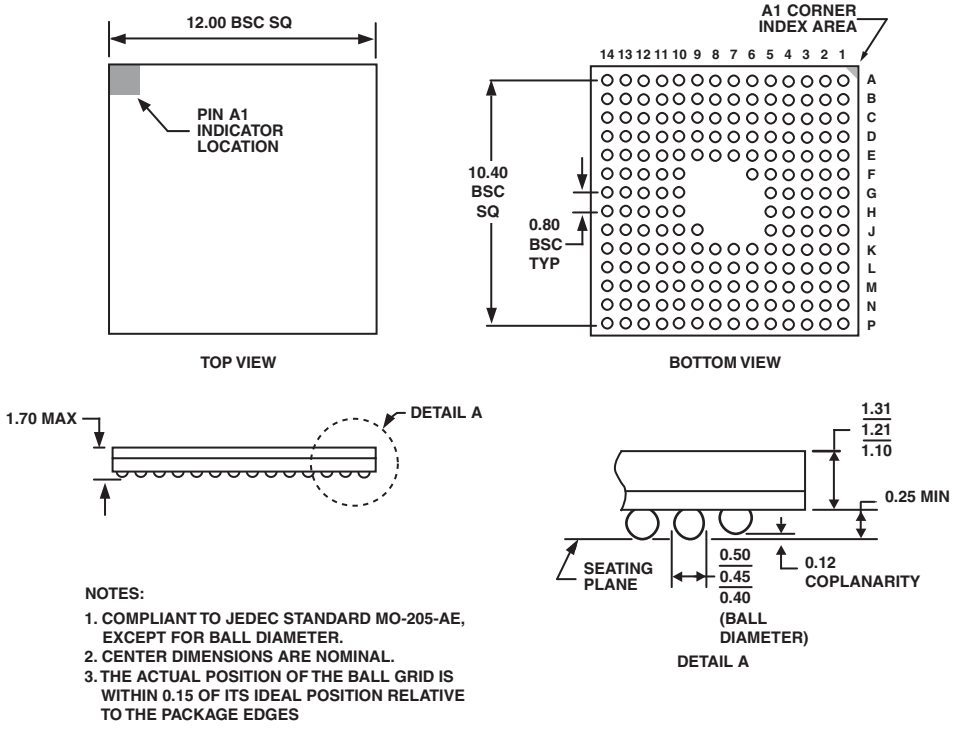


Figure 67. 182-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-182)
Dimensions shown in millimeters

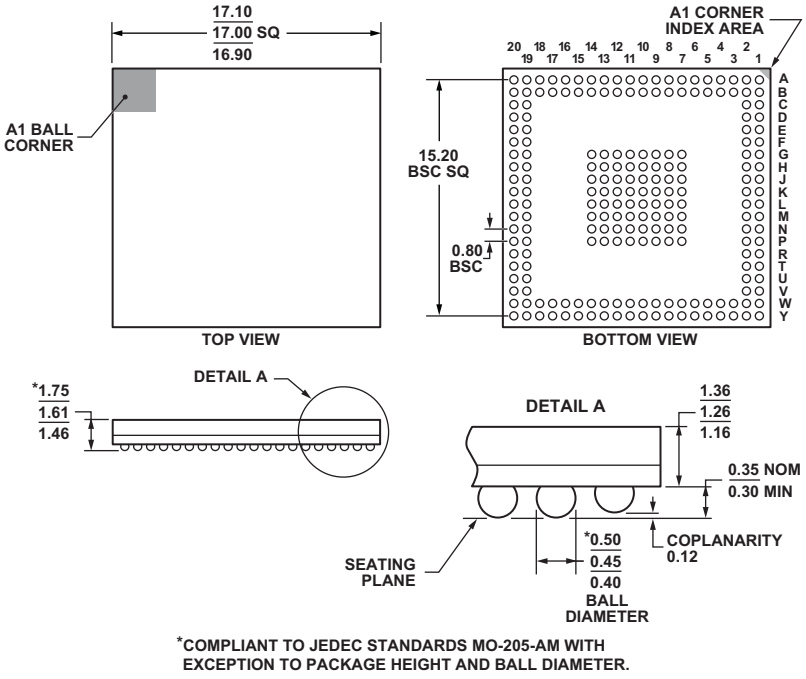


Figure 68. 208-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-208-2)
Dimensions shown in millimeters

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In the following table CSP_BGA = Chip Scale Package Ball Grid Array.

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF534BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534YBCZ-4B	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBC-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3B	–40°C to +85°C	300 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBCZ3BRL	–40°C to +85°C	300 MHz	208-Ball CSP_BGA, 13" Tape and Reel	BC-208-2
ADSP-BF536BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBCZ-5AV	–40°C to +85°C	533 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5BV	–40°C to +85°C	533 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537KBCZ-6AV	0°C to +70°C	600 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537KBCZ-6BV	0°C to +70°C	600 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 23 for junction temperature (T_J) specification which is the only temperature specification.