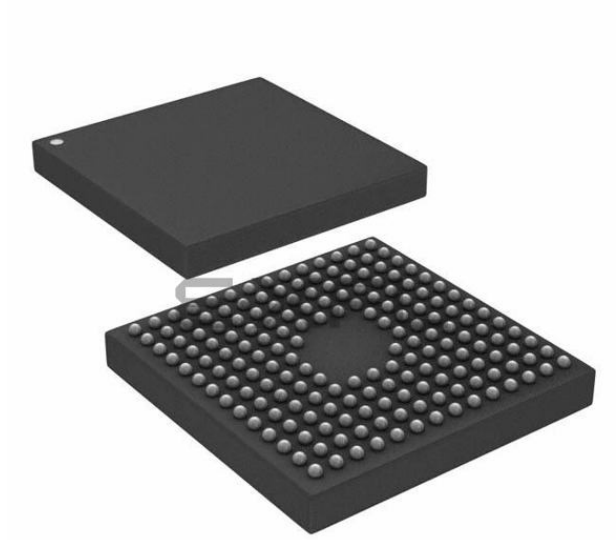

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.26V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	182-LFBGA, CSPBGA
Supplier Device Package	182-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf534bbc-5a

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates, and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

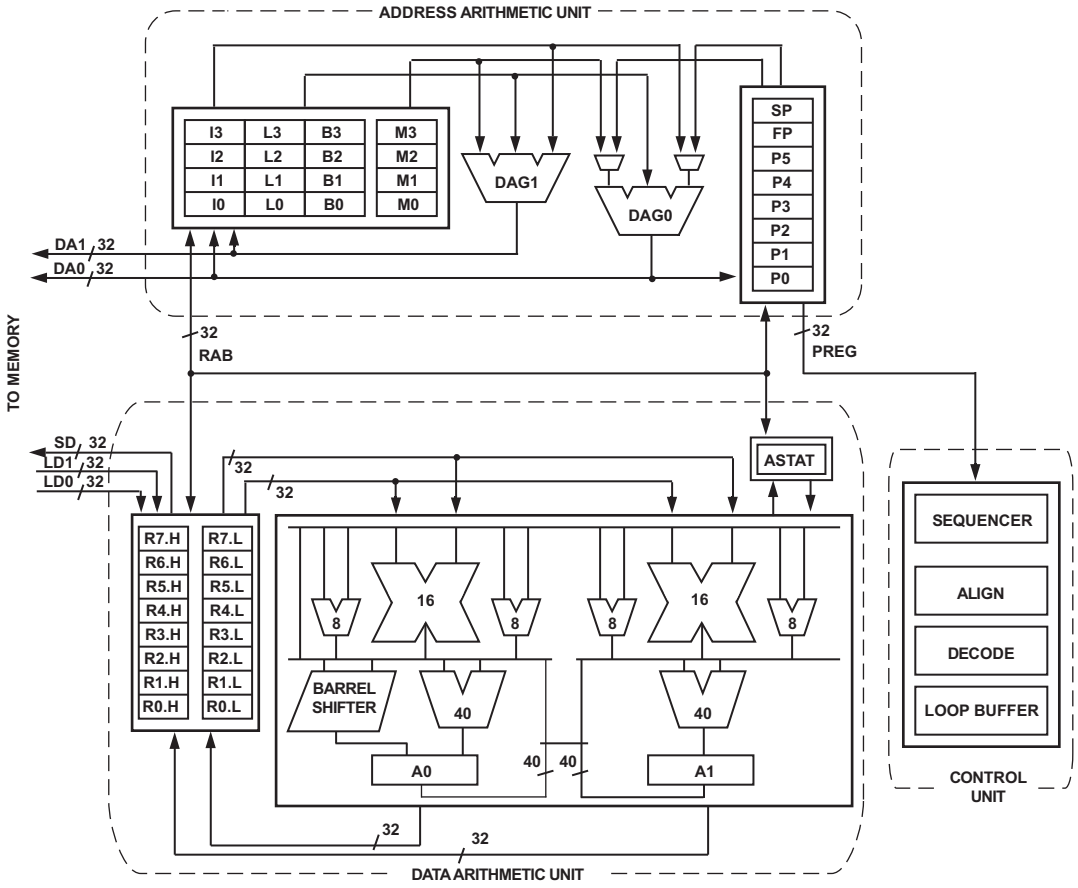


Figure 2. Blackfin Processor Core

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

MEMORY ARCHITECTURE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost, and performance off-chip memory systems. (See Figure 3).

The on-chip L1 memory system is the highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 516M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have three blocks of on-chip memory providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 64K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM, and cannot be configured as cache memory.

External (Off-Chip) Memory

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank, and the SDRAM controller supports up to 4 internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

I/O Memory Space

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The Blackfin processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the Blackfin processor is configured to boot from boot ROM

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the Blackfin processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 Is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (IAR). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
PLL Wakeup	IVG7	0
DMA Error (Generic)	IVG7	1
DMAR0 Block Interrupt	IVG7	1
DMAR1 Block Interrupt	IVG7	1
DMAR0 Overflow Error	IVG7	1
DMAR1 Overflow Error	IVG7	1
CAN Error	IVG7	2
Ethernet Error (ADSP-BF536 and ADSP-BF537 only)	IVG7	2
SPORT 0 Error	IVG7	2
SPORT 1 Error	IVG7	2
PPI Error	IVG7	2
SPI Error	IVG7	2
UART0 Error	IVG7	2
UART1 Error	IVG7	2
Real-Time Clock	IVG8	3
DMA Channel 0 (PPI)	IVG8	4
DMA Channel 3 (SPORT 0 Rx)	IVG9	5
DMA Channel 4 (SPORT 0 Tx)	IVG9	6
DMA Channel 5 (SPORT 1 Rx)	IVG9	7
DMA Channel 6 (SPORT 1 Tx)	IVG9	8
TWI	IVG10	9
DMA Channel 7 (SPI)	IVG10	10
DMA Channel 8 (UART0 Rx)	IVG10	11
DMA Channel 9 (UART0 Tx)	IVG10	12
DMA Channel 10 (UART1 Rx)	IVG10	13
DMA Channel 11 (UART1 Tx)	IVG10	14
CAN Rx	IVG11	15
CAN Tx	IVG11	16
DMA Channel 1 (Ethernet Rx, ADSP-BF536 and ADSP-BF537 only)	IVG11	17
Port H Interrupt A	IVG11	17
DMA Channel 2 (Ethernet Tx, ADSP-BF536 and ADSP-BF537 only)	IVG11	18
Port H Interrupt B	IVG11	18
Timer 0	IVG12	19
Timer 1	IVG12	20
Timer 2	IVG12	21
Timer 3	IVG12	22
Timer 4	IVG12	23
Timer 5	IVG12	24
Timer 6	IVG12	25
Timer 7	IVG12	26
Port F, G Interrupt A	IVG12	27
Port G Interrupt B	IVG12	28

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

CONTROLLER AREA NETWORK (CAN)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors offer a CAN controller that is a communication controller implementing the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well-suited for control applications due to its capability to communicate reliably over a network, since the protocol incorporates CRC checking message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (eight receive only, eight transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wake-up from hibernation mode (lowest static power consumption mode).
- Interrupts, including: Tx complete, Rx complete, error, global.

The electrical characteristics of each network connection are very demanding so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high-speed, fault-tolerant, single-wire transceivers.

TWI CONTROLLER INTERFACE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

10/100 ETHERNET MAC

The ADSP-BF536 and ADSP-BF537 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet Media Access Controller (MAC) that supports both 10-BaseT (10 Mbps) and 100-BaseT (100 Mbps) operation. The 10/100 Ethernet MAC peripheral is fully compliant to the IEEE 802.3-2002 standard, and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are

- Support of MII and RMII protocols for external PHYs.
- Full duplex and half duplex modes.
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS.
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing.
- Flow control (in full-duplex operation): generation and detection of PAUSE frames.
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers.
- SCLK operating range down to 25 MHz (active and sleep operating modes).
- Internal loopback from Tx to Rx.

Some advanced features are

- Buffered crystal output to external PHY for support of a single crystal system.
- Automatic checksum computation of IP header and IP payload fields of Rx frames.
- Independent 32-bit descriptor-driven Rx and Tx DMA channels.
- Frame status delivery to memory via DMA, including frame completion semaphores, for efficient buffer queue management in software.
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations.
- Convenient frame alignment modes support even 32-bit alignment of encapsulated Rx or Tx IP packet data in memory after the 14-byte MAC header.
- Programmable Ethernet event interrupt supports any combination of
  - Any selected Rx or Tx frame status conditions.
  - PHY interrupt condition.
  - Wake-up frame detected.
  - Any selected MAC management counter(s) at half-full.
  - DMA descriptor error.
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value.

(VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios.

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO:SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0001	1:1	100	100
0110	6:1	300	50
1010	10:1	500	50

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be changed dynamically without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV).

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. This programmable core clock capability is useful for fast core frequency modifications.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO:CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

The maximum CCLK frequency not only depends on the part's speed grade (see Ordering Guide on Page 67), it also depends on the applied V_{DDINT} voltage (see Table 10, Table 11, and Table 12 on Page 24 for details). The maximal system clock rate (SCLK) depends on the chip package and the applied V_{DDEXT} voltage (see Table 14 on Page 24).

BOOTING MODES

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processor has six mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. A seventh mode is provided to execute from external memory, bypassing the boot sequence.

Table 8. Booting Modes

BMODE2–0	Description
000	Execute from 16-bit external memory (bypass boot ROM)
001	Boot from 8-bit or 16-bit memory (EPROM/flash)
010	Reserved
011	Boot from serial SPI memory (EEPROM/flash)
100	Boot from SPI host (slave mode)
101	Boot from serial TWI memory (EEPROM/flash)
110	Boot from TWI host (slave mode)
111	Boot from UART host (slave mode)

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Execute from 16-bit external memory – Execution starts from address 0x2000 0000 with 16-bit packing. The boot ROM is bypassed in this mode. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).
- Boot from 8-bit and 16-bit external flash memory – The 8-bit or 16-bit flash boot routine located in Boot ROM memory space is set up using asynchronous memory bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup). The Boot ROM evaluates the first byte of the boot stream at address 0x2000 0000. If it is 0x40, 8-bit boot is performed. A 0x60 byte assumes a 16-bit memory device and performs 8-bit DMA. A 0x20 byte also assumes 16-bit memory but performs 16-bit DMA.
- Boot from serial SPI memory (EEPROM or flash) – 8-, 16-, or 24-bit addressable devices are supported as well as AT45DB041, AT45DB081, AT45DB161, AT45DB321, AT45DB642, and AT45DB1282 DataFlash® devices from Atmel. The SPI uses the PF10/SPI SSEL1 output pin to select a single SPI EEPROM/flash device, submits a read command and successive address bytes (0x00) until a valid 8-, 16-, or 24-bit, or Atmel addressable device is detected, and begins clocking data into the processor.
- Boot from SPI host device – The Blackfin processor operates in SPI slave mode and is configured to receive the bytes of the .LDR file from an SPI host (master) agent. To hold off the host device from transmitting while the boot ROM is busy, the Blackfin processor asserts a GPIO pin, called host wait (HWAIT), to signal the host device not to send any more bytes until the flag is deasserted. The flag is chosen by the user and this information is transferred to the Blackfin processor via bits 10:5 of the FLAG header.
- Boot from UART – Using an autobaud handshake sequence, a boot-stream-formatted program is downloaded by the host. The host agent selects a baud rate within the UART's clocking capabilities. When performing the autobaud, the UART expects an "@" (boot stream) character (8 bits data, 1 start bit, 1 stop bit, no parity bit) on the RXD pin to determine the bit rate. It then replies with an acknowledgement that is composed of 4 bytes: 0xBF, the value of UART_DLL, the value of UART_DLH, and 0x00. The host can then download the boot stream. When the processor needs to hold off the host, it deasserts CTS. Therefore, the host must monitor this signal.

suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF534/ADSP-BF536/ADSP-BF537 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started with Blackfin Processors*
- *ADSP-BF537 Blackfin Processor Hardware Reference*
- *ADSP-BF53x/ADSP-BF56x Blackfin Processor Programming Reference*
- *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 10 through Table 12 describe the voltage/frequency requirements for the ADSP-BF534/ADSP-BF536/ADSP-BF537 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 13 describes phase-locked loop operating conditions.

Table 10. Core Clock Requirements—500 MHz, 533 MHz, and 600 MHz Speed Grades[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.30 V Minimum)[2]	1.30 V	600	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.20 V Minimum)[3]	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] See Ordering Guide on Page 67.
[2] Applies to 600 MHz models only. See Ordering Guide on Page 67.
[3] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 67.

Table 11. Core Clock Requirements—400 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	120°C ≥ T_J > 105°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	363	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 67.
[2] See Operating Conditions on Page 23.

Table 12. Core Clock Requirements—300 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	300	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	255	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	210	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	180	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	160	MHz

[1] See Ordering Guide on Page 67.

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 14. System Clock Requirements

Parameter	Condition	Max	Unit
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, V_{DDINT} ≥ 1.14 V	133[2]	MHz
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, V_{DDINT} < 1.14 V	100	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 27 on Page 34.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 27 on Page 34.

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
C_{IN}	Input Capacitance[13, 14]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			8			8	pF
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.0 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.43		14			24		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		100			113		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		125			138		mA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		6			16		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.0 V, f_{SCLK} = 25 MHz, T_J = 25°C		9.5			19.5		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 533 MHz, T_J = 25°C, ASF = 1.00					185		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.30 V, f_{CCLK} = 600 MHz, T_J = 25°C, ASF = 1.00					227		mA
$I_{DDHIBERNATE}$[15, 16]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.60 V, CLKIN=0 MHz, T_J = maximum, with voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J= 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} =0 MHz			Table 16			Table 15	mA
$I_{DDSLEEP}$[15, 17]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})	mA
I_{DDINT}[18]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 18 × ASF)			$I_{DDSLEEP}$ + (Table 18 × ASF)	mA

[1] Applies to all 300 MHz and 400 MHz speed grade models. See Ordering Guide on Page 67.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 67.
[3] Applies to all output and bidirectional pins except port F pins, port G pins, and port H pins.
[4] Applies to port F pins PF7–0.
[5] Applies to port F pins PF15–8, all port G pins, and all port H pins.
[6] Maximum combined current for Port F7–0.
[7] Maximum total current for all port F, port G, and port H pins.
[8] Applies to all input pins except PJ4.
[9] Applies to input pin PJ4 only.
[10] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[11] Applies to three-statable pins.
[12] Applies to bidirectional pins PJ2 and PJ3.
[13] Applies to all signal pins.
[14] Guaranteed, but not tested.
[15] See the *ADSP-BF537 Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[16] CLKIN must be tied to V_{DDEXT} or GND during hibernate.
[17] In the equations, the f_{SCLK} parameter is the system clock in MHz.
[18] See Table 17 for the list of I_{DDINT} power vectors covered.

System designers should refer to *Estimating Power for the ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-297. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 18).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 17).

Table 15. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})													
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
–40	3.9	4.7	6.8	8.2	9.9	12.0	14.6	17.3	20.3	24.1	27.1	28.6	36.3	44.4
0	17.0	19.2	21.9	25.0	28.2	32.1	36.9	41.8	47.7	53.8	61.0	63.8	73.2	84.1
25	35.0	39.2	44.3	50.8	56.1	63.3	69.1	76.4	84.7	93.5	104.5	109.1	123.4	138.8
40	53.0	59.2	65.3	71.9	79.1	88.0	96.6	108.0	120.0	130.7	142.6	148.5	166.5	185.6
55	76.7	84.6	93.6	103.1	113.7	123.9	136.3	148.3	162.8	178.4	194.4	201.4	223.7	247.5
70	110.1	120.0	130.9	142.2	156.5	171.3	185.2	201.7	220.6	239.7	259.8	268.8	295.9	325.2
85	150.1	164.5	178.7	193.2	210.4	228.9	247.7	268.8	291.4	314.1	341.1	351.2	384.6	420.3
100	202.3	219.2	236.5	255.8	277.8	299.8	323.8	351.2	378.8	407.5	440.4	453.4	494.3	538.2
105	223.8	241.4	260.4	282.0	303.4	328.7	354.5	381.7	410.8	443.6	477.8	492.2	535.1	581.5

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Static Current–300 MHz and 400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})											
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–40	2.6	3.2	3.7	4.5	5.5	6.6	7.9	9.3	10.5	12.5	13.9	14.8
0	6.6	7.8	8.4	9.9	10.9	12.3	13.8	15.5	17.5	19.6	21.7	23.1
25	12.2	13.5	14.8	16.4	18.2	19.9	22.7	25.6	28.4	31.8	35.7	37.2
40	17.2	19.0	20.6	22.9	25.9	28.2	31.6	34.9	38.9	42.9	47.6	49.5
55	25.7	27.8	30.9	33.7	37.3	41.4	44.8	50.0	54.8	59.4	66.1	68.4
70	37.6	41.3	44.8	48.9	53.9	58.6	63.9	69.7	76.9	84.0	92.2	94.9
85	53.7	58.3	63.7	69.0	75.9	82.9	90.5	98.4	106.4	115.3	124.6	128.1
100	75.1	82.3	88.5	95.8	104.0	112.5	121.8	130.6	141.3	153.2	164.8	169.7
105	84.5	91.2	98.2	106.0	114.2	123.0	132.4	143.3	155.0	167.4	179.8	185.4
115[2]	103.8	111.8	120.3	127.6	138.0	148.5	159.6	171.4	184.6	198.8	213.4	219.6
120[2]	115.5	123.6	132.2	141.9	152.3	163.7	175.6	189.3	202.8	217.7	232.3	238.6

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Applies to automotive grade models only.

Table 17. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.33
$I_{DD-HIGH}$	1.29
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.43

[1] See EE-297 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 18. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})													
Frequency (MHz)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
50	11.0	13.7	19.13	18.2	18.67	19.13	19.6	21.2	24.1	25.5	28.5	28.6	28.85	29.2
100	27.9	22.7	30.8	28.4	29.3	30.8	32.9	35.3	37.8	40.6	43.5	43.7	44.1	45.8
200	36.9	42.6	55.0	49.2	51.5	55.0	58.3	62.9	67.0	69.7	73.0	74.0	75.7	80.7
300	N/A	61.5	79.2	70.4	74.6	79.2	84.4	90.7	94.3	99.1	103.9	105.5	108.0	113.4
400	N/A	N/A	N/A	92.4	97.2	104.3	109.8	116.5	121.9	128.0	134.6	136.6	139.8	145.1
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	142.3	149.3	157.5	164.7	166.7	169.8	176.9
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	158.6	167.0	174.3	176.6	180.1	187.9
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	193.7	196.5	200.7	210.0

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

TIMING SPECIFICATIONS

Component specifications are subject to change without notice.

Clock and Reset Timing

Table 22. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	8.0		ns
t_{CKINH}	CLKIN High Pulse	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low	$11 \times t_{CKIN}$		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[5]	$3 \times t_{CKIN}$	$5 \times t_{CKIN}$	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 14. Since by default the PLL is multiplying the CLKIN frequency by 10 MHz, 300 MHz, and 400 MHz speed grade parts can not use the full CLKIN period range.
[2] Applies to PLL bypass mode and PLL non bypass mode.
[3] CLKIN frequency must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

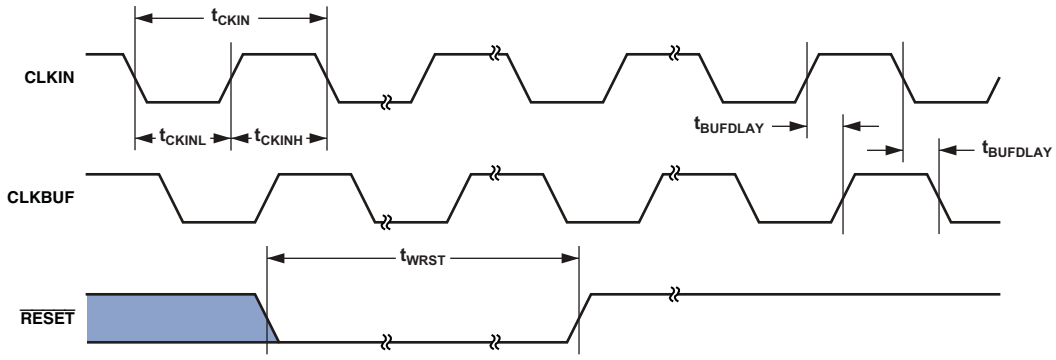
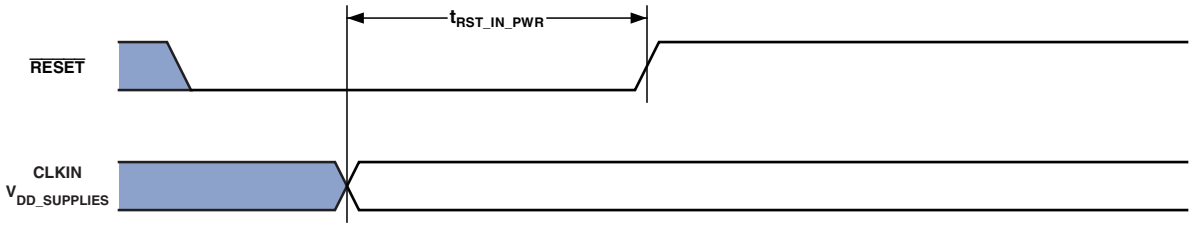


Figure 9. Clock and Reset Timing

Table 23. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



In Figure 10, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 10. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 24. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

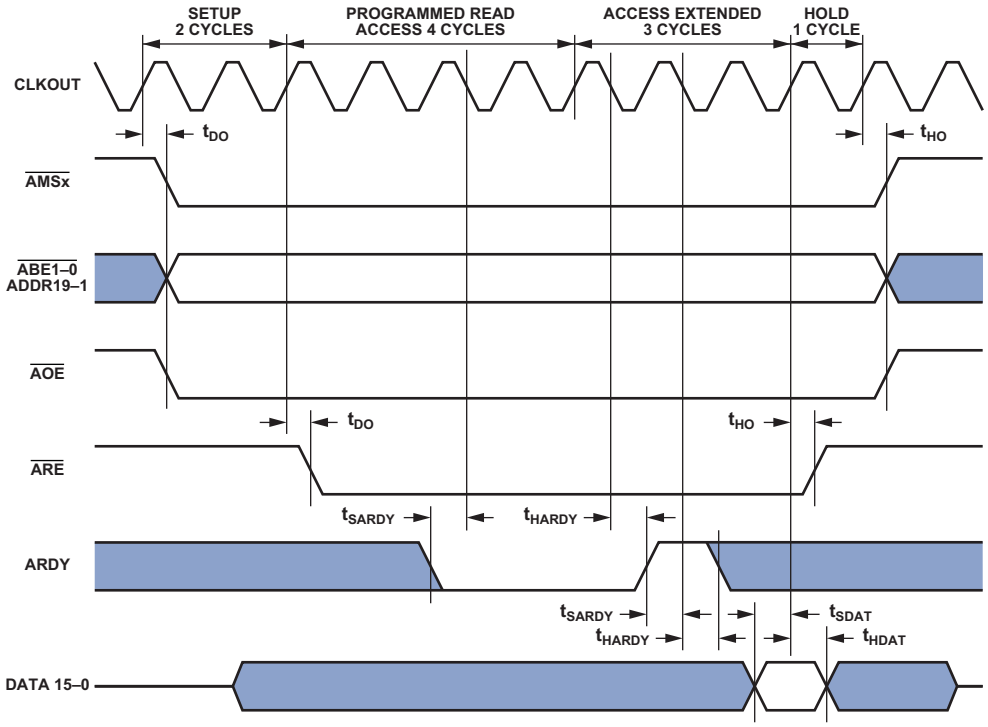


Figure 11. Asynchronous Memory Read Cycle Timing

SDRAM Interface Timing

Table 27. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA15–0 Setup Before CLKOUT	1.5		ns
t_{HSDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{DCAD}	COMMAND[1], ADDR19–1, DATA15–0 Delay After CLKOUT		4.0	ns
t_{HCAD}	COMMAND[1], ADDR19–1, DATA15–0 Hold After CLKOUT	1.0		ns
t_{DSDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENSDAT}	DATA15–0 Enable After CLKOUT	0.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J \leq +105°C$	7.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J > +105°C$	10		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.
[2] These limits are specific to the SDRAM interface only. In addition, CLKOUT must always comply with the limits in Table 14 on Page 24.

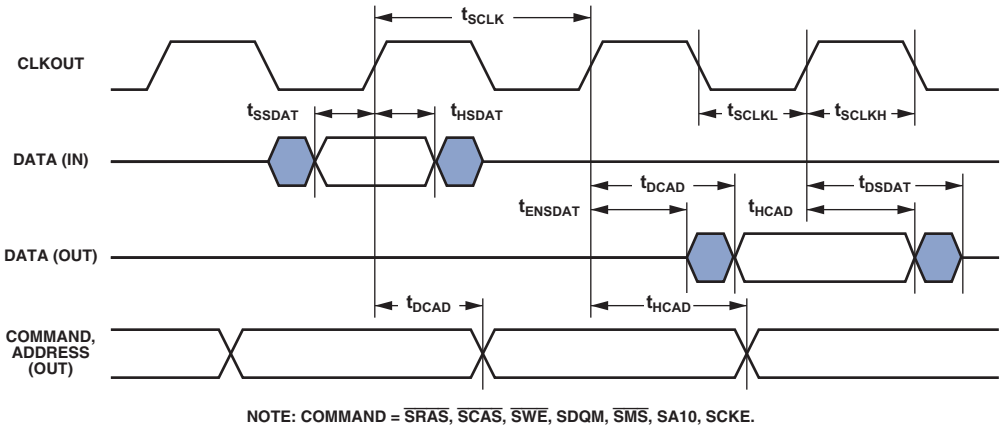


Figure 14. SDRAM Interface Timing

Parallel Peripheral Interface Timing

Table 29 and Figure 16 on Page 36, Figure 20 on Page 39, and Figure 23 on Page 41 describe parallel peripheral interface operations.

Table 29. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width[1]	6.0		ns
t_{PCLK}	PPI_CLK Period[1]	15.0		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK	6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

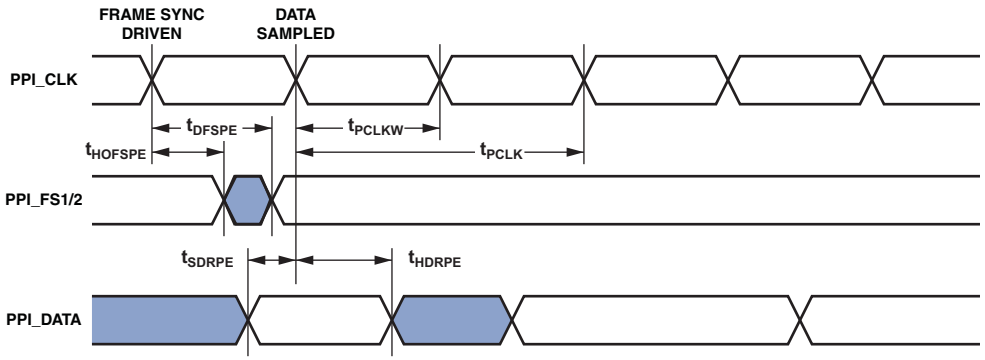


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

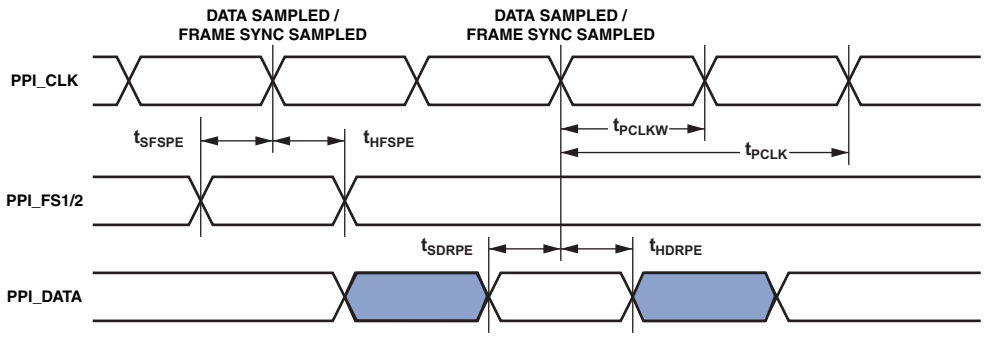


Figure 17. PPI GP Rx Mode with External Frame Sync Timing

Table 32. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2]		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only. TSCLKx is tied to RSCLKx.

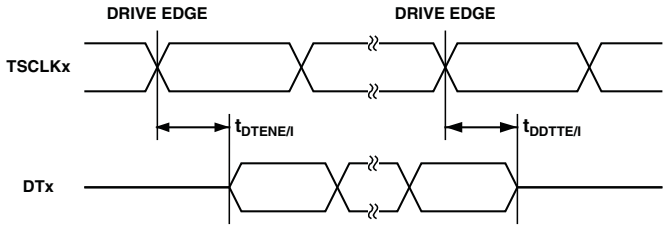


Figure 22. Enable and Three-State

General-Purpose Port Timing

Table 36 and Figure 26 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	0	6	ns

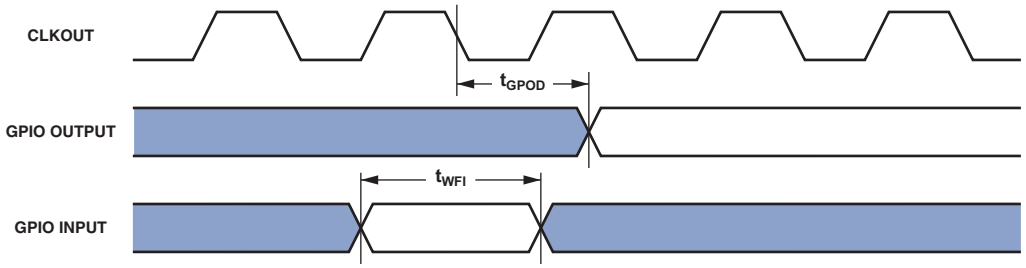


Figure 26. General-Purpose Port Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF537 Blackfin Processor Hardware Reference*.

JTAG Test and Emulation Port Timing

Table 39 and Figure 29 describe JTAG port operations.

Table 39. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay From TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA15–0, $\overline{\text{BR}}$, ARDY, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH15–0, MDIO, TCK, $\overline{\text{TRST}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, RTXI, BMODE2–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{\text{ABE1–0}}$, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, SCL, SDA, MDC, MDIO, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH15–0, RTXO, TDO, $\overline{\text{EMU}}$, XTAL, VROUT1–0.

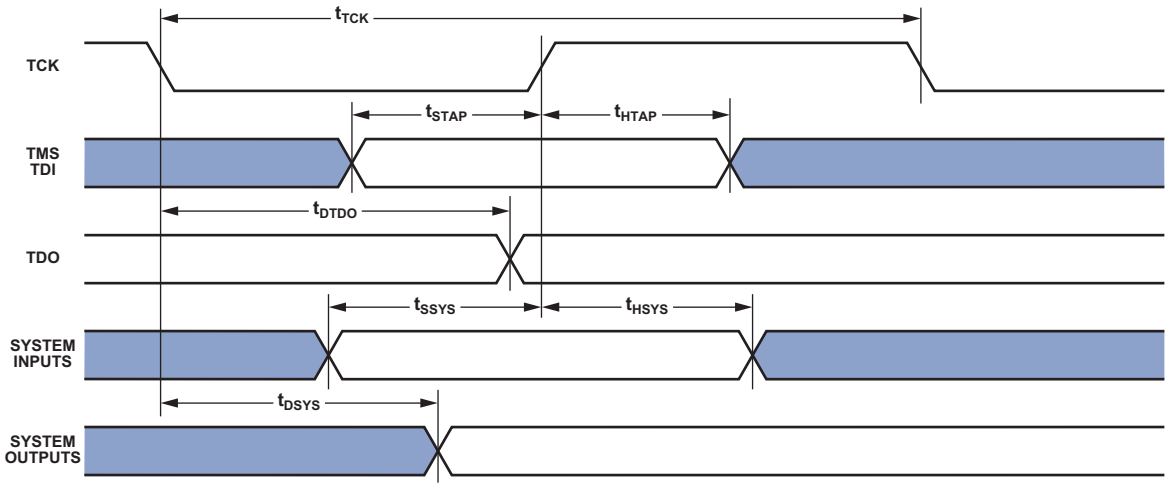


Figure 29. JTAG Port Timing

182-BALL CSP_BGA BALL ASSIGNMENT

Table 49 lists the CSP_BGA ball assignment by signal mnemonic. Table 50 on Page 58 lists the CSP_BGA ball assignment by ball number.

Table 49. 182-Ball CSP_BGA Ball Assignment (Alphabetically by Signal Mnemonic)

Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.
$\overline{ABE0}$	H13	CLKOUT	B14	GND	L6	PG8	E3	$\overline{SRAS}$	D13
$\overline{ABE1}$	H12	DATA0	M9	GND	L8	PG9	E4	$\overline{SWE}$	D12
ADDR1	J14	DATA1	N9	GND	L10	PH0	C2	TCK	P2
ADDR10	M13	DATA10	N6	GND	M4	PH1	C3	TDI	M3
ADDR11	M14	DATA11	P6	GND	M10	PH10	B6	TDO	N3
ADDR12	N14	DATA12	M5	GND	P14	PH11	A2	TMS	N2
ADDR13	N13	DATA13	N5	$\overline{NMI}$	B10	PH12	A3	$\overline{TRST}$	N1
ADDR14	N12	DATA14	P5	PF0	M1	PH13	A4	V_{DDEXT}	A1
ADDR15	M11	DATA15	P4	PF1	L1	PH14	A5	V_{DDEXT}	C12
ADDR16	N11	DATA2	P9	PF10	J2	PH15	A6	V_{DDEXT}	E6
ADDR17	P13	DATA3	M8	PF11	J3	PH2	C4	V_{DDEXT}	E11
ADDR18	P12	DATA4	N8	PF12	H1	PH3	C5	V_{DDEXT}	F4
ADDR19	P11	DATA5	P8	PF13	H2	PH4	C6	V_{DDEXT}	F12
ADDR2	K14	DATA6	M7	PF14	H3	PH5	B1	V_{DDEXT}	H5
ADDR3	L14	DATA7	N7	PF15	H4	PH6	B2	V_{DDEXT}	H10
ADDR4	J13	DATA8	P7	PF2	L2	PH7	B3	V_{DDEXT}	J11
ADDR5	K13	DATA9	M6	PF3	L3	PH8	B4	V_{DDEXT}	J12
ADDR6	L13	$\overline{EMU}$	M2	PF4	L4	PH9	B5	V_{DDEXT}	K7
ADDR7	K12	GND	A10	PF5	K1	PJ0	C7	V_{DDEXT}	K9
ADDR8	L12	GND	A14	PF6	K2	PJ1	B7	V_{DDEXT}	L7
ADDR9	M12	GND	D4	PF7	K3	PJ10	D10	V_{DDEXT}	L9
$\overline{AMS0}$	E14	GND	E7	PF8	K4	PJ11	D11	V_{DDEXT}	L11
$\overline{AMS1}$	F14	GND	E9	PF9	J1	PJ2	B11	V_{DDEXT}	P1
$\overline{AMS2}$	F13	GND	F5	PG0	G1	PJ3	C11	V_{DDINT}	E5
$\overline{AMS3}$	G12	GND	F6	PG1	G2	PJ4	D7	V_{DDINT}	E8
$\overline{AOE}$	G13	GND	F10	PG10	D1	PJ5	D8	V_{DDINT}	E10
ARDY	E13	GND	F11	PG11	D2	PJ6	C8	V_{DDINT}	G10
$\overline{ARE}$	G14	GND	G4	PG12	D3	PJ7	B8	V_{DDINT}	K5
$\overline{AWE}$	H14	GND	G5	PG13	D5	PJ8	D9	V_{DDINT}	K8
$\overline{BG}$	P10	GND	G11	PG14	D6	PJ9	C9	V_{DDINT}	K10
$\overline{BGH}$	N10	GND	H11	PG15	C1	$\overline{RESET}$	C10	V_{DDRTC}	B9
BMODE0	N4	GND	J4	PG2	G3	RTXO	A8	VROUT0	A13
BMODE1	P3	GND	J5	PG3	F1	RTXI	A9	VROUT1	B12
BMODE2	L5	GND	J9	PG4	F2	SA10	E12	XTAL	A11
$\overline{BR}$	D14	GND	J10	PG5	F3	$\overline{SCAS}$	C14		
CLKBUF	A7	GND	K6	PG6	E1	SCKE	B13		
CLKIN	A12	GND	K11	PG7	E2	$\overline{SMS}$	C13		

Figure 63 shows the top view of the CSP_BGA ball configuration. Figure 64 shows the bottom view of the CSP_BGA ball configuration.

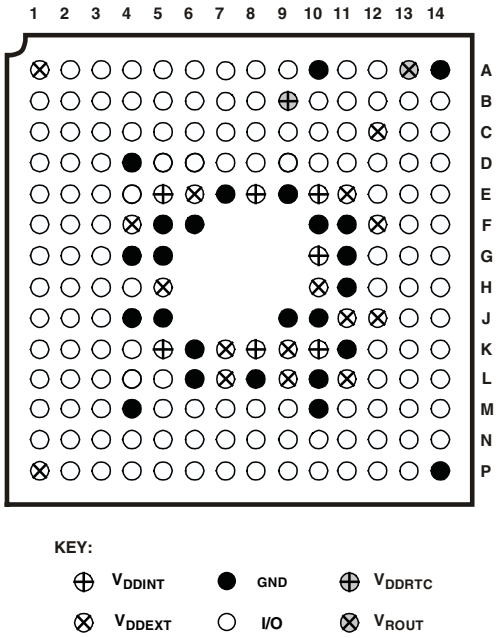


Figure 63. 182-Ball CSP_BGA Configuration (Top View)

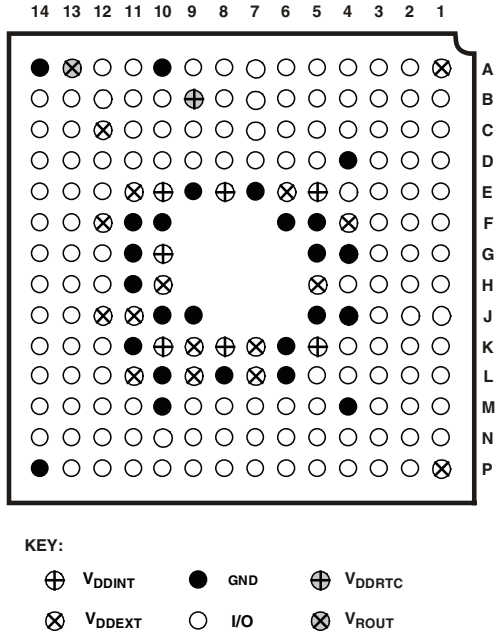


Figure 64. 182-Ball CSP_BGA Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 67 and Figure 68 are shown in millimeters.

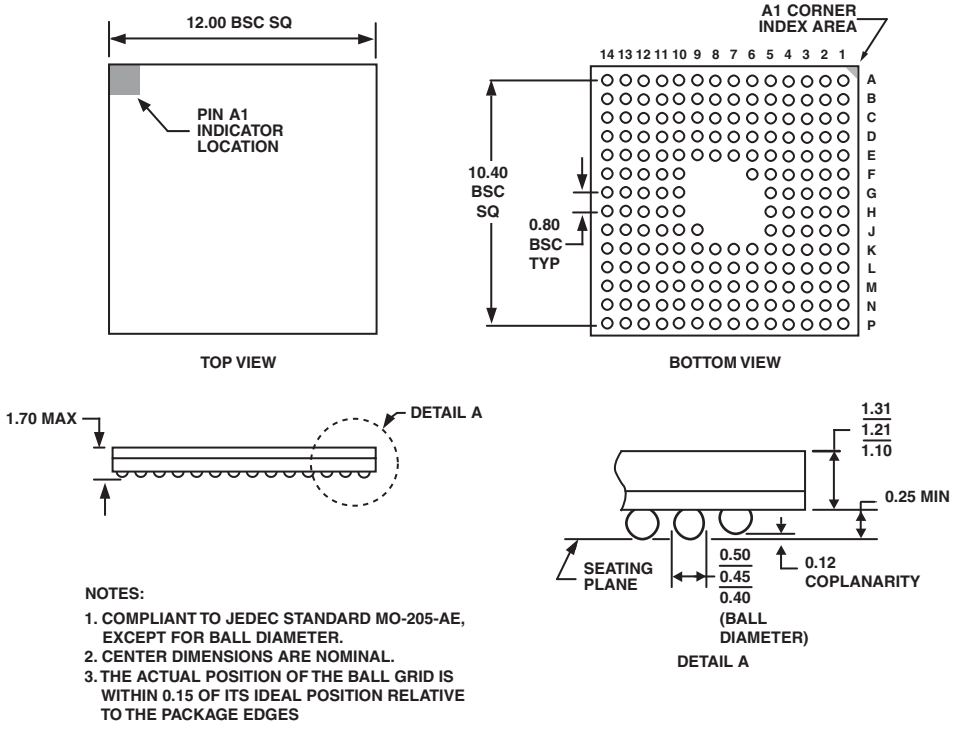


Figure 67. 182-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-182)
Dimensions shown in millimeters