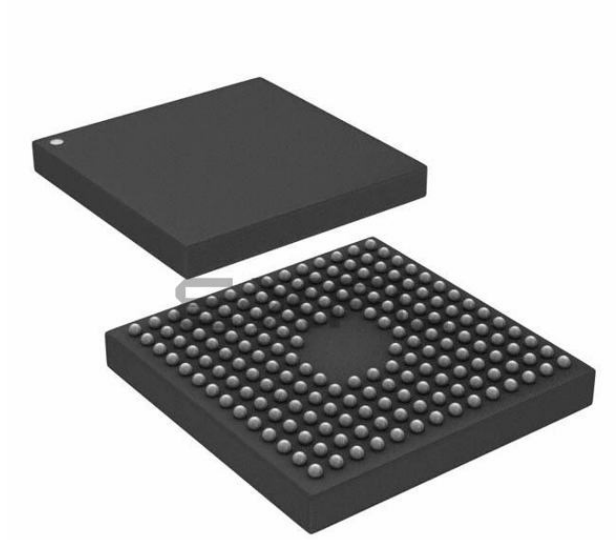

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed Point |
| Interface | CAN, SPI, SSP, TWI, UART |
| Clock Rate | 400MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 132kB |
| Voltage - I/O | 2.50V, 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 182-LFBGA, CSPBGA |
| Supplier Device Package | 182-CSPBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-bf534bbcz-4a |

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify, length, and base registers (for circular buffering), and eight additional 32-bit pointer registers (for C-style indexed stack manipulation).

Blackfin processors support a modified Harvard architecture in combination with a hierarchical memory structure. Level 1 (L1) memories are those that typically operate at the full processor speed with little or no latency. At the L1 level, the instruction memory holds instructions only. The two data memories hold data, and a dedicated scratchpad data memory stores stack and local variable information.

In addition, multiple L1 memory blocks are provided, offering a configurable mix of SRAM and cache. The memory management unit (MMU) provides memory protection for individual tasks that may be operating on the core and can protect system registers from unintended access.

The architecture provides three modes of operation: user mode, supervisor mode, and emulation mode. User mode has restricted access to certain system resources, thus providing a protected software environment, while supervisor mode has unrestricted access to the system and core resources.

The Blackfin processor instruction set has been optimized so that 16-bit opcodes represent the most frequently used instructions, resulting in excellent compiled code density. Complex DSP instructions are encoded into 32-bit opcodes, representing fully featured multifunction instructions. Blackfin processors support a limited multi-issue capability, where a 32-bit instruction can be issued in parallel with two 16-bit instructions, allowing the programmer to use many of the core resources in a single instruction cycle.

The Blackfin processor assembly language uses an algebraic syntax for ease of coding and readability. The architecture has been optimized for use in conjunction with the C/C++ compiler, resulting in fast and efficient software implementations.

## MEMORY ARCHITECTURE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low latency on-chip memory as cache or SRAM, and larger, lower cost, and performance off-chip memory systems. (See Figure 3).

The on-chip L1 memory system is the highest performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with SDRAM, flash memory, and SRAM, optionally accessing up to 516M bytes of physical memory.

The memory DMA controller provides high bandwidth data-movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

### *Internal (On-Chip) Memory*

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have three blocks of on-chip memory providing high-bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 64K bytes SRAM, of which 16K bytes can be configured as a four-way set-associative cache. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of up to two banks of up to 32K bytes each. Each memory bank is configurable, offering both cache and SRAM functionality. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories, but is only accessible as data SRAM, and cannot be configured as cache memory.

### *External (Off-Chip) Memory*

External memory is accessed via the EBIU. This 16-bit interface provides a glueless connection to a bank of synchronous DRAM (SDRAM) as well as up to four banks of asynchronous memory devices including flash, EPROM, ROM, SRAM, and memory mapped I/O devices.

The PC133-compliant SDRAM controller can be programmed to interface to up to 128M bytes of SDRAM. A separate row can be open for each SDRAM internal bank, and the SDRAM controller supports up to 4 internal SDRAM banks, improving overall performance.

The asynchronous memory controller can be programmed to control up to four banks of devices with very flexible timing parameters for a wide variety of devices. Each bank occupies a 1M byte segment regardless of the size of the devices used, so that these banks are only contiguous if each is fully populated with 1M byte of memory.

### *I/O Memory Space*

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one which contains the control MMRs for all core functions, and the other which contains the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

### *Booting*

The Blackfin processor contains a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the Blackfin processor is configured to boot from boot ROM

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

## CONTROLLER AREA NETWORK (CAN)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors offer a CAN controller that is a communication controller implementing the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well-suited for control applications due to its capability to communicate reliably over a network, since the protocol incorporates CRC checking message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (eight receive only, eight transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wake-up from hibernation mode (lowest static power consumption mode).
- Interrupts, including: Tx complete, Rx complete, error, global.

The electrical characteristics of each network connection are very demanding so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high-speed, fault-tolerant, single-wire transceivers.

## TWI CONTROLLER INTERFACE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used $I^2C$® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

## 10/100 ETHERNET MAC

The ADSP-BF536 and ADSP-BF537 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet Media Access Controller (MAC) that supports both 10-BaseT (10 Mbps) and 100-BaseT (100 Mbps) operation. The 10/100 Ethernet MAC peripheral is fully compliant to the IEEE 802.3-2002 standard, and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are

- Support of MII and RMII protocols for external PHYs.
- Full duplex and half duplex modes.
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS.
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing.
- Flow control (in full-duplex operation): generation and detection of PAUSE frames.
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers.
- SCLK operating range down to 25 MHz (active and sleep operating modes).
- Internal loopback from Tx to Rx.

Some advanced features are

- Buffered crystal output to external PHY for support of a single crystal system.
- Automatic checksum computation of IP header and IP payload fields of Rx frames.
- Independent 32-bit descriptor-driven Rx and Tx DMA channels.
- Frame status delivery to memory via DMA, including frame completion semaphores, for efficient buffer queue management in software.
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations.
- Convenient frame alignment modes support even 32-bit alignment of encapsulated Rx or Tx IP packet data in memory after the 14-byte MAC header.
- Programmable Ethernet event interrupt supports any combination of
  - Any selected Rx or Tx frame status conditions.
  - PHY interrupt condition.
  - Wake-up frame detected.
  - Any selected MAC management counter(s) at half-full.
  - DMA descriptor error.
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value.

- Programmable Rx address filters, including a 64-bit address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames.
- Advanced power management supporting unattended transfer of Rx and Tx frames and status to/from external memory via DMA during low power sleep mode.
- System wake-up from sleep operating mode upon magic packet or any of four user-definable wake-up frame filters.
- Support for 802.3Q tagged VLAN frames.
- Programmable MDC clock rate and preamble suppression.
- In RMII operation, 7 unused pins can be configured as GPIO pins for other purposes.

## PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors group the many peripheral signals to four ports—Port F, Port G, Port H, and Port J. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Eight of the pins (Port F7–0) offer high source/high sink current capabilities.

### *General-Purpose I/O (GPIO)*

The processors have 48 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Port J does not provide GPIO functionality. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output or input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processors employ a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

## PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

### *General-Purpose Mode Descriptions*

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode – Frame syncs and data are inputs into the PPI.
2. Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode – Frame syncs and data are outputs from the PPI.

#### Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

#### Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

**Table 9. Pin Descriptions (Continued)**

| Pin Name | Type | Function | Driver Type[1] |
|---|---|---|---|
| *Port H: GPIO/10/100 Ethernet MAC* (On ADSP-BF534, these pins are GPIO only) | | | |
| PH0 – GPIO/*ETxD0* | I/O | GPIO/*Ethernet MII or RMII Transmit D0* | E |
| PH1 – GPIO/*ETxD1* | I/O | GPIO/*Ethernet MII or RMII Transmit D1* | E |
| PH2 – GPIO/*ETxD2* | I/O | GPIO/*Ethernet MII Transmit D2* | E |
| PH3 – GPIO/*ETxD3* | I/O | GPIO/*Ethernet MII Transmit D3* | E |
| PH4 – GPIO/*ETxEN* | I/O | GPIO/*Ethernet MII or RMII Transmit Enable* | E |
| PH5 – GPIO/*MII TxCLK/RMII REF_CLK* | I/O | GPIO/*Ethernet MII Transmit Clock/RMII Reference Clock* | E |
| PH6 – GPIO/*MII* $\overline{PHYINT}$/*RMII* $\overline{MDINT}$ | I/O | GPIO/*Ethernet MII PHY Interrupt/RMII Management Data Interrupt* (This pin should be pulled high when used as a hibernate wake-up.) | E |
| PH7 – GPIO/*COL* | I/O | GPIO/*Ethernet Collision* | E |
| PH8 – GPIO/*ERxD0* | I/O | GPIO/*Ethernet MII or RMII Receive D0* | E |
| PH9 – GPIO/*ERxD1* | I/O | GPIO/*Ethernet MII or RMII Receive D1* | E |
| PH10 – GPIO/*ERxD2* | I/O | GPIO/*Ethernet MII Receive D2* | E |
| PH11 – GPIO/*ERxD3* | I/O | GPIO/*Ethernet MII Receive D3* | E |
| PH12 – GPIO/*ERxDV/TACLK5* | I/O | GPIO/*Ethernet MII Receive Data Valid/Alternate Timer5 Input Clock* | E |
| PH13 – GPIO/*ERxCLK/TACLK6* | I/O | GPIO/*Ethernet MII Receive Clock/Alternate Timer6 Input Clock* | E |
| PH14 – GPIO/*ERxER/TACLK7* | I/O | GPIO/*Ethernet MII or RMII Receive Error/Alternate Timer7 Input Clock* | E |
| PH15 – GPIO/*MII CRS/RMII CRS_DV* | I/O | GPIO/*Ethernet MII Carrier Sense/Ethernet RMII Carrier Sense and Receive Data Valid* | E |
| *Port J: SPORT0/TWI/SPI Select/CAN* | | | |
| PJ0 – MDC | O | Ethernet Management Channel Clock (On ADSP-BF534 processors, do not connect this pin.) | E |
| PJ1 – MDIO | I/O | Ethernet Management Channel Serial Data (On ADSP-BF534 processors, tie this pin to ground.) | E |
| PJ2 – SCL | I/O | TWI Serial Clock (This pin is an open-drain output and requires a pull-up resistor.) | F |
| PJ3 – SDA | I/O | TWI Serial Data (This pin is an open-drain output and requires a pull-up resistor.) | F |
| PJ4 – DR0SEC/*CANRX/TACI0* | I | SPORT0 Receive Data Secondary/*CAN Receive/Timer0 Alternate Input Capture* | |
| PJ5 – DT0SEC/*CANTX/SPI SSEL7* | O | SPORT0 Transmit Data Secondary/*CAN Transmit/SPI Slave Select Enable 7* | C |
| PJ6 – RSCLK0/*TACLK2* | I/O | SPORT0 Receive Serial Clock/*Alternate Timer2 Clock Input* | D |
| PJ7 – RFS0/*TACLK3* | I/O | SPORT0 Receive Frame Sync/*Alternate Timer3 Clock Input* | C |
| PJ8 – DR0PRI/*TACLK4* | I | SPORT0 Receive Data Primary/*Alternate Timer4 Clock Input* | |
| PJ9 – TSCLK0/*TACLK1* | I/O | SPORT0 Transmit Serial Clock/*Alternate Timer1 Clock Input* | D |
| PJ10 – TFS0/*SPI SSEL3* | I/O | SPORT0 Transmit Frame Sync/*SPI Slave Select Enable 3* | C |
| PJ11 – DT0PRI/*SPI SSEL2* | O | SPORT0 Transmit Data Primary/*SPI Slave Select Enable 2* | C |
| *Real-Time Clock* | | | |
| RTXI | I | RTC Crystal Input (This pin should be pulled low when not used.) | |
| RTXO | O | RTC Crystal Output (Does not three-state in hibernate.) | |
| *JTAG Port* | | | |
| TCK | I | JTAG Clock | |
| TDO | O | JTAG Serial Data Out | C |
| TDI | I | JTAG Serial Data In | |
| TMS | I | JTAG Mode Select | |
| $\overline{TRST}$ | I | JTAG Reset (This pin should be pulled low if the JTAG port is not used.) | |
| $\overline{EMU}$ | O | Emulation Output | C |

| Parameter | | Test Conditions | 300 MHz/400 MHz[1] Min | Typ | Max | 500 MHz/533 MHz/600 MHz[2] Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance[13, 14] | $f_{IN}$ = 1 MHz, $T_{AMBIENT}$ = 25°C, $V_{IN}$ = 2.5 V | | | 8 | | | 8 | pF |
| $I_{DD-IDLE}$ | $V_{DDINT}$ Current in Idle | $V_{DDINT}$ = 1.0 V, $f_{CCLK}$ = 50 MHz, $T_J$ = 25°C, ASF = 0.43 | | 14 | | | 24 | | mA |
| $I_{DD-TYP}$ | $V_{DDINT}$ Current | $V_{DDINT}$ = 1.14 V, $f_{CCLK}$ = 300 MHz, $T_J$ = 25°C, ASF = 1.00 | | 100 | | | 113 | | mA |
| $I_{DD-TYP}$ | $V_{DDINT}$ Current | $V_{DDINT}$ = 1.14 V, $f_{CCLK}$ = 400 MHz, $T_J$ = 25°C, ASF = 1.00 | | 125 | | | 138 | | mA |
| $I_{DDDEEPSLEEP}$[15] | $V_{DDINT}$ Current in Deep Sleep Mode | $V_{DDINT}$ = 1.0 V, $f_{CCLK}$ = 0 MHz, $T_J$ = 25°C, ASF = 0.00 | | 6 | | | 16 | | mA |
| $I_{DDSLEEP}$ | $V_{DDINT}$ Current in Sleep Mode | $V_{DDINT}$ = 1.0 V, $f_{SCLK}$ = 25 MHz, $T_J$ = 25°C | | 9.5 | | | 19.5 | | mA |
| $I_{DD-TYP}$ | $V_{DDINT}$ Current | $V_{DDINT}$ = 1.20 V, $f_{CCLK}$ = 533 MHz, $T_J$ = 25°C, ASF = 1.00 | | | | | 185 | | mA |
| $I_{DD-TYP}$ | $V_{DDINT}$ Current | $V_{DDINT}$ = 1.30 V, $f_{CCLK}$ = 600 MHz, $T_J$ = 25°C, ASF = 1.00 | | | | | 227 | | mA |
| $I_{DDHIBERNATE}$[15, 16] | $V_{DDEXT}$ Current in Hibernate State | $V_{DDEXT}$ = 3.60 V, CLKIN=0 MHz, $T_J$ = maximum, with voltage regulator off ($V_{DDINT}$ = 0 V) | | 50 | 100 | | 50 | 100 | µA |
| $I_{DDRTC}$ | $V_{DDRTC}$ Current | $V_{DDRTC}$ = 3.3 V, $T_J$= 25°C | | 20 | | | 20 | | µA |
| $I_{DDDEEPSLEEP}$[15] | $V_{DDINT}$ Current in Deep Sleep Mode | $f_{CCLK}$ = 0 MHz, $f_{SCLK}$ =0 MHz | | | Table 16 | | | Table 15 | mA |
| $I_{DDSLEEP}$[15, 17] | $V_{DDINT}$ Current in Sleep Mode | $f_{CCLK}$ = 0 MHz, $f_{SCLK}$ > 0 MHz | | | $I_{DDDEEPSLEEP}$ + (0.14 × $V_{DDINT}$ × $f_{SCLK}$) | | | $I_{DDDEEPSLEEP}$ + (0.14 × $V_{DDINT}$ × $f_{SCLK}$) | mA |
| $I_{DDINT}$[18] | $V_{DDINT}$ Current | $f_{CCLK}$ > 0 MHz, $f_{SCLK}$ > 0 MHz | | | $I_{DDSLEEP}$ + (Table 18 × ASF) | | | $I_{DDSLEEP}$ + (Table 18 × ASF) | mA |

[1] Applies to all 300 MHz and 400 MHz speed grade models. See Ordering Guide on Page 67.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 67.
[3] Applies to all output and bidirectional pins except port F pins, port G pins, and port H pins.
[4] Applies to port F pins PF7–0.
[5] Applies to port F pins PF15–8, all port G pins, and all port H pins.
[6] Maximum combined current for Port F7–0.
[7] Maximum total current for all port F, port G, and port H pins.
[8] Applies to all input pins except PJ4.
[9] Applies to input pin PJ4 only.
[10] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[11] Applies to three-statable pins.
[12] Applies to bidirectional pins PJ2 and PJ3.
[13] Applies to all signal pins.
[14] Guaranteed, but not tested.
[15] See the *ADSP-BF537 Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[16] CLKIN must be tied to $V_{DDEXT}$ or GND during hibernate.
[17] In the equations, the $f_{SCLK}$ parameter is the system clock in MHz.
[18] See Table 17 for the list of $I_{DDINT}$ power vectors covered.

System designers should refer to *Estimating Power for the ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-297. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry ($V_{DDINT}$). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage ($V_{DDINT}$) and temperature (see Table 16 or Table 15), and $I_{DDINT}$ specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage ($V_{DDINT}$) and frequency (Table 18).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 17).

**Table 15. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]**

| | Voltage ($V_{DDINT}$) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 0.80 V | 0.85 V | 0.90 V | 0.95 V | 1.00 V | 1.05 V | 1.10 V | 1.15 V | 1.20 V | 1.25 V | 1.30 V | 1.32 V | 1.375 V | 1.43 V |
| –40 | 3.9 | 4.7 | 6.8 | 8.2 | 9.9 | 12.0 | 14.6 | 17.3 | 20.3 | 24.1 | 27.1 | 28.6 | 36.3 | 44.4 |
| 0 | 17.0 | 19.2 | 21.9 | 25.0 | 28.2 | 32.1 | 36.9 | 41.8 | 47.7 | 53.8 | 61.0 | 63.8 | 73.2 | 84.1 |
| 25 | 35.0 | 39.2 | 44.3 | 50.8 | 56.1 | 63.3 | 69.1 | 76.4 | 84.7 | 93.5 | 104.5 | 109.1 | 123.4 | 138.8 |
| 40 | 53.0 | 59.2 | 65.3 | 71.9 | 79.1 | 88.0 | 96.6 | 108.0 | 120.0 | 130.7 | 142.6 | 148.5 | 166.5 | 185.6 |
| 55 | 76.7 | 84.6 | 93.6 | 103.1 | 113.7 | 123.9 | 136.3 | 148.3 | 162.8 | 178.4 | 194.4 | 201.4 | 223.7 | 247.5 |
| 70 | 110.1 | 120.0 | 130.9 | 142.2 | 156.5 | 171.3 | 185.2 | 201.7 | 220.6 | 239.7 | 259.8 | 268.8 | 295.9 | 325.2 |
| 85 | 150.1 | 164.5 | 178.7 | 193.2 | 210.4 | 228.9 | 247.7 | 268.8 | 291.4 | 314.1 | 341.1 | 351.2 | 384.6 | 420.3 |
| 100 | 202.3 | 219.2 | 236.5 | 255.8 | 277.8 | 299.8 | 323.8 | 351.2 | 378.8 | 407.5 | 440.4 | 453.4 | 494.3 | 538.2 |
| 105 | 223.8 | 241.4 | 260.4 | 282.0 | 303.4 | 328.7 | 354.5 | 381.7 | 410.8 | 443.6 | 477.8 | 492.2 | 535.1 | 581.5 |

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

**Table 16. Static Current–300 MHz and 400 MHz Speed Grade Devices (mA)[1]**

| | Voltage ($V_{DDINT}$) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 0.80 V | 0.85 V | 0.90 V | 0.95 V | 1.00 V | 1.05 V | 1.10 V | 1.15 V | 1.20 V | 1.25 V | 1.30 V | 1.32 V |
| –40 | 2.6 | 3.2 | 3.7 | 4.5 | 5.5 | 6.6 | 7.9 | 9.3 | 10.5 | 12.5 | 13.9 | 14.8 |
| 0 | 6.6 | 7.8 | 8.4 | 9.9 | 10.9 | 12.3 | 13.8 | 15.5 | 17.5 | 19.6 | 21.7 | 23.1 |
| 25 | 12.2 | 13.5 | 14.8 | 16.4 | 18.2 | 19.9 | 22.7 | 25.6 | 28.4 | 31.8 | 35.7 | 37.2 |
| 40 | 17.2 | 19.0 | 20.6 | 22.9 | 25.9 | 28.2 | 31.6 | 34.9 | 38.9 | 42.9 | 47.6 | 49.5 |
| 55 | 25.7 | 27.8 | 30.9 | 33.7 | 37.3 | 41.4 | 44.8 | 50.0 | 54.8 | 59.4 | 66.1 | 68.4 |
| 70 | 37.6 | 41.3 | 44.8 | 48.9 | 53.9 | 58.6 | 63.9 | 69.7 | 76.9 | 84.0 | 92.2 | 94.9 |
| 85 | 53.7 | 58.3 | 63.7 | 69.0 | 75.9 | 82.9 | 90.5 | 98.4 | 106.4 | 115.3 | 124.6 | 128.1 |
| 100 | 75.1 | 82.3 | 88.5 | 95.8 | 104.0 | 112.5 | 121.8 | 130.6 | 141.3 | 153.2 | 164.8 | 169.7 |
| 105 | 84.5 | 91.2 | 98.2 | 106.0 | 114.2 | 123.0 | 132.4 | 143.3 | 155.0 | 167.4 | 179.8 | 185.4 |
| 115[2] | 103.8 | 111.8 | 120.3 | 127.6 | 138.0 | 148.5 | 159.6 | 171.4 | 184.6 | 198.8 | 213.4 | 219.6 |
| 120[2] | 115.5 | 123.6 | 132.2 | 141.9 | 152.3 | 163.7 | 175.6 | 189.3 | 202.8 | 217.7 | 232.3 | 238.6 |

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Applies to automotive grade models only.

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 19 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 19. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Internal (Core) Supply Voltage ($V_{DDINT}$) | −0.3 V to +1.43 V |
| External (I/O) Supply Voltage ($V_{DDEXT}$) | −0.3 V to +3.8 V |
| Input Voltage[1] | −0.5 V to +3.6 V |
| Input Voltage[1, 2] | −0.5 V to +5.5 V |
| Output Voltage Swing | −0.5 V to $V_{DDEXT}$ + 0.5 V |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature While Biased | +125°C |

[1] Applies only when $V_{DDEXT}$ is within specifications. When $V_{DDEXT}$ is outside specifications, the range is $V_{DDEXT}$ ± 0.2 V.
[2] Applies to 5 V tolerant pins SCL, SDA, and PJ4. For duty cycles, see Table 20.

**Table 20. Maximum Duty Cycle for Input[1] Transient Voltage**

| $V_{IN}$ Min (V)[2] | $V_{IN}$ Max (V)[2] | Maximum Duty Cycle[3] |
|---|---|---|
| −0.50 | +3.80 | 100% |
| −0.70 | +4.00 | 40% |
| −0.80 | +4.10 | 25% |
| −0.90 | +4.20 | 15% |
| −1.00 | +4.30 | 10% |

[1] Applies to all signal pins with the exception of CLKIN, XTAL, and VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PACKAGE INFORMATION

The information presented in Figure 8 and Table 21 provide details about the package branding for the Blackfin processors. For a complete listing of product availability, see Ordering Guide on Page 67.


*Figure 8. Product Information on Package*

**Table 21. Package Brand Information[1]**

| Brand Key | Field Description |
|---|---|
| t | Temperature Range |
| pp | Package Type |
| Z | RoHS Compliant Designation |
| ccc | See Ordering Guide |
| vvvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| # | RoHS Compliant Designation |
| yyww | Date Code |

[1] Nonautomotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

## TIMING SPECIFICATIONS

Component specifications are subject to change without notice.

### *Clock and Reset Timing*

**Table 22. Clock Input and Reset Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{CKIN}$ | CLKIN Period[1, 2, 3, 4] | 20.0 | 100.0 | ns |
| $t_{CKINL}$ | CLKIN Low Pulse | 8.0 | | ns |
| $t_{CKINH}$ | CLKIN High Pulse | 8.0 | | ns |
| $t_{BUFDLAY}$ | CLKIN to CLKBUF Delay | | 10 | ns |
| $t_{WRST}$ | $\overline{\text{RESET}}$ Asserted Pulse Width Low | $11 \times t_{CKIN}$ | | ns |
| $t_{NOBOOT}$ | $\overline{\text{RESET}}$ Deassertion to First External Access Delay[5] | $3 \times t_{CKIN}$ | $5 \times t_{CKIN}$ | ns |

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed $f_{VCO}$, $f_{CCLK}$, and $f_{SCLK}$ settings discussed in Table 10 through Table 14. Since by default the PLL is multiplying the CLKIN frequency by 10 MHz, 300 MHz, and 400 MHz speed grade parts can not use the full CLKIN period range.
[2] Applies to PLL bypass mode and PLL non bypass mode.
[3] CLKIN frequency must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum $t_{CKIN}$ period is 50 ns.
[5] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

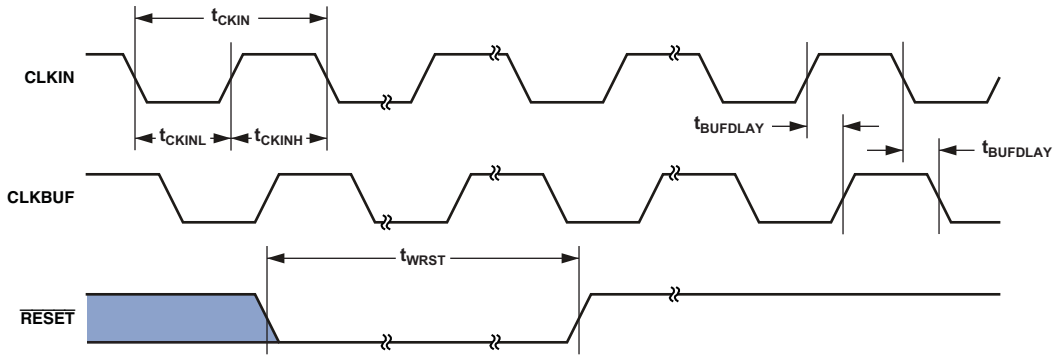
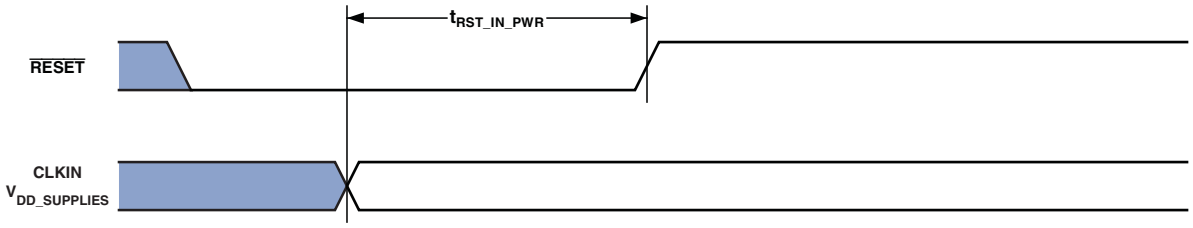



*Figure 9. Clock and Reset Timing*

**Table 23. Power-Up Reset Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{RST\_IN\_PWR}$ | $\overline{\text{RESET}}$ Deasserted After the $V_{DDINT}$, $V_{DDEXT}$, $V_{DDRTC}$, and CLKIN Pins Are Stable and Within Specification | $3500 \times t_{CKIN}$ | | ns |




In Figure 10, $V_{DD\_SUPPLIES}$ is $V_{DDINT}$, $V_{DDEXT}$, $V_{DDRTC}$

*Figure 10. Power-Up Reset Timing*

### *Asynchronous Memory Write Cycle Timing*

**Table 25. Asynchronous Memory Write Cycle Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SARDY}$ | ARDY Setup Before CLKOUT | 4.0 | | ns |
| $t_{HARDY}$ | ARDY Hold After CLKOUT | 0.0 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DDAT}$ | DATA15–0 Disable After CLKOUT | | 6.0 | ns |
| $t_{ENDAT}$ | DATA15–0 Enable After CLKOUT | 1.0 | | ns |
| $t_{DO}$ | Output Delay After CLKOUT[1] | | 6.0 | ns |
| $t_{HO}$ | Output Hold After CLKOUT[1] | 0.8 | | ns |

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{AWE}$.

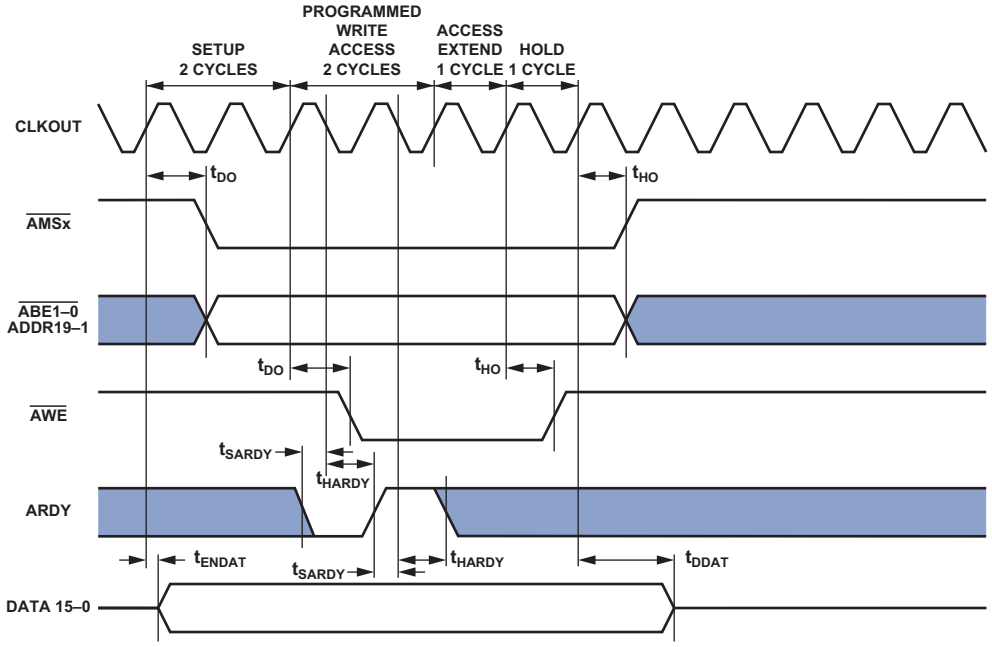



*Figure 12. Asynchronous Memory Write Cycle Timing*

### *External Port Bus Request and Grant Cycle Timing*

Table 26 and Figure 13 describe external port bus request and bus grant operations.

**Table 26. External Port Bus Request and Grant Cycle Timing**

| Parameter[1, 2] | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{BS}$ | $\overline{BR}$ Asserted to CLKOUT Low Setup | 4.6 | | ns |
| $t_{BH}$ | CLKOUT Low to $\overline{BR}$ Deasserted Hold Time | 0.0 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SD}$ | CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable | | 4.5 | ns |
| $t_{SE}$ | CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable | | 4.5 | ns |
| $t_{DBG}$ | CLKOUT High to $\overline{BG}$ Asserted Setup | | 3.6 | ns |
| $t_{EBG}$ | CLKOUT High to $\overline{BG}$ Deasserted Hold Time | | 3.6 | ns |
| $t_{DBH}$ | CLKOUT High to $\overline{BGH}$ Asserted Setup | | 3.6 | ns |
| $t_{EBH}$ | CLKOUT High to $\overline{BGH}$ Deasserted Hold Time | | 3.6 | ns |

[1] These timing parameters are based on worst-case operating conditions.
[2] The pad loads for these timing parameters are 20 pF.

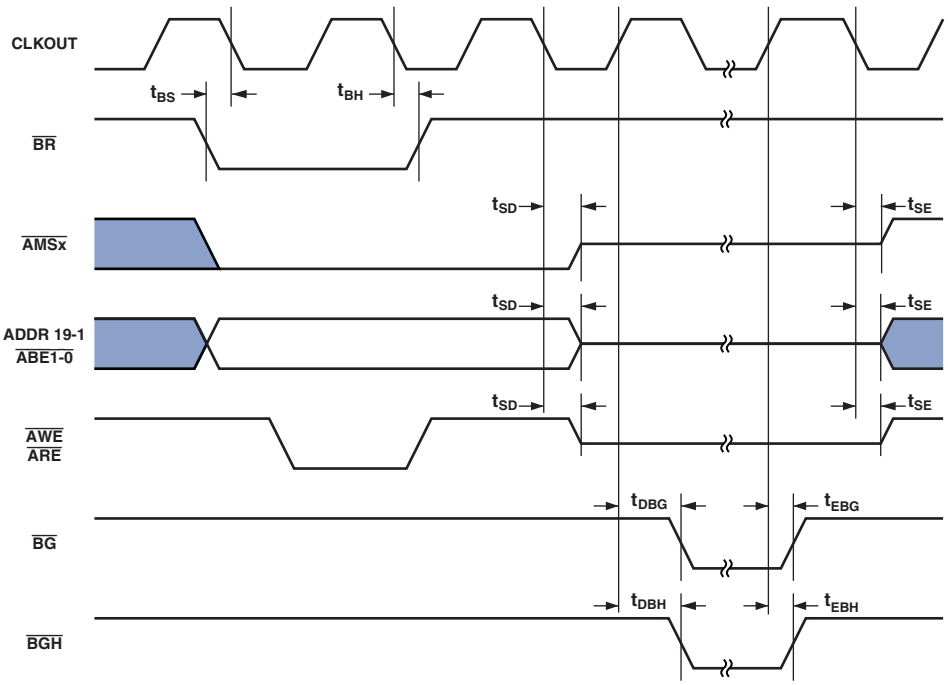



*Figure 13. External Port Bus Request and Grant Cycle Timing*

### *External DMA Request Timing*

Table 28 and Figure 15 describe the external DMA request operations.

**Table 28. External DMA Request Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DS}$ | DMARx Asserted to CLKOUT High Setup | 6.0 | | ns |
| $t_{DH}$ | CLKOUT High to DMARx Deasserted Hold Time | 0.0 | | ns |
| $t_{DMARACT}$ | DMARx Active Pulse Width | $1.0 \times t_{SCLK}$ | | ns |
| $t_{DMARINACT}$ | DMARx Inactive Pulse Width | $1.75 \times t_{SCLK}$ | | ns |

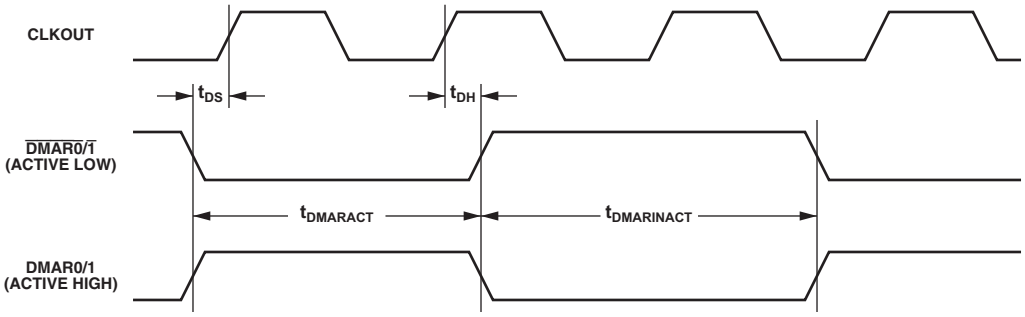



*Figure 15. External DMA Request Timing*

### *Serial Port Timing*

Table 30 through Table 33 on Page 41 and Figure 20 on Page 39 through Figure 23 on Page 41 describe serial port operations.

**Table 30. Serial Ports—External Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFSE}$ | TFSx/RFSx Setup Before TSCLKx/RSCLKx[1] | 3.0 | | ns |
| $t_{HFSE}$ | TFSx/RFSx Hold After TSCLKx/RSCLKx[1] | 3.0 | | ns |
| $t_{SDRE}$ | Receive Data Setup Before RSCLKx[1] | 3.0 | | ns |
| $t_{HDRE}$ | Receive Data Hold After RSCLKx[1] | 3.0 | | ns |
| $t_{SCLKEW}$ | TSCLKx/RSCLKx Width | 4.5 | | ns |
| $t_{SCLKE}$ | TSCLKx/RSCLKx Period | 15.0 | | ns |
| $t_{SUDTE}$ | Start-Up Delay From SPORT Enable To First External TFSx[2] | $4.0 \times t_{SCLKE}$ | | ns |
| $t_{SUDRE}$ | Start-Up Delay From SPORT Enable To First External RFSx[2] | $4.0 \times t_{SCLKE}$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFSE}$ | TFSx/RFSx Delay After TSCLKx/RSCLK (Internally Generated TFSx/RFSx)[3] | | 10.0 | ns |
| $t_{HOFSE}$ | TFSx/RFSx Hold After TSCLKx/RSCLK (Internally Generated TFSx/RFSx)[2] | 0 | | ns |
| $t_{DDTE}$ | Transmit Data Delay After TSCLKx[2] | | 10.0 | ns |
| $t_{HDTE}$ | Transmit Data Hold After TSCLKx[2] | 0 | | ns |

[1] Referenced to sample edge.
[2] Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.
[3] Referenced to drive edge.

**Table 31. Serial Ports—Internal Clock**

| Parameter | | $2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1] | | $2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3] | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| *Timing Requirements* | | | | | | |
| $t_{SFSI}$ | TFSx/RFSx Setup Before TSCLKx/RSCLKx[4] | 8.5 | | 8.0 | | ns |
| $t_{HFSI}$ | TFSx/RFSx Hold After TSCLKx/RSCLKx[4] | −1.5 | | −1.5 | | ns |
| $t_{SDRI}$ | Receive Data Setup Before RSCLKx[4] | 8.5 | | 8.0 | | ns |
| $t_{HDRI}$ | Receive Data Hold After RSCLKx[4] | −1.5 | | −1.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DFSI}$ | TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[5] | | 3.0 | | 3.0 | ns |
| $t_{HOFSI}$ | TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[5] | −1.0 | | −1.0 | | ns |
| $t_{DDTI}$ | Transmit Data Delay After TSCLKx[5] | | 3.0 | | 3.0 | ns |
| $t_{HDTI}$ | Transmit Data Hold After TSCLKx[5] | −1.0 | | −1.0 | | ns |
| $t_{SCLKIW}$ | TSCLKx/RSCLKx Width | 4.5 | | 4.5 | | ns |

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.
[4] Referenced to sample edge.
[5] Referenced to drive edge.

**Table 32. Serial Ports—Enable and Three-State**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DTENE}$ | Data Enable Delay from External TSCLKx[1] | 0 | | ns |
| $t_{DDTTE}$ | Data Disable Delay from External TSCLKx[1, 2] | | 10.0 | ns |
| $t_{DTENI}$ | Data Enable Delay from Internal TSCLKx[1] | –2.0 | | ns |
| $t_{DDTTI}$ | Data Disable Delay from Internal TSCLKx[1, 2] | | 3.0 | ns |

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only. TSCLKx is tied to RSCLKx.

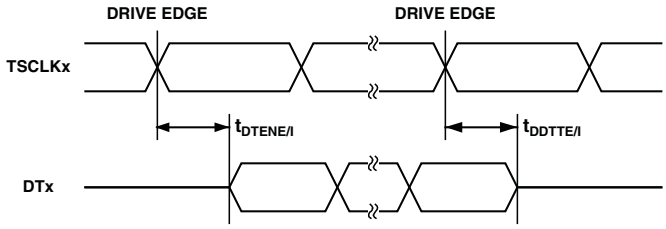



*Figure 22. Enable and Three-State*

**Table 33. External Late Frame Sync**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DDTLFSE}$ | Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1, 2] | | 10.0 | ns |
| $t_{DTENLFS}$ | Data Enable from Late FS or MCMEN = 1, MFD = 0[1, 2] | 0 | | ns |

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and $t_{DDTLFS}$.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

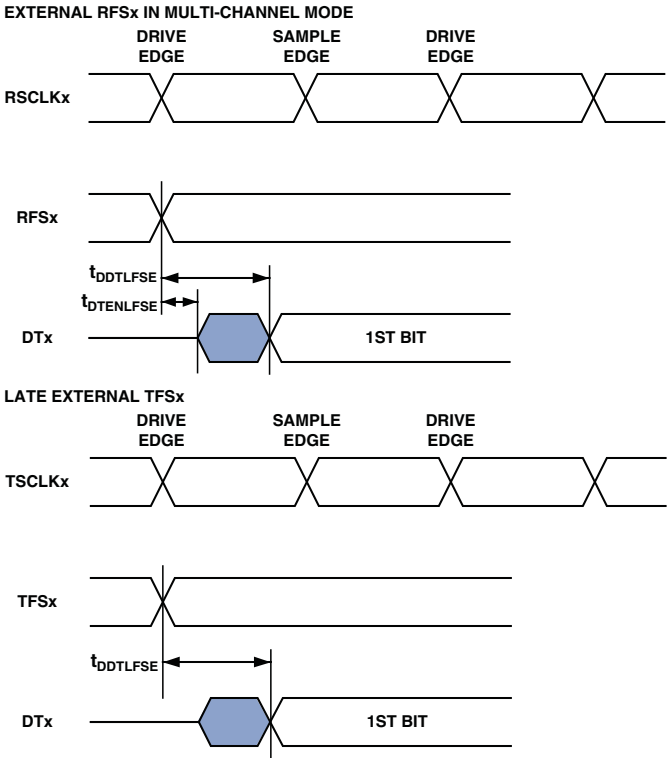



*Figure 23. External Late Frame Sync*

### *Serial Peripheral Interface Port—Master Timing*

Table 34 and Figure 24 describe SPI port master operations.

**Table 34. Serial Peripheral Interface (SPI) Port—Master Timing**

| Parameter | | $2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1] Min | Max | $2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3] Min | Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SSPIDM}$ | Data Input Valid to SCK Edge (Data Input Setup) | 8.7 | | 7.5 | | ns |
| $t_{HSPIDM}$ | SCK Sampling Edge to Data Input Invalid | −1.5 | | −1.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{SDSCIM}$ | $\overline{SPISEL}$x Low to First SCK Edge | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICHM}$ | Serial Clock High Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLM}$ | Serial Clock Low Period | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPICLK}$ | Serial Clock Period | $4 \times t_{SCLK} - 1.5$ | | $4 \times t_{SCLK} - 1.5$ | | ns |
| $t_{HDSM}$ | Last SCK Edge to $\overline{SPISEL}$x High | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{SPITDM}$ | Sequential Transfer Delay | $2 \times t_{SCLK} - 1.5$ | | $2 \times t_{SCLK} - 1.5$ | | ns |
| $t_{DDSPIDM}$ | SCK Edge to Data Out Valid (Data Out Delay) | | 6 | | 6 | ns |
| $t_{HDSPIDM}$ | SCK Edge to Data Out Invalid (Data Out Hold) | −1.0 | | −1.0 | | ns |

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.

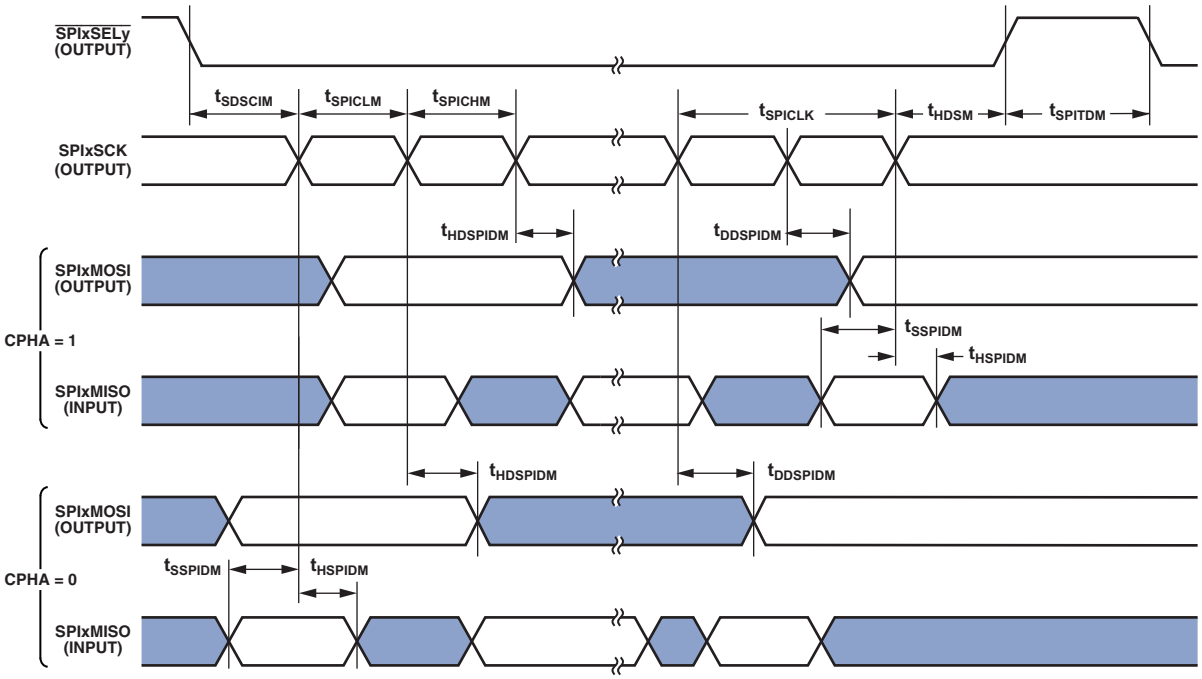



*Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing*

### General-Purpose Port Timing

Table 36 and Figure 26 describe general-purpose port operations.

**Table 36. General-Purpose Port Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{WFI}$ | General-Purpose Port Pin Input Pulse Width | $t_{SCLK}$ + 1 | | ns |
| *Switching Characteristic* | | | | |
| $t_{GPOD}$ | General-Purpose Port Pin Output Delay from CLKOUT Low | 0 | 6 | ns |

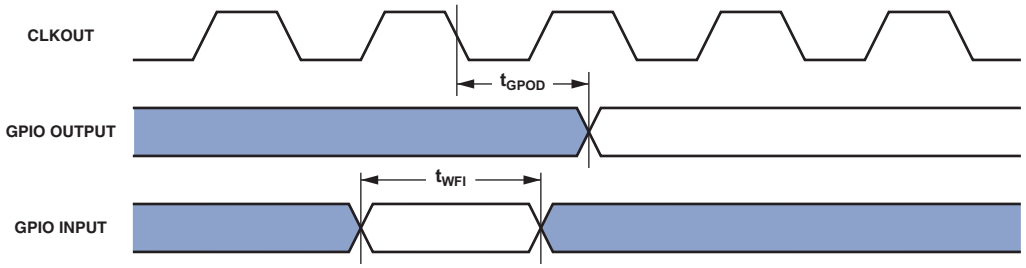



*Figure 26. General-Purpose Port Timing*

### Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF537 Blackfin Processor Hardware Reference*.

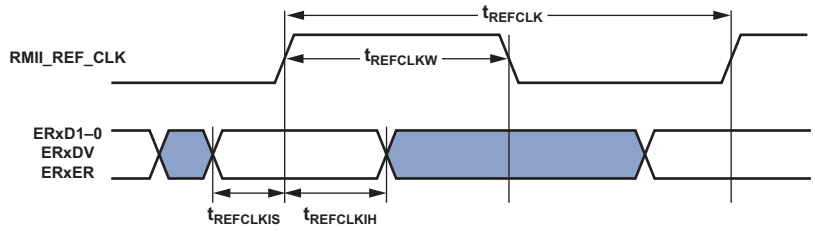



*Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal*

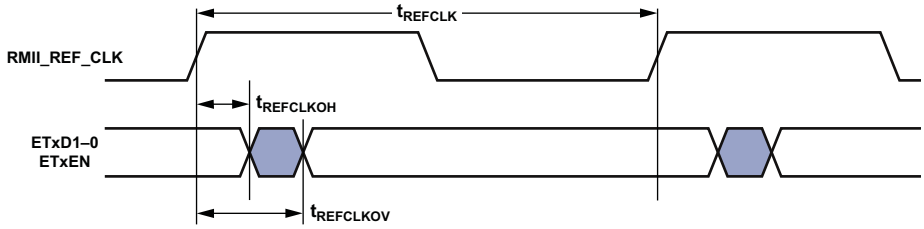



*Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal*

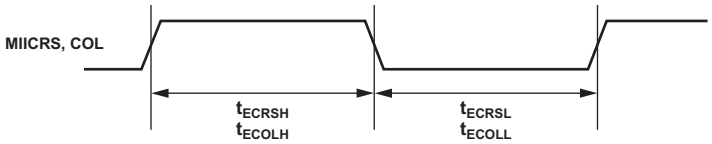



*Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal*

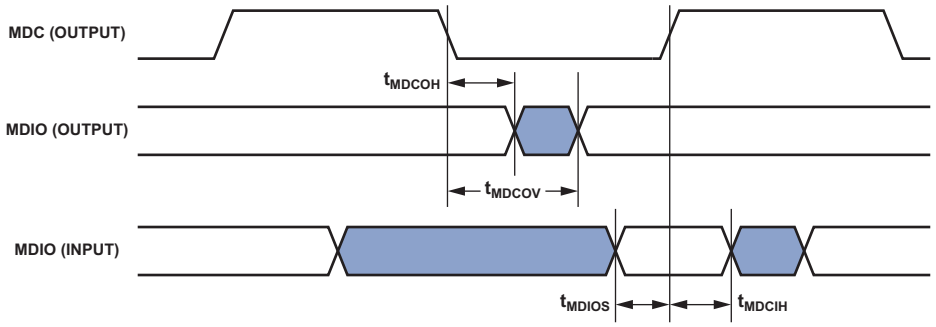



*Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management*

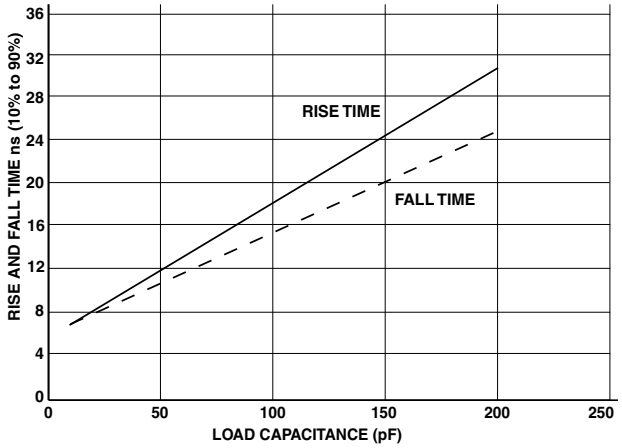



*Figure 59. Typical Output Delay or Hold for Driver E at $V_{DDEXT}$ Min*

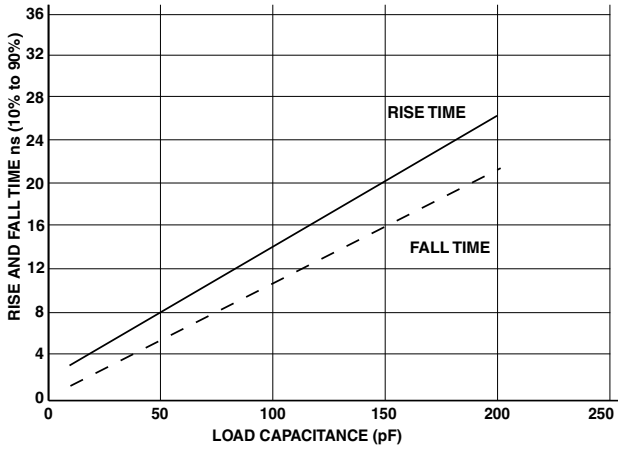



*Figure 60. Typical Output Delay or Hold for Driver E at $V_{DDEXT}$ Max*

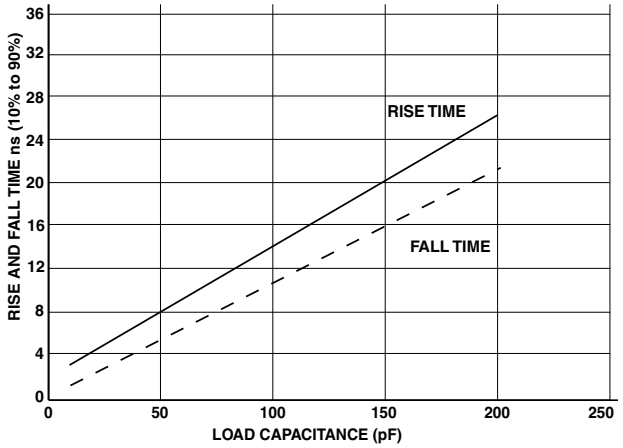



*Figure 61. Typical Output Delay or Hold for Driver F at $V_{DDEXT}$ Min*

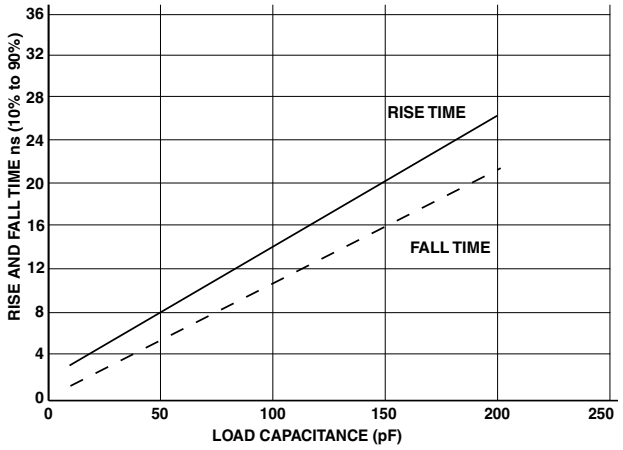



*Figure 62. Typical Output Delay or Hold for Driver F at $V_{DDEXT}$ Max*

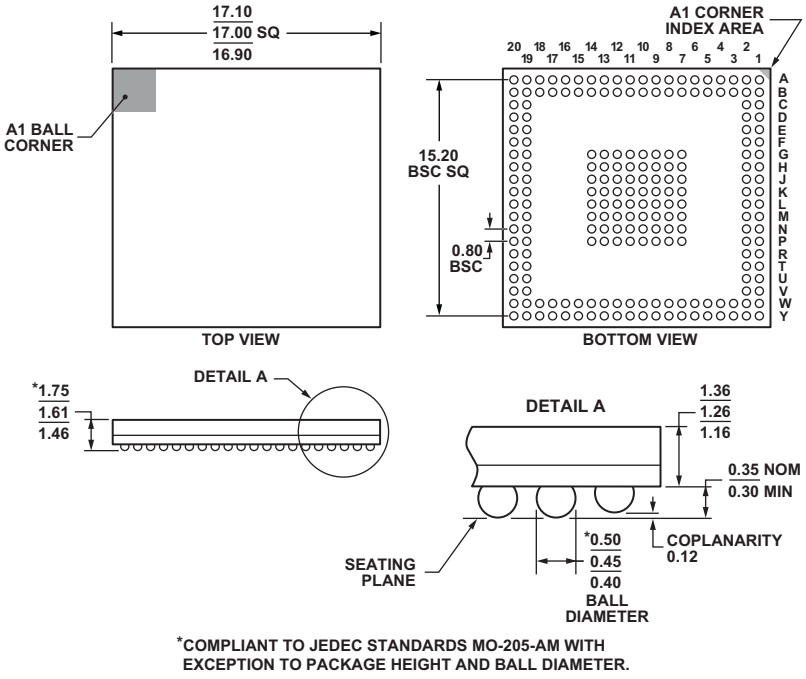



*Figure 68. 208-Ball Chip Scale Package Ball Grid Array [CSP_BGA]*
*(BC-208-2)*
*Dimensions shown in millimeters*

## AUTOMOTIVE PRODUCTS

The ADBF534W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 53 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 53. Automotive Products**

| Product Family[1,2] | Temperature Range[3] | Speed Grade (Max) | Package Description | Package Option |
|---|---|---|---|---|
| ADBF534WBBCZ4Axx | –40°C to +85°C | 400 MHz | 182-Ball CSP_BGA | BC-182 |
| ADBF534WBBCZ4Bxx | –40°C to +85°C | 400 MHz | 208-Ball CSP_BGA | BC-208-2 |
| ADBF534WYBCZ4Bxx | –40°C to +105°C | 400 MHz | 208-Ball CSP_BGA | BC-208-2 |

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature.