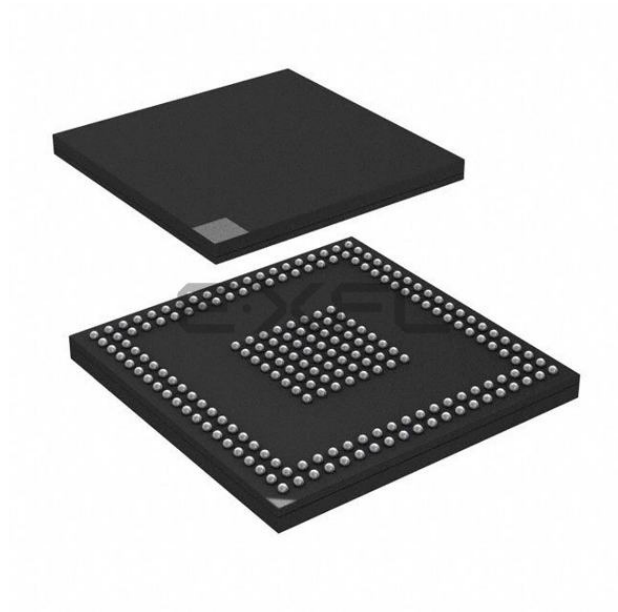

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf534bbcz-4b

GENERAL DESCRIPTION

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors are members of the Blackfin® family of products, incorporating the Analog Devices, Inc./Intel Micro Signal Architecture (MSA). Blackfin processors combine a dual-MAC, state-of-the-art signal processing engine, the advantages of a clean, orthogonal RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors are completely code and pin compatible. They differ only with respect to their performance, on-chip memory, and presence of the Ethernet MAC module. Specific performance, memory, and feature configurations are shown in Table 1.

Table 1. Processor Comparison

Features		ADSP-BF534	ADSP-BF536	ADSP-BF537
Ethernet MAC		—	1	1
CAN		1	1	1
TWI		1	1	1
SPORTs		2	2	2
UARTs		2	2	2
SPI		1	1	1
GP Timers		8	8	8
Watchdog Timers		1	1	1
RTC		1	1	1
Parallel Peripheral Interface		1	1	1
GPIOs		48	48	48
Memory Configuration	L1 Instruction SRAM/Cache	16K bytes	16K bytes	16K bytes
	L1 Instruction SRAM	48K bytes	48K bytes	48K bytes
	L1 Data SRAM/Cache	32K bytes	32K bytes	32K bytes
	L1 Data SRAM	32K bytes	—	32K bytes
	L1 Scratchpad	4K bytes	4K bytes	4K bytes
	L3 Boot ROM	2K bytes	2K bytes	2K bytes
Maximum Speed Grade		500 MHz	400 MHz	600 MHz
Package Options: CSP_BGA CSP_BGA		 208-Ball 182-Ball	 208-Ball 182-Ball	 208-Ball 182-Ball

By integrating a rich set of industry-leading system peripherals and memory, the Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

PORTABLE LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. They are produced with a low power and low voltage design methodology and feature on-chip dynamic power management, which is the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. This capability can result in a substantial reduction in power consumption, compared with just varying the frequency of operation. This allows longer battery life for portable appliances.

SYSTEM INTEGRATION

The Blackfin processor is a highly integrated system-on-a-chip solution for the next generation of embedded network-connected applications. By combining industry-standard interfaces with a high performance signal processing core, cost-effective applications can be developed quickly, without the need for costly external components. The system peripherals include an IEEE-compliant 802.3 10/100 Ethernet MAC (ADSP-BF536 and ADSP-BF537 only), a CAN 2.0B controller, a TWI controller, two UART ports, an SPI port, two serial ports (SPORTs), nine general-purpose 32-bit timers (eight with PWM capability), a real-time clock, a watchdog timer, and a parallel peripheral interface (PPI).

BLACKFIN PROCESSOR PERIPHERALS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1). The processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for the general-purpose I/O, CAN, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external SDRAM and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The Blackfin processors include an on-chip voltage regulator in support of the processors' dynamic power management capability. The voltage regulator provides a range of core voltage levels when supplied from V_{DDEXT}. The voltage regulator can be bypassed at the user's discretion.

Table 3. System Interrupt Controller (SIC) (Continued)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
DMA Channels 12 and 13 (Memory DMA Stream 0)	IVG13	29
DMA Channels 14 and 15 (Memory DMA Stream 1)	IVG13	30
Software Watchdog Timer	IVG13	31
Port F Interrupt B	IVG13	31

Event Control

The Blackfin processor provides a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC interrupt mask register (SIC_IMASK) – Controls the masking and unmasking of each peripheral interrupt event. When a bit is set in the register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wake-up enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. (For more information, see Dynamic Power Management on Page 13.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The Blackfin processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC (ADSP-BF536 and ADSP-BF537 only), SPORTs, SPI port, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

SERIAL PORTS (SPORTs)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide two full-duplex universal asynchronous receiver and transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UARTx\_Divisor}$$

where the 16-bit *UARTx_Divisor* comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant 8 bits).

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

1. Active video only mode
2. Vertical blanking only mode
3. Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide five operating modes, each with a different performance and power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode. Also, see Table 16, Table 15 and Table 17.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wake-up causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all of the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings. To preserve the processor state, prior to removing power, any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device.

Since V_{DDEXT} is still supplied in this state, all of the external pins three-state, unless otherwise specified. This allows other devices that are connected to the processor to still have power applied without drawing unwanted current.

The Ethernet or CAN modules can wake up the internal supply regulator. If the PH6 pin does not connect as the $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The regulator can also be woken up by a real-time clock wake-up event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wake-up events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables can be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register provides a means of waking from hibernate state without disrupting a self-refreshing SDRAM, provided that there is also an external pull-down on the SCKE pin.

Power Savings

As shown in Table 5, the processors support three different power domains which maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management, without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The dynamic power management feature allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in power dissipation, while reducing the voltage by 25% reduces power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

The power savings factor (PSF) is calculated as:

$$PSF = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as

$$\%\ power\ savings = (1 - PSF) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 23 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

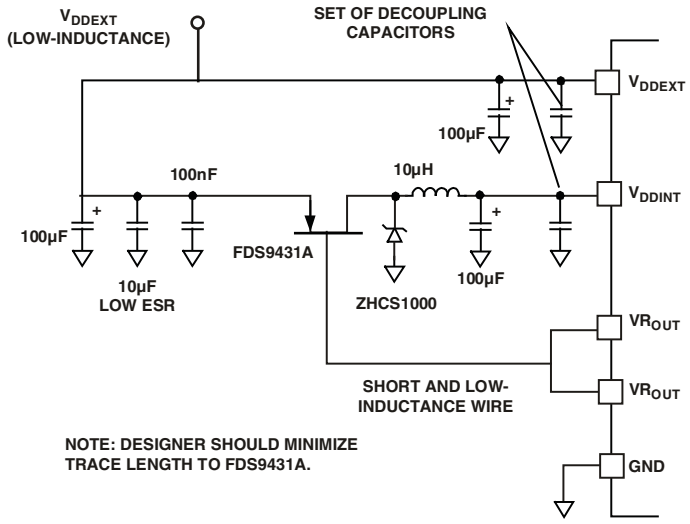

Figure 5. Voltage Regulator Circuit

Figure 5 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in

hibernate state, V_{DDEXT} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. The regulator can also be disabled and bypassed at the user's discretion. For additional information on voltage regulation, see *Switching Regulator Design Considerations for the ADSP-BF533 Blackfin Processors (EE-228)*.

CLOCK SIGNALS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 6. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 6 fine-tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations of multiple devices over temperature range.

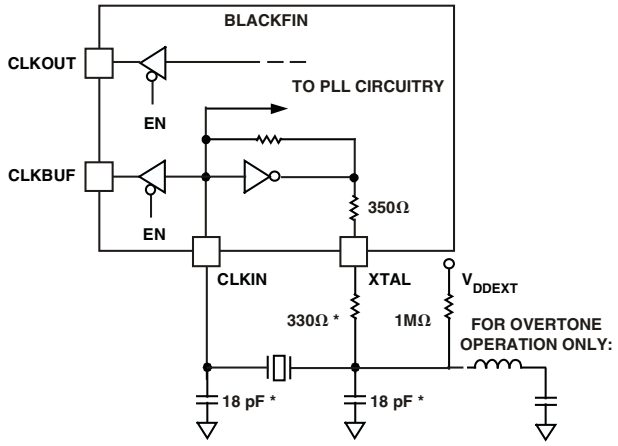

Figure 6. External Crystal Connections

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 6. A design procedure for third-overtone operation is discussed in detail in the application note *Using Third Overtone Crystals with the ADSP-218x DSP (EE-168)*.

The CLKBUF pin is an output pin, and is a buffer version of the input clock. This pin is particularly useful in Ethernet applications to limit the number of required clock sources in the system. In this type of application, a single 25 MHz or 50 MHz crystal can be applied directly to the processors. The 25 MHz or 50 MHz output of CLKBUF can then be connected to an external Ethernet MII or RMII PHY device.

Because of the default 10× PLL multiplier, providing a 50 MHz CLKIN exceeds the recommended operating conditions of the lower speed grades. Because of this restriction, an RMII PHY requiring a 50 MHz clock input cannot be clocked directly from the CLKBUF pin for the lower speed grades. In this case, either provide a separate 50 MHz clock source, or use an RMII PHY with 25 MHz clock input options. The CLKBUF output is active by default and can be disabled using the VR_CTL register for power savings.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 7, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence in the PLL_CTL register.

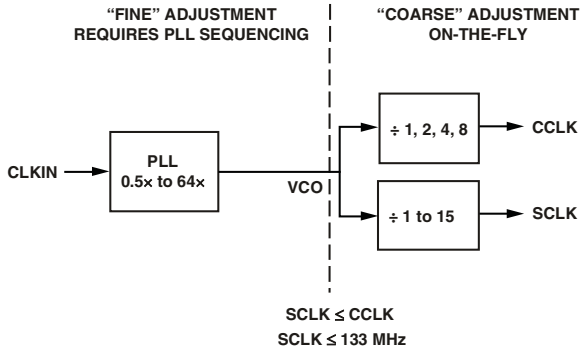

Figure 7. Frequency Modification Methods

On-the-fly CCLK and SCLK frequency changes can be effected by simply writing to the PLL_DIV register. Whereas the maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}, the VCO is always permitted to run up to the frequency specified by the part's speed grade. The CLKOUT pin reflects the SCLK frequency to the off-chip world. It belongs to the SDRAM interface, but it functions as a reference signal in other timing specifications as well. While active by default, it can be disabled using the EBIU_SDGCTL and EBIU_AMGCTL registers.

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 300 MHz, 400 MHz, and 500 MHz speed grade models[2]	0.8	1.2	1.32	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 600 MHz speed grade models[2]	0.8	1.3	1.43	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive grade models and +105°C nonautomotive grade models[2]	0.95	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Nonautomotive grade models[2]	2.25	2.5 or 3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models and +105°C nonautomotive grade models[2]	2.7	3.0 or 3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[3, 4]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.2			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[6]		$0.7 \times V_{DDEXT}$			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[7]	V_{DDEXT} = Maximum	2.0			V
V_{IL}	Low Level Input Voltage[3, 8]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[6]				$0.3 \times V_{DDEXT}$	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[7]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+120	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance. The required V_{DDINT} is a function of speed grade and operating frequency. See Table 10, Table 11, and Table 12 for details.

[2] See Ordering Guide on Page 67.

[3] Bidirectional pins (DATA15–0, PF15–0, PG15–0, PH15–0, TFS0, TSCLK0, RSCLK0, RFS0, MDIO) and input pins ($\overline{BR}$, ARDY, DR0PRI, DR0SEC, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF534/ADSP-BF536/ADSP-BF537 are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[4] Parameter value applies to all input and bidirectional pins except CLKIN, SDA, and SCL.

[5] Parameter value applies to CLKIN pin only.

[6] Applies to pins PJ2/SCL and PJ3/SDA which are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[7] Applies to pin PJ4/DR0SEC/CANRX/TACI0 which is 5.0 V tolerant (always accepts up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Parameter value applies to all input and bidirectional pins except SDA and SCL.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
V_{OH}[3]	High Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –2.0 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
I_{OH}[6]	High Level Output Current	V_{OH} = V_{DDEXT} – 0.5 V Min			–64			–64	mA
I_{OH}[7]		V_{OH} = V_{DDEXT} – 0.5 V Min			–144			–144	mA
V_{OL}[3]	Low Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA			0.5			0.5	V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OL} = 6 mA			0.5			0.5	V
V_{OL}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.5			0.5	V
I_{OL}[6]	Low Level Output Current	V_{OL} = 0.5 V Max			64			64	mA
I_{OL}[7]		V_{OL} = 0.5 V Max			144			144	mA
I_{IH}	High Level Input Current[8]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{IH5V}	High Level Input Current[9]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{IL}	Low Level Input Current[2]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA
I_{IHP}	High Level Input Current JTAG[10]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			50			50	µA
I_{OZH}	Three-State Leakage Current[11]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{OZH5V}	Three-State Leakage Current[12]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA

Parallel Peripheral Interface Timing

Table 29 and Figure 16 on Page 36, Figure 20 on Page 39, and Figure 23 on Page 41 describe parallel peripheral interface operations.

Table 29. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width[1]	6.0		ns
t_{PCLK}	PPI_CLK Period[1]	15.0		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK	6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

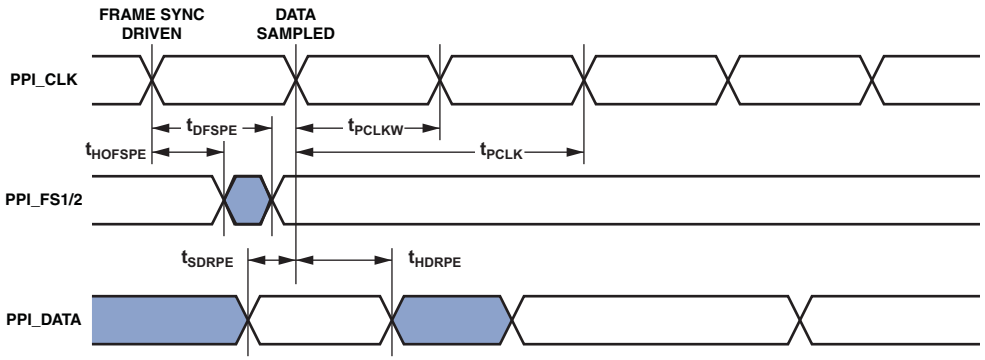

Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

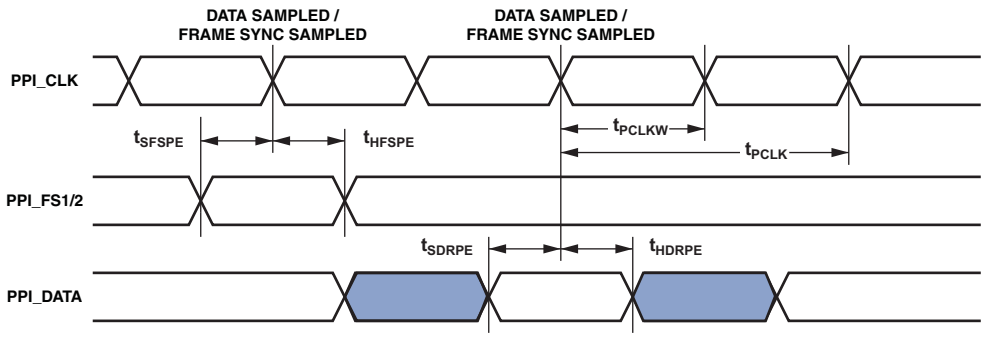

Figure 17. PPI GP Rx Mode with External Frame Sync Timing

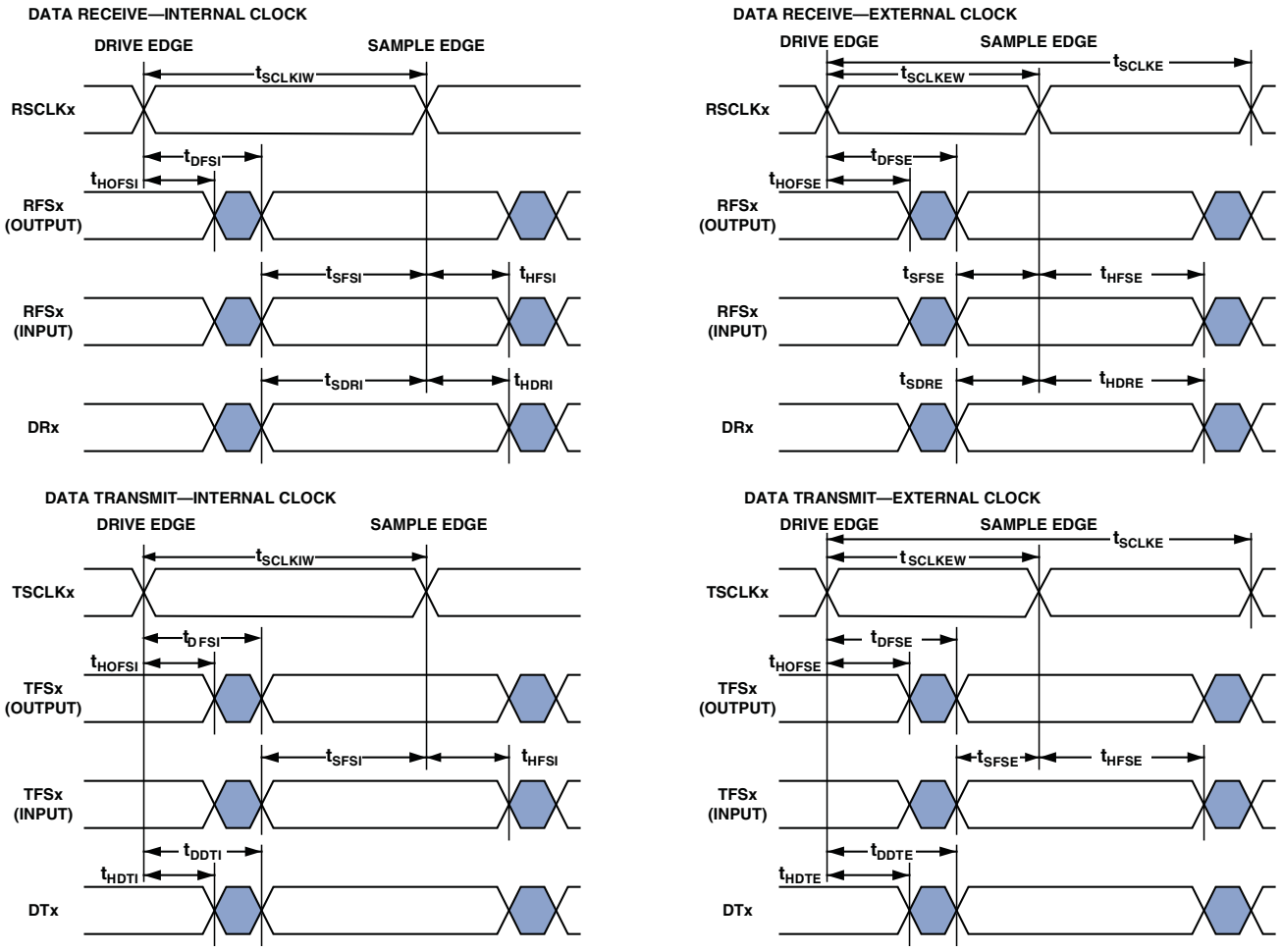

Figure 20. Serial Ports

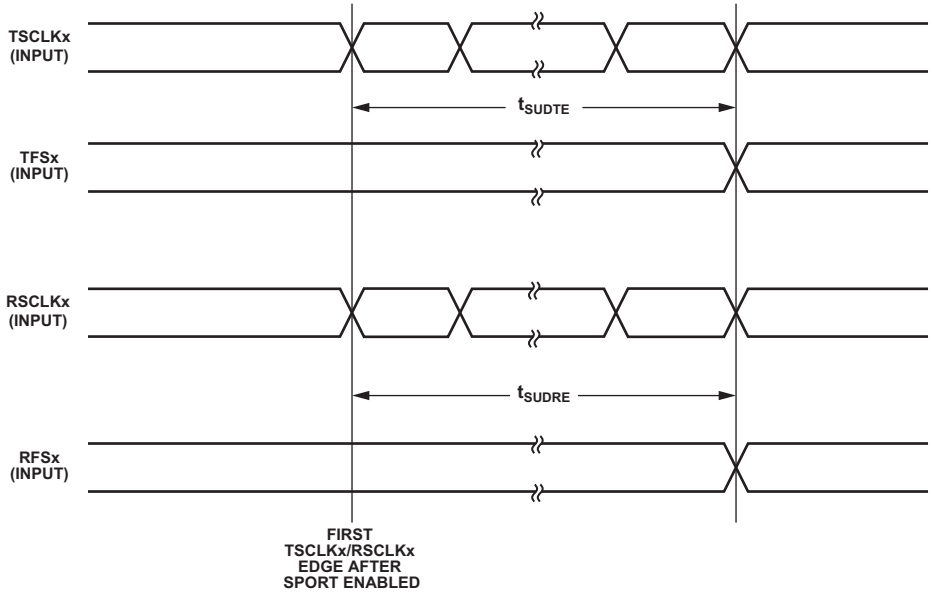

Figure 21. Serial Port Start Up with External Clock and Frame Sync

Table 32. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2]		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only. TSCLKx is tied to RSCLKx.

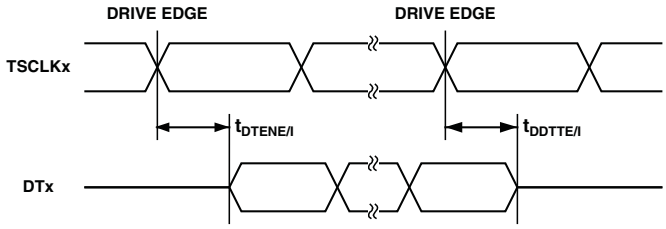

Figure 22. Enable and Three-State

Table 33. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or MCMEN = 1, MFD = 0[1, 2]	0		ns

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and t_{DDTLFS}.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

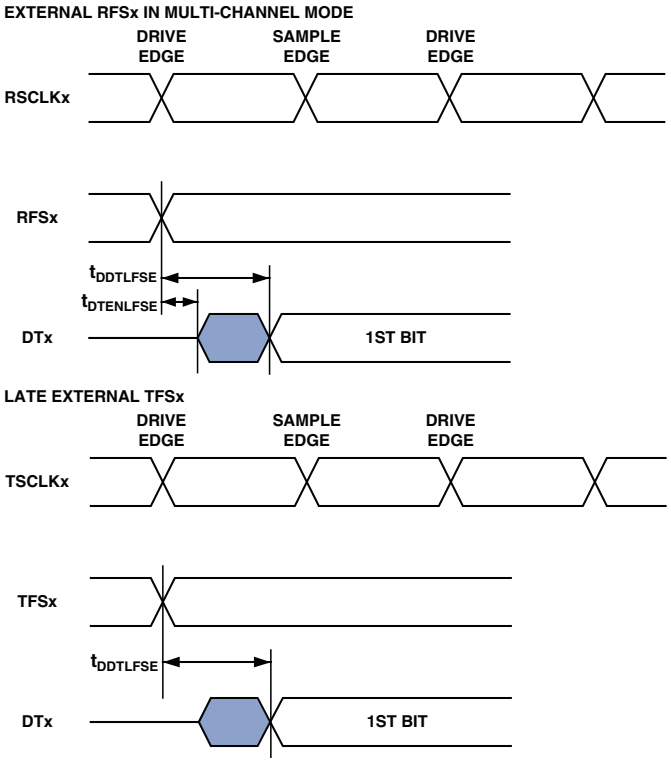

Figure 23. External Late Frame Sync

Serial Peripheral Interface Port—Master Timing

Table 34 and Figure 24 describe SPI port master operations.

Table 34. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		$2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1] Min	Max	$2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3] Min	Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	8.7		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	−1.5		−1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISEL}$x Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISEL}$x High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	−1.0		−1.0		ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.

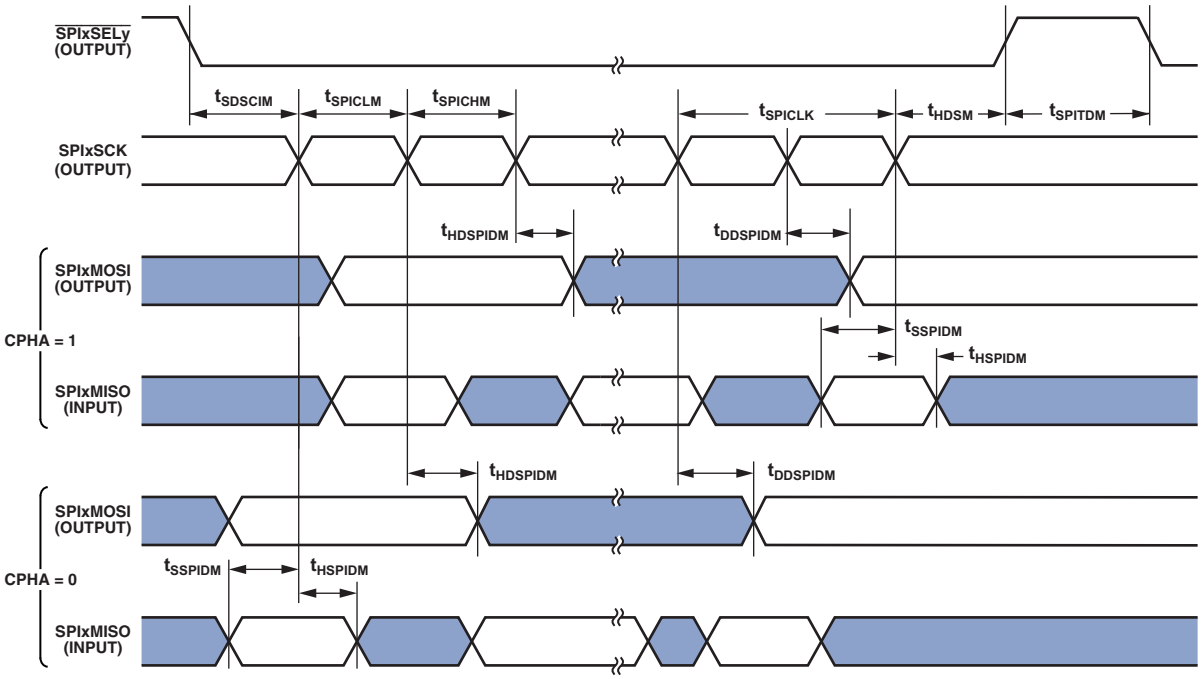

Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

General-Purpose Port Timing

Table 36 and Figure 26 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	0	6	ns

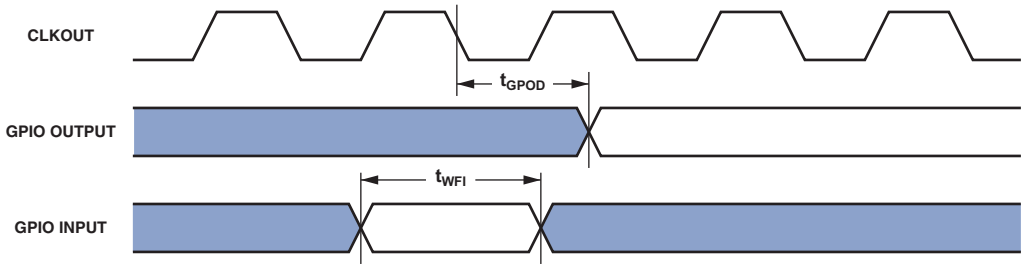

Figure 26. General-Purpose Port Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF537 Blackfin Processor Hardware Reference*.

Table 44. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 45. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	10		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	10		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

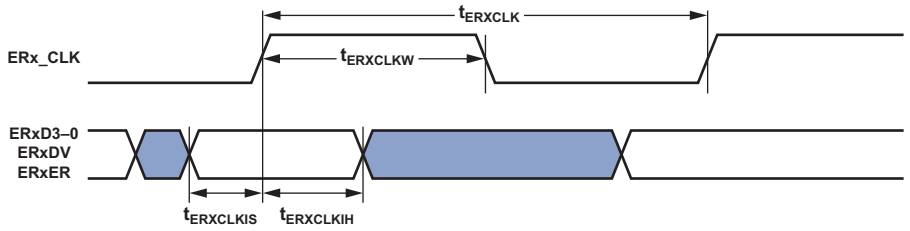

Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

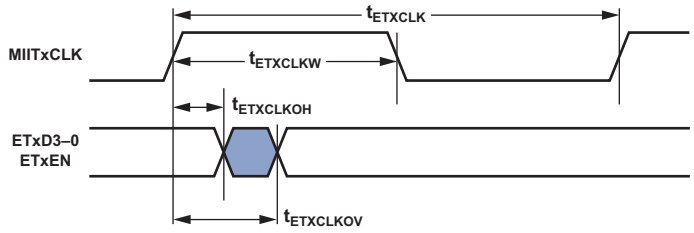

Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

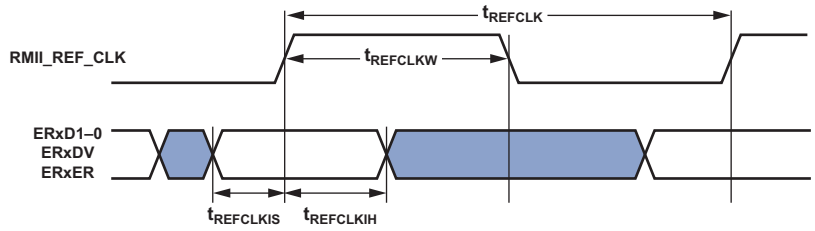

Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

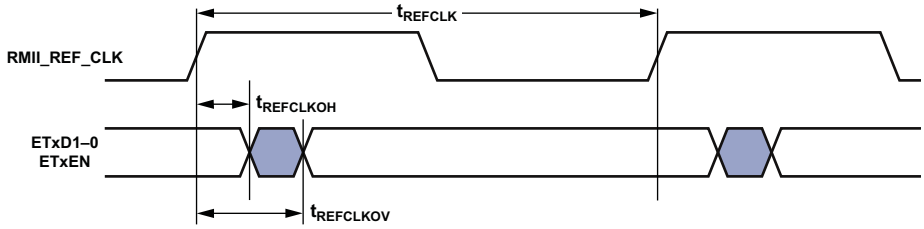

Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

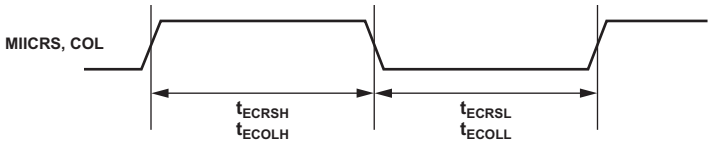

Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

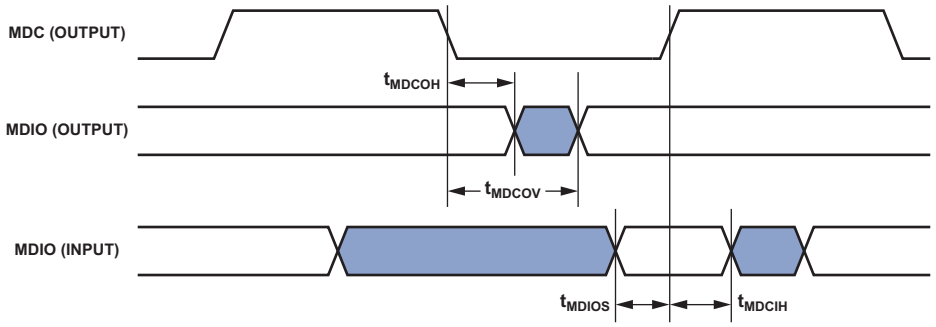

Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management

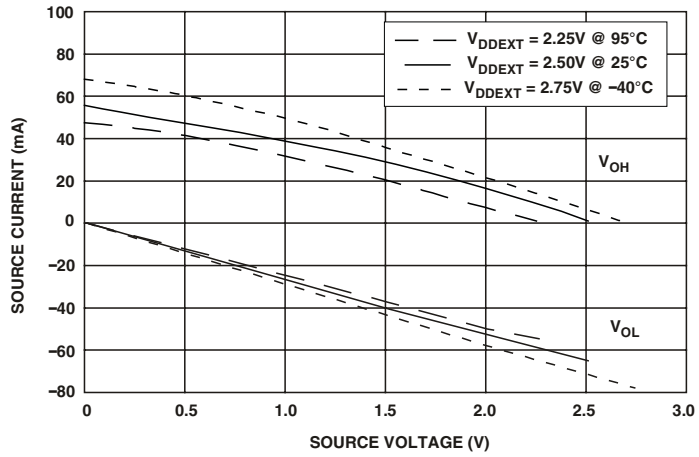

Figure 42. Drive Current D (Low V_{DDEXT})

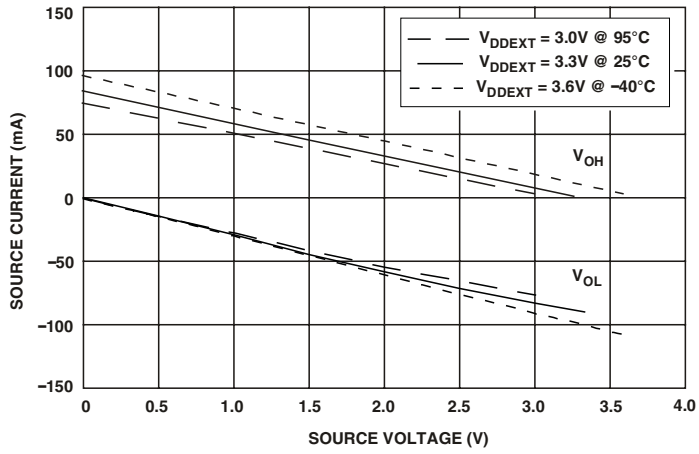

Figure 43. Drive Current D (High V_{DDEXT})

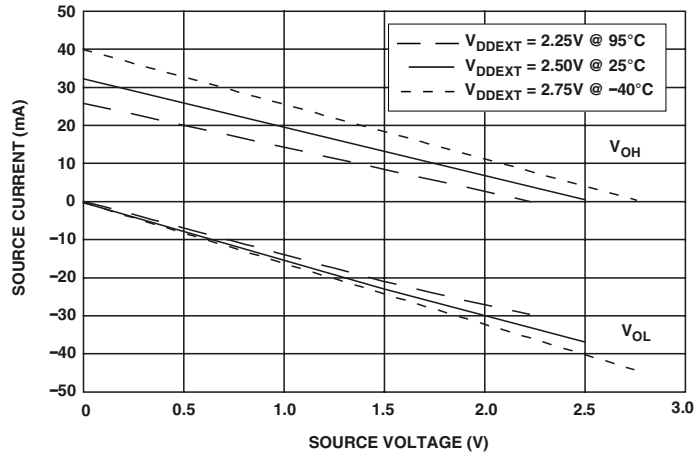

Figure 44. Drive Current E (Low V_{DDEXT})

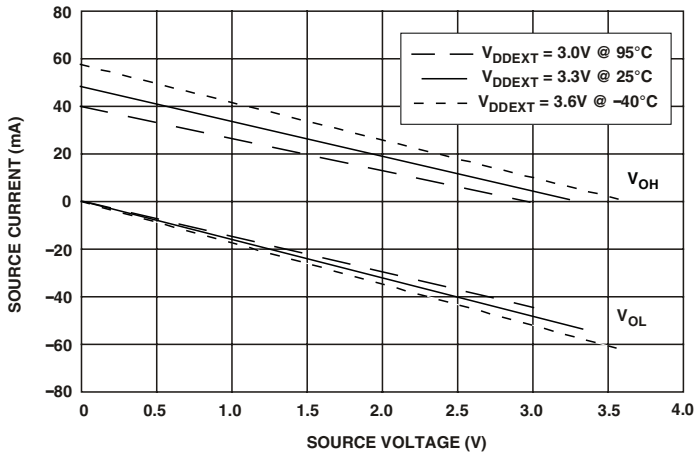

Figure 45. Drive Current E (High V_{DDEXT})

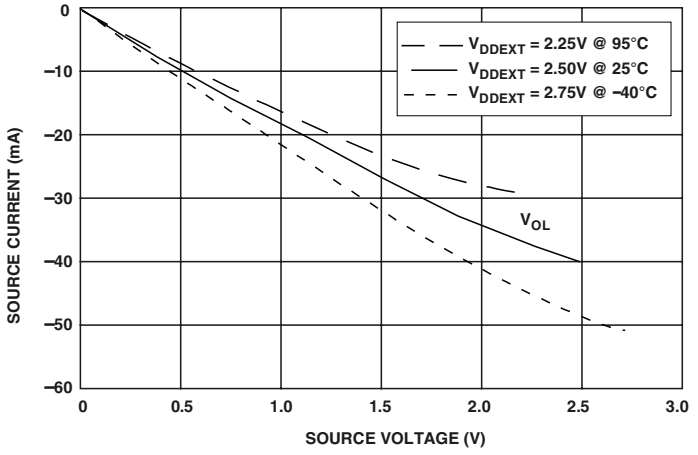

Figure 46. Drive Current F (Low V_{DDEXT})

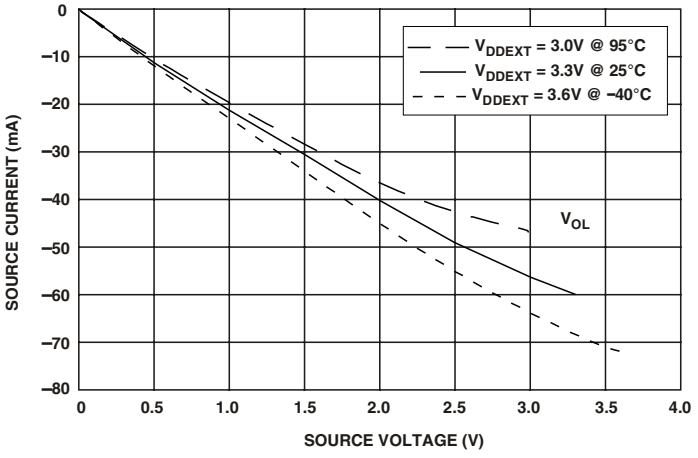

Figure 47. Drive Current F (High V_{DDEXT})

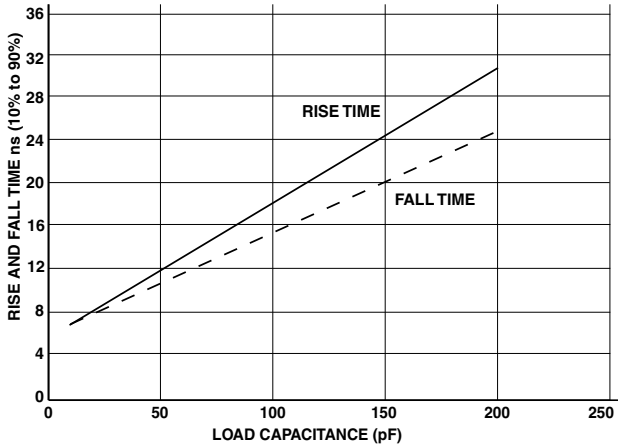

Figure 59. Typical Output Delay or Hold for Driver E at V_{DDEXT} Min

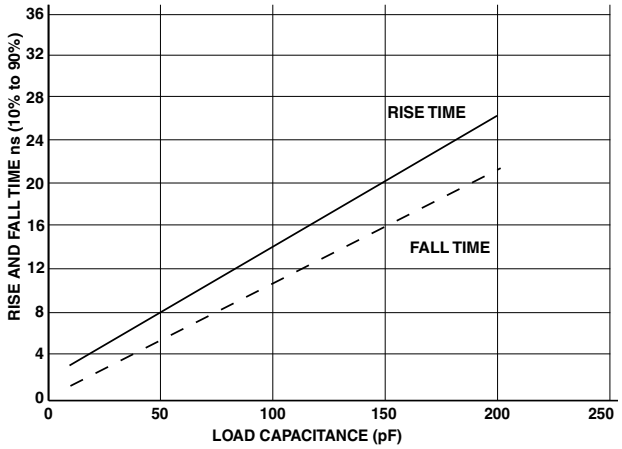

Figure 60. Typical Output Delay or Hold for Driver E at V_{DDEXT} Max

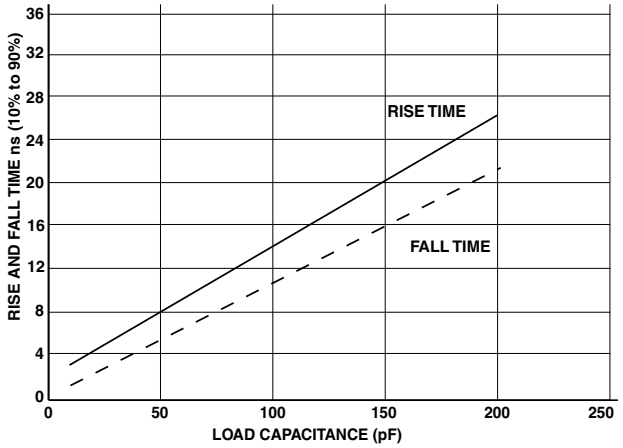

Figure 61. Typical Output Delay or Hold for Driver F at V_{DDEXT} Min

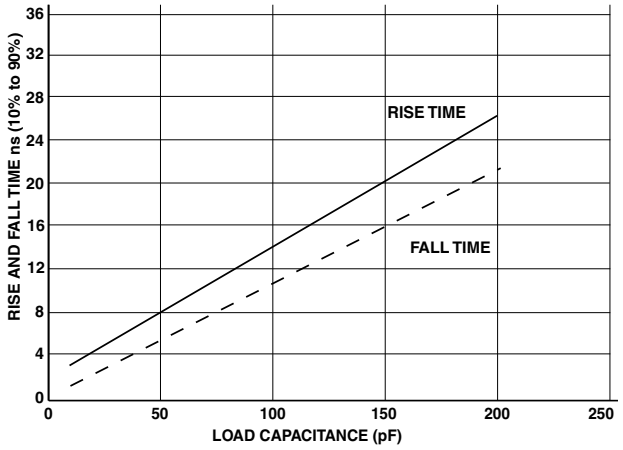

Figure 62. Typical Output Delay or Hold for Driver F at V_{DDEXT} Max

Table 50. 182-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	V_{DDEXT}	C10	$\overline{RESET}$	F5	GND	J14	ADDR1	M9	DATA0
A2	PH11	C11	PJ3	F6	GND	K1	PF5	M10	GND
A3	PH12	C12	V_{DDEXT}	F10	GND	K2	PF6	M11	ADDR15
A4	PH13	C13	$\overline{SMS}$	F11	GND	K3	PF7	M12	ADDR9
A5	PH14	C14	$\overline{SCAS}$	F12	V_{DDEXT}	K4	PF8	M13	ADDR10
A6	PH15	D1	PG10	F13	$\overline{AMS2}$	K5	V_{DDINT}	M14	ADDR11
A7	CLKBUF	D2	PG11	F14	$\overline{AMS1}$	K6	GND	N1	$\overline{TRST}$
A8	RTXO	D3	PG12	G1	PG0	K7	V_{DDEXT}	N2	TMS
A9	RTXI	D4	GND	G2	PG1	K8	V_{DDINT}	N3	TDO
A10	GND	D5	PG13	G3	PG2	K9	V_{DDEXT}	N4	BMODE0
A11	XTAL	D6	PG14	G4	GND	K10	V_{DDINT}	N5	DATA13
A12	CLKIN	D7	PJ4	G5	GND	K11	GND	N6	DATA10
A13	VROUT0	D8	PJ5	G10	V_{DDINT}	K12	ADDR7	N7	DATA7
A14	GND	D9	PJ8	G11	GND	K13	ADDR5	N8	DATA4
B1	PH5	D10	PJ10	G12	$\overline{AMS3}$	K14	ADDR2	N9	DATA1
B2	PH6	D11	PJ11	G13	$\overline{AOE}$	L1	PF1	N10	$\overline{BGH}$
B3	PH7	D12	$\overline{SWE}$	G14	$\overline{ARE}$	L2	PF2	N11	ADDR16
B4	PH8	D13	$\overline{SRAS}$	H1	PF12	L3	PF3	N12	ADDR14
B5	PH9	D14	$\overline{BR}$	H2	PF13	L4	PF4	N13	ADDR13
B6	PH10	E1	PG6	H3	PF14	L5	BMODE2	N14	ADDR12
B7	PJ1	E2	PG7	H4	PF15	L6	GND	P1	V_{DDEXT}
B8	PJ7	E3	PG8	H5	V_{DDEXT}	L7	V_{DDEXT}	P2	TCK
B9	V_{DDRTC}	E4	PG9	H10	V_{DDEXT}	L8	GND	P3	BMODE1
B10	$\overline{NMI}$	E5	V_{DDINT}	H11	GND	L9	V_{DDEXT}	P4	DATA15
B11	PJ2	E6	V_{DDEXT}	H12	$\overline{ABE1}$	L10	GND	P5	DATA14
B12	VROUT1	E7	GND	H13	$\overline{ABE0}$	L11	V_{DDEXT}	P6	DATA11
B13	SCKE	E8	V_{DDINT}	H14	$\overline{AWE}$	L12	ADDR8	P7	DATA8
B14	CLKOUT	E9	GND	J1	PF9	L13	ADDR6	P8	DATA5
C1	PG15	E10	V_{DDINT}	J2	PF10	L14	ADDR3	P9	DATA2
C2	PH0	E11	V_{DDEXT}	J3	PF11	M1	PF0	P10	$\overline{BG}$
C3	PH1	E12	SA10	J4	GND	M2	$\overline{EMU}$	P11	ADDR19
C4	PH2	E13	ARDY	J5	GND	M3	TDI	P12	ADDR18
C5	PH3	E14	$\overline{AMS0}$	J9	GND	M4	GND	P13	ADDR17
C6	PH4	F1	PG3	J10	GND	M5	DATA12	P14	GND
C7	PJ0	F2	PG4	J11	V_{DDEXT}	M6	DATA9		
C8	PJ6	F3	PG5	J12	V_{DDEXT}	M7	DATA6		
C9	PJ9	F4	V_{DDEXT}	J13	ADDR4	M8	DATA3		

Figure 63 shows the top view of the CSP_BGA ball configuration. Figure 64 shows the bottom view of the CSP_BGA ball configuration.

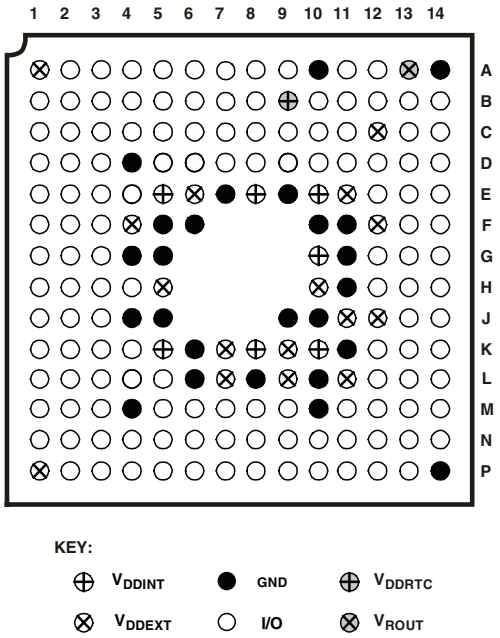

Figure 63. 182-Ball CSP_BGA Configuration (Top View)

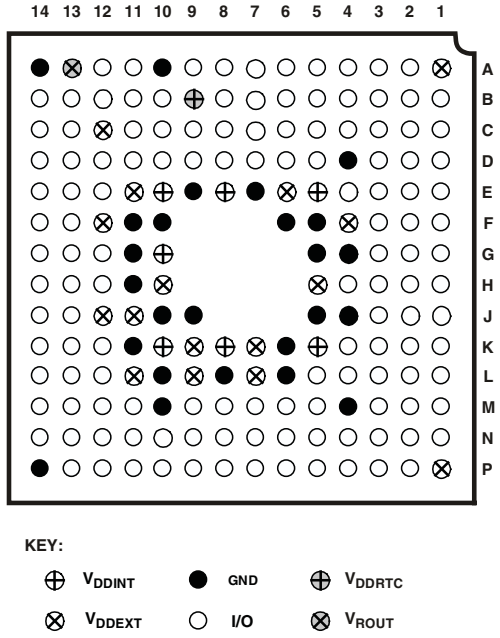

Figure 64. 182-Ball CSP_BGA Configuration (Bottom View)