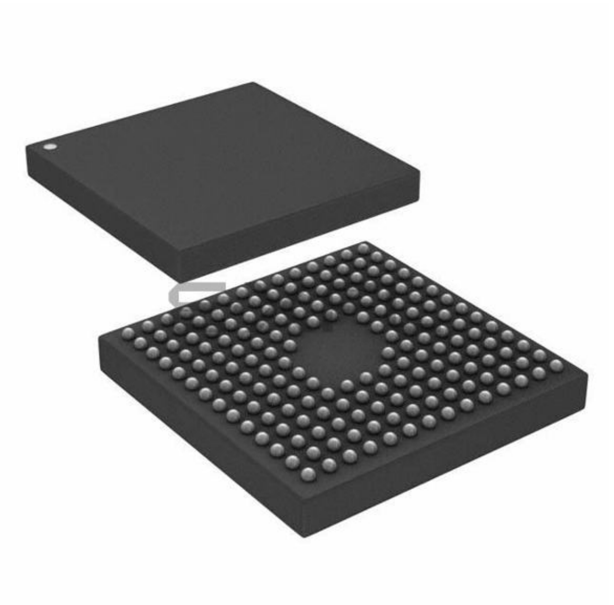

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.26V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	182-LFBGA, CSPBGA
Supplier Device Package	182-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf534bbcz-5a

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates, and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

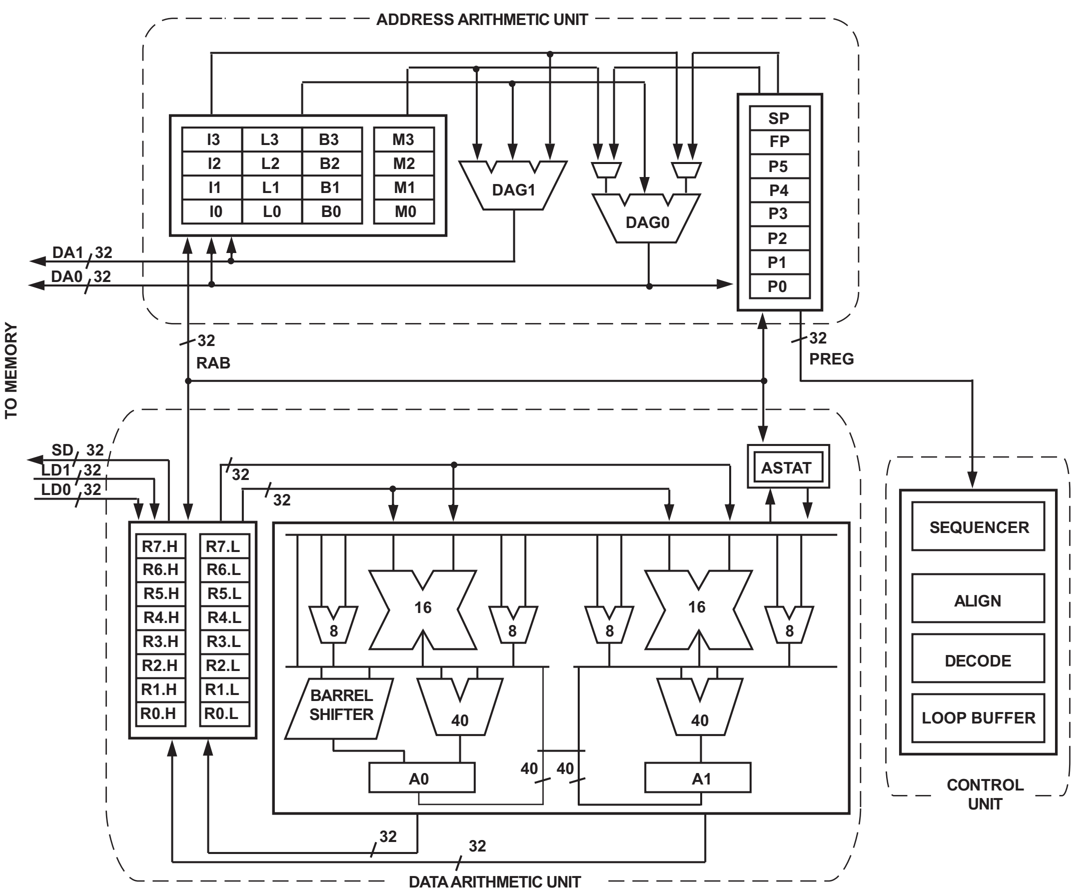


Figure 2. Blackfin Processor Core

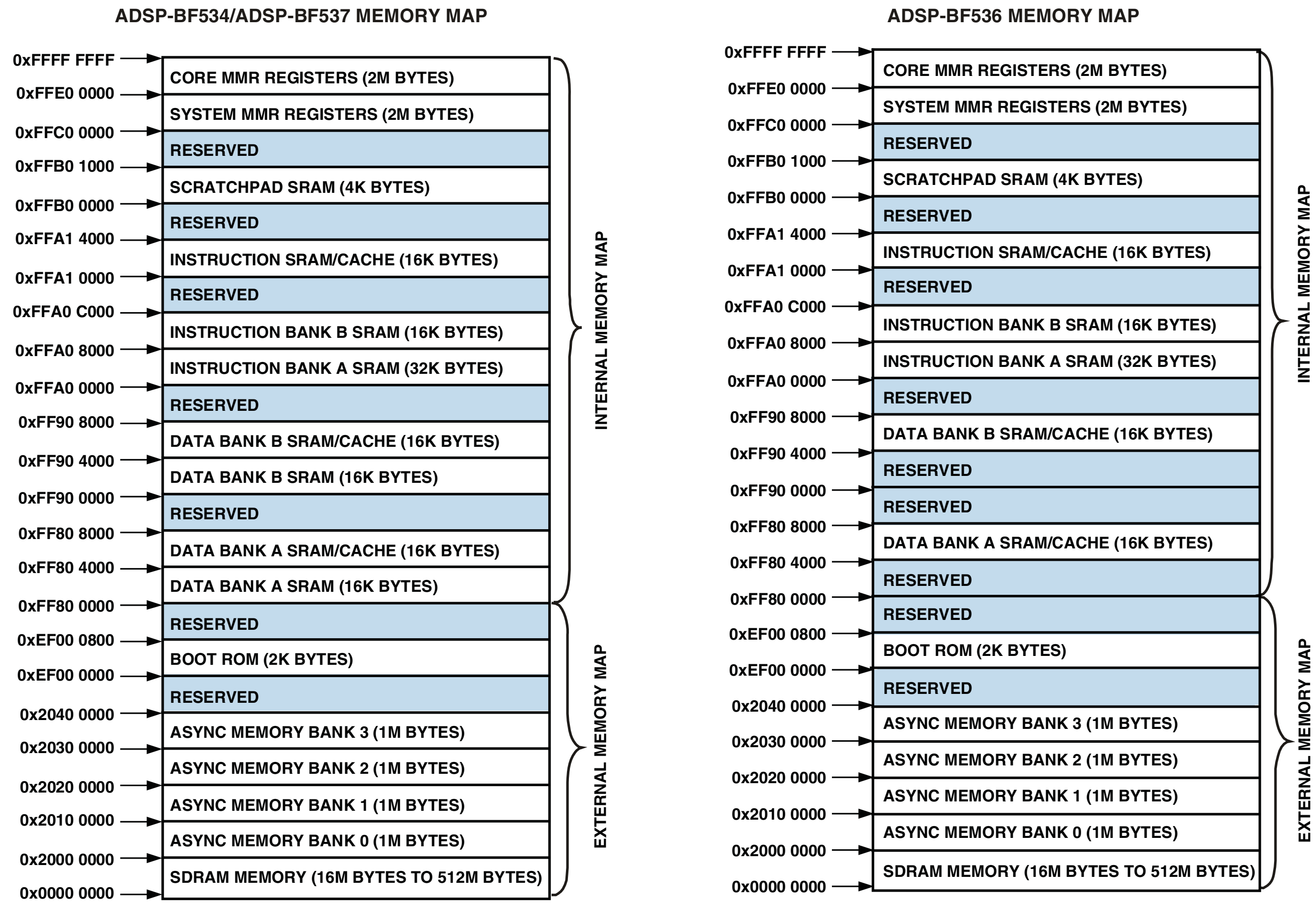


Figure 3. ADSP-BF534/ADSP-BF536/ADSP-BF537 Memory Maps

memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 16.

Event Handling

The event controller on the Blackfin processor handles all asynchronous and synchronous events to the processor. The Blackfin processor provides event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher priority event takes precedence over servicing of a lower priority event. The controller provides support for five different types of events:

- Emulation – An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset – This event resets the processor.
- Nonmaskable Interrupt (NMI) – The NMI event can be generated by the software watchdog timer or by the $\overline{\text{NMI}}$ input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shutdown of the system.
- Exceptions – Events that occur synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts – Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The Blackfin processor event controller consists of two stages: the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC, and are then routed directly into the general-purpose interrupts of the CEC.

Table 3. System Interrupt Controller (SIC) (Continued)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
DMA Channels 12 and 13 (Memory DMA Stream 0)	IVG13	29
DMA Channels 14 and 15 (Memory DMA Stream 1)	IVG13	30
Software Watchdog Timer	IVG13	31
Port F Interrupt B	IVG13	31

Event Control

The Blackfin processor provides a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 32 bits wide:

- CEC interrupt latch register (ILAT) – Indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it can be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK) – Controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register can be read or written while in supervisor mode. (Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.)
- CEC interrupt pending register (IPEND) – The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates the event is currently active or nested at some level. This register is updated automatically by the controller but can be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in Table 3 on Page 7.

- SIC interrupt mask register (SIC_IMASK) – Controls the masking and unmasking of each peripheral interrupt event. When a bit is set in the register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status register (SIC_ISR) – As multiple peripherals can be mapped to a single event, this register allows the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wake-up enable register (SIC_IWR) – By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled when the event is generated. (For more information, see Dynamic Power Management on Page 13.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected (detection requires two core clock cycles). The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

The Blackfin processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the processor's internal memories and any of its DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including the SDRAM controller and the asynchronous memory controller. DMA-capable peripherals include the Ethernet MAC (ADSP-BF536 and ADSP-BF537 only), SPORTs, SPI port, UARTs, and PPI. Each individual DMA-capable peripheral has at least one dedicated DMA channel.

The DMA controller supports both one-dimensional (1-D) and two-dimensional (2-D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2-D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the DMA controller include

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1-D or 2-D DMA using a linked list of descriptors
- 2-D DMA using an array of descriptors, specifying only the base DMA address within a common page.

SERIAL PORTS (SPORTs)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide two full-duplex universal asynchronous receiver and transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UARTx\_Divisor}$$

where the 16-bit *UARTx_Divisor* comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant 8 bits).

- Programmable Rx address filters, including a 64-bit address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames.
- Advanced power management supporting unattended transfer of Rx and Tx frames and status to/from external memory via DMA during low power sleep mode.
- System wake-up from sleep operating mode upon magic packet or any of four user-definable wake-up frame filters.
- Support for 802.3Q tagged VLAN frames.
- Programmable MDC clock rate and preamble suppression.
- In RMII operation, 7 unused pins can be configured as GPIO pins for other purposes.

PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors group the many peripheral signals to four ports—Port F, Port G, Port H, and Port J. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Eight of the pins (Port F7–0) offer high source/high sink current capabilities.

General-Purpose I/O (GPIO)

The processors have 48 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Port J does not provide GPIO functionality. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output or input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processors employ a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode – Frame syncs and data are inputs into the PPI.
2. Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

1. Active video only mode
2. Vertical blanking only mode
3. Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide five operating modes, each with a different performance and power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode. Also, see Table 16, Table 15 and Table 17.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wake-up causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all of the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings. To preserve the processor state, prior to removing power, any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device.

Since V_{DDEXT} is still supplied in this state, all of the external pins three-state, unless otherwise specified. This allows other devices that are connected to the processor to still have power applied without drawing unwanted current.

The Ethernet or CAN modules can wake up the internal supply regulator. If the PH6 pin does not connect as the $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The regulator can also be woken up by a real-time clock wake-up event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wake-up events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables can be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register provides a means of waking from hibernate state without disrupting a self-refreshing SDRAM, provided that there is also an external pull-down on the SCKE pin.

Power Savings

As shown in Table 5, the processors support three different power domains which maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management, without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The dynamic power management feature allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in power dissipation, while reducing the voltage by 25% reduces power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

The power savings factor (PSF) is calculated as:

$$PSF = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as

$$\%\ power\ savings = (1 - PSF) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 23 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

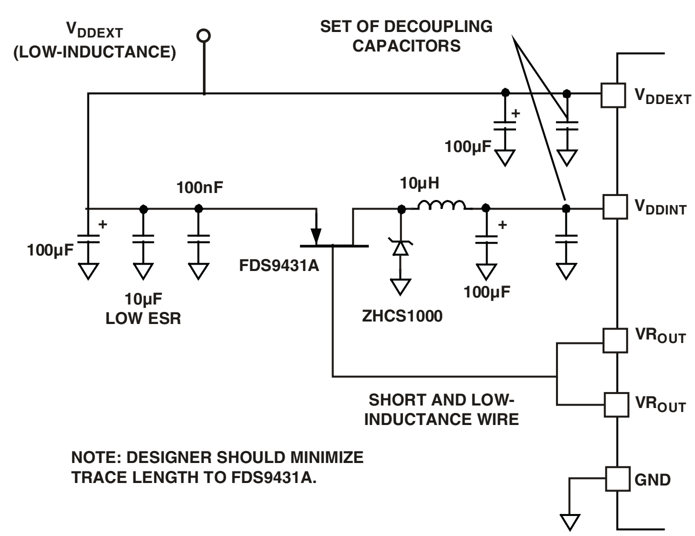


Figure 5. Voltage Regulator Circuit

Figure 5 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF534/ADSP-BF536/ADSP-BF537 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started with Blackfin Processors*
- *ADSP-BF537 Blackfin Processor Hardware Reference*
- *ADSP-BF53x/ADSP-BF56x Blackfin Processor Programming Reference*
- *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN DESCRIPTIONS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors pin definitions are listed in Table 9. In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics. Pins shown with an asterisk after their name (*) offer high source/high sink current capabilities.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. If $\overline{\text{BR}}$ is active (whether or not $\overline{\text{RESET}}$ is asserted), the memory pins are also three-stated. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

All I/O pins have their input buffers disabled with the exception of the pins noted in the data sheet that need pull-ups or pull-downs if unused.

The SDA (serial data) and SCL (serial clock) pins are open drain and therefore require a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{\text{ABE1–0}}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{\text{BR}}$	I	Bus Request (This pin should be pulled high when not used.)	
$\overline{\text{BG}}$	O	Bus Grant	A
$\overline{\text{BGH}}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{\text{AMS3–0}}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{\text{AOE}}$	O	Output Enable	A
$\overline{\text{ARE}}$	O	Read Enable	A
$\overline{\text{AWE}}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{\text{SRAS}}$	O	Row Address Strobe	A
$\overline{\text{SCAS}}$	O	Column Address Strobe	A
$\overline{\text{SWE}}$	O	Write Enable	A
SCKE	O	Clock Enable(Requires a pull-down if hibernate with SDRAM self-refresh is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{\text{SMS}}$	O	Bank Select	A

Table 10 through Table 12 describe the voltage/frequency requirements for the ADSP-BF534/ADSP-BF536/ADSP-BF537 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 13 describes phase-locked loop operating conditions.

Table 10. Core Clock Requirements—500 MHz, 533 MHz, and 600 MHz Speed Grades[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.30 V Minimum)[2]	1.30 V	600	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.20 V Minimum)[3]	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] See Ordering Guide on Page 67.
[2] Applies to 600 MHz models only. See Ordering Guide on Page 67.
[3] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 67.

Table 11. Core Clock Requirements—400 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	120°C ≥ T_J > 105°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	363	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 67.
[2] See Operating Conditions on Page 23.

Table 12. Core Clock Requirements—300 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	300	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	255	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	210	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	180	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	160	MHz

[1] See Ordering Guide on Page 67.

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 14. System Clock Requirements

Parameter	Condition	Max	Unit
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, $V_{DDINT} \geq 1.14$ V	133[2]	MHz
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, $V_{DDINT} < 1.14$ V	100	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 27 on Page 34.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 27 on Page 34.

System designers should refer to *Estimating Power for the ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-297. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 18).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 17).

Table 15. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})													
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
–40	3.9	4.7	6.8	8.2	9.9	12.0	14.6	17.3	20.3	24.1	27.1	28.6	36.3	44.4
0	17.0	19.2	21.9	25.0	28.2	32.1	36.9	41.8	47.7	53.8	61.0	63.8	73.2	84.1
25	35.0	39.2	44.3	50.8	56.1	63.3	69.1	76.4	84.7	93.5	104.5	109.1	123.4	138.8
40	53.0	59.2	65.3	71.9	79.1	88.0	96.6	108.0	120.0	130.7	142.6	148.5	166.5	185.6
55	76.7	84.6	93.6	103.1	113.7	123.9	136.3	148.3	162.8	178.4	194.4	201.4	223.7	247.5
70	110.1	120.0	130.9	142.2	156.5	171.3	185.2	201.7	220.6	239.7	259.8	268.8	295.9	325.2
85	150.1	164.5	178.7	193.2	210.4	228.9	247.7	268.8	291.4	314.1	341.1	351.2	384.6	420.3
100	202.3	219.2	236.5	255.8	277.8	299.8	323.8	351.2	378.8	407.5	440.4	453.4	494.3	538.2
105	223.8	241.4	260.4	282.0	303.4	328.7	354.5	381.7	410.8	443.6	477.8	492.2	535.1	581.5

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Static Current–300 MHz and 400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})											
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–40	2.6	3.2	3.7	4.5	5.5	6.6	7.9	9.3	10.5	12.5	13.9	14.8
0	6.6	7.8	8.4	9.9	10.9	12.3	13.8	15.5	17.5	19.6	21.7	23.1
25	12.2	13.5	14.8	16.4	18.2	19.9	22.7	25.6	28.4	31.8	35.7	37.2
40	17.2	19.0	20.6	22.9	25.9	28.2	31.6	34.9	38.9	42.9	47.6	49.5
55	25.7	27.8	30.9	33.7	37.3	41.4	44.8	50.0	54.8	59.4	66.1	68.4
70	37.6	41.3	44.8	48.9	53.9	58.6	63.9	69.7	76.9	84.0	92.2	94.9
85	53.7	58.3	63.7	69.0	75.9	82.9	90.5	98.4	106.4	115.3	124.6	128.1
100	75.1	82.3	88.5	95.8	104.0	112.5	121.8	130.6	141.3	153.2	164.8	169.7
105	84.5	91.2	98.2	106.0	114.2	123.0	132.4	143.3	155.0	167.4	179.8	185.4
115[2]	103.8	111.8	120.3	127.6	138.0	148.5	159.6	171.4	184.6	198.8	213.4	219.6
120[2]	115.5	123.6	132.2	141.9	152.3	163.7	175.6	189.3	202.8	217.7	232.3	238.6

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Applies to automotive grade models only.

TIMING SPECIFICATIONS

Component specifications are subject to change without notice.

Clock and Reset Timing

Table 22. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	8.0		ns
t_{CKINH}	CLKIN High Pulse	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{RESET}$ Asserted Pulse Width Low	$11 \times t_{CKIN}$		ns
t_{NOBOOT}	$\overline{RESET}$ Deassertion to First External Access Delay[5]	$3 \times t_{CKIN}$	$5 \times t_{CKIN}$	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 14. Since by default the PLL is multiplying the CLKIN frequency by 10 MHz, 300 MHz, and 400 MHz speed grade parts can not use the full CLKIN period range.
[2] Applies to PLL bypass mode and PLL non bypass mode.
[3] CLKIN frequency must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

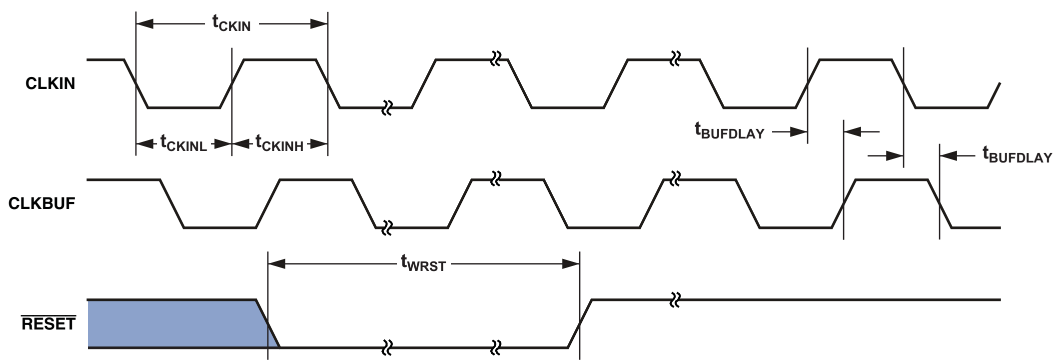
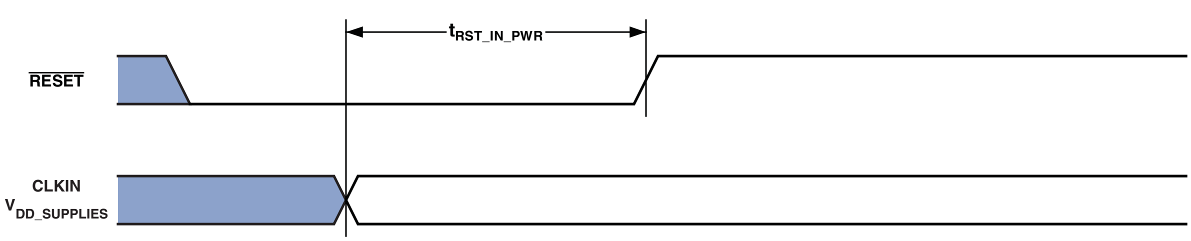


Figure 9. Clock and Reset Timing

Table 23. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{RESET}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



In Figure 10, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 10. Power-Up Reset Timing

Asynchronous Memory Read Cycle Timing

Table 24. Asynchronous Memory Read Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	2.1		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT [1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{ARE}$.

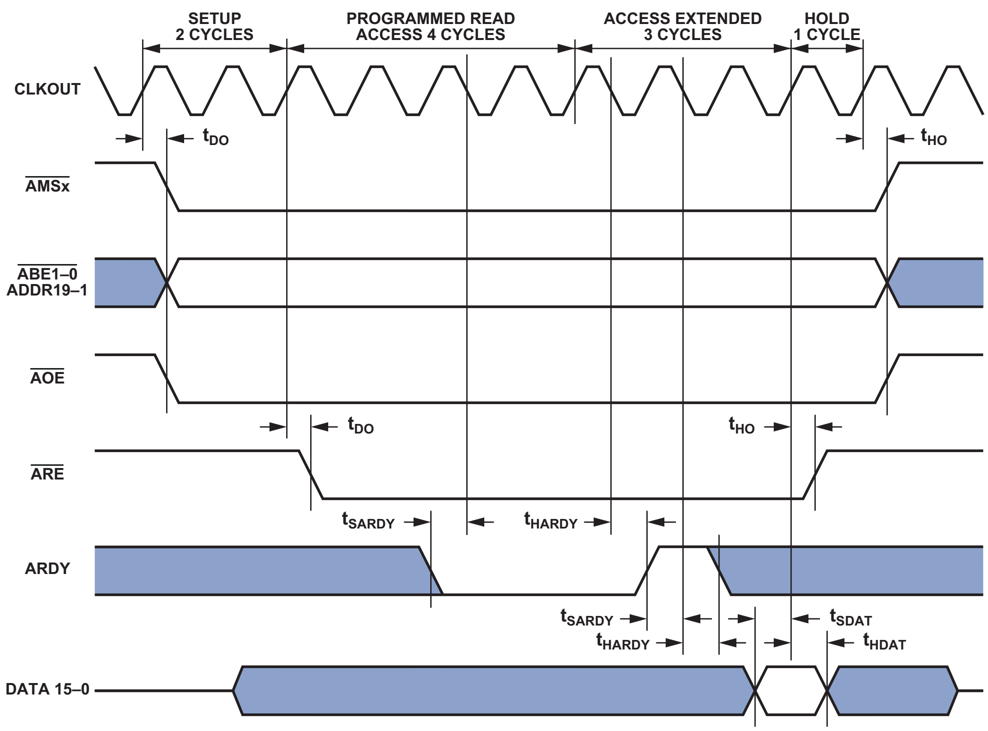


Figure 11. Asynchronous Memory Read Cycle Timing

SDRAM Interface Timing

Table 27. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA15–0 Setup Before CLKOUT	1.5		ns
t_{HSDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{DCAD}	COMMAND[1], ADDR19–1, DATA15–0 Delay After CLKOUT		4.0	ns
t_{HCAD}	COMMAND[1], ADDR19–1, DATA15–0 Hold After CLKOUT	1.0		ns
t_{DSDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENSDAT}	DATA15–0 Enable After CLKOUT	0.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J \leq +105°C$	7.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J > +105°C$	10		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.

[2] These limits are specific to the SDRAM interface only. In addition, CLKOUT must always comply with the limits in Table 14 on Page 24.

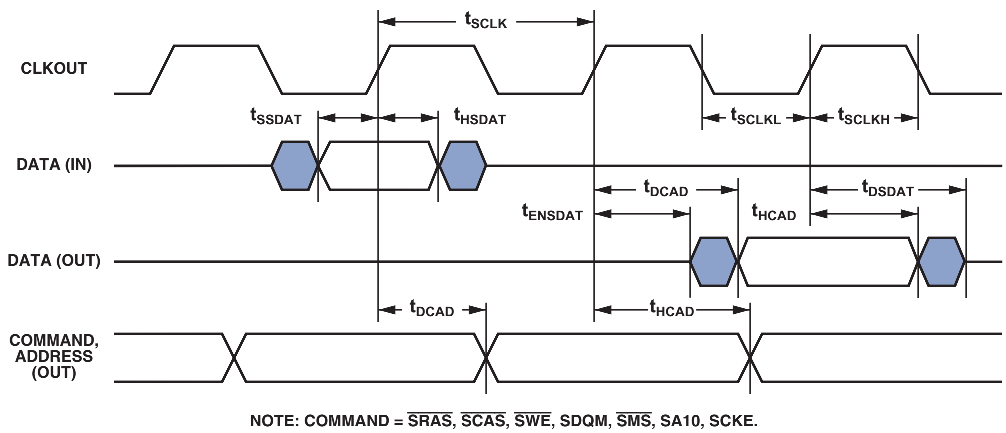


Figure 14. SDRAM Interface Timing

External DMA Request Timing

Table 28 and Figure 15 describe the external DMA request operations.

Table 28. External DMA Request Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{DS}	DMARx Asserted to CLKOUT High Setup	6.0		ns
t_{DH}	CLKOUT High to DMARx Deasserted Hold Time	0.0		ns
$t_{DMARACT}$	DMARx Active Pulse Width	$1.0 \times t_{SCLK}$		ns
$t_{DMARINACT}$	DMARx Inactive Pulse Width	$1.75 \times t_{SCLK}$		ns

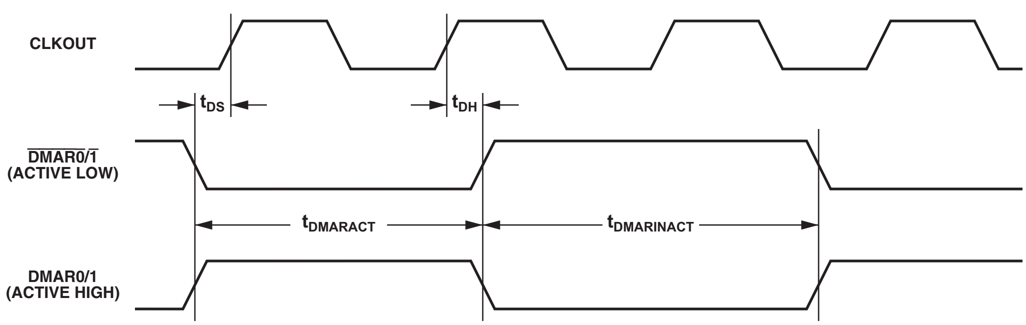


Figure 15. External DMA Request Timing

Table 33. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1,2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or MCMEN = 1, MFD = 0[1,2]	0		ns

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and t_{DDTLFS}.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

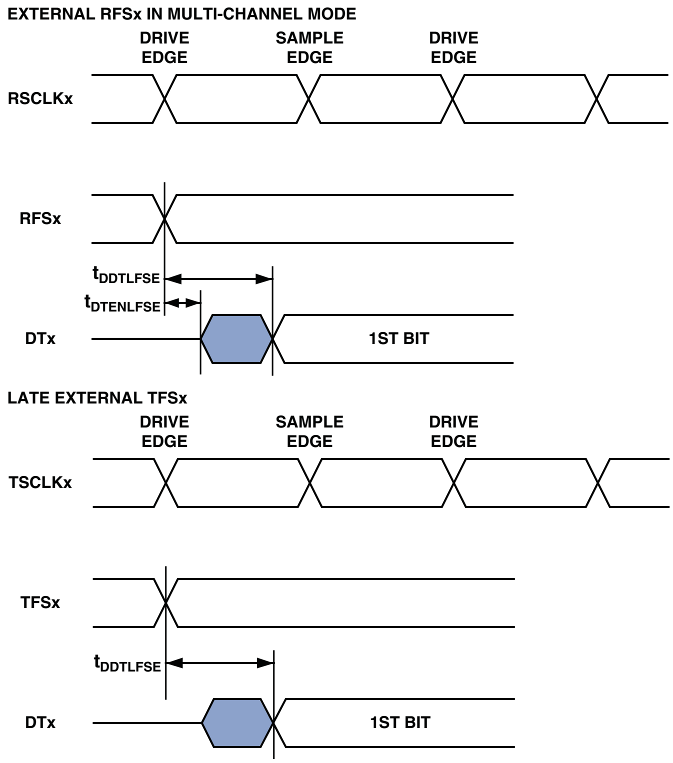


Figure 23. External Late Frame Sync

Timer Clock Timing

Table 37 and Figure 27 describe timer clock timing.

Table 37. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

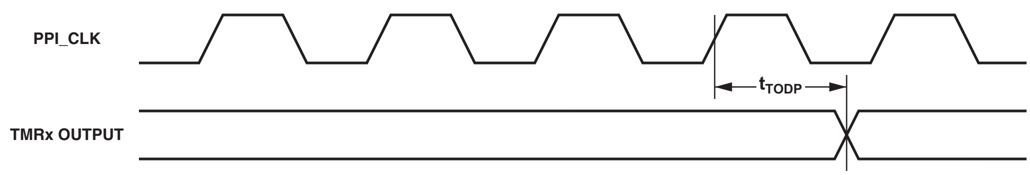


Figure 27. Timer Clock Timing

Timer Cycle Timing

Table 38 and Figure 28 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 38. Timer Cycle Timing

Parameter		$2.25\text{ V} \le V_{DDEXT} < 2.70\text{ V}$ or $0.80\text{ V} \le V_{DDINT} < 0.95\text{ V}$[1] Min	Max	$2.70\text{ V} \le V_{DDEXT} \le 3.60\text{ V}$ and $0.95\text{ V} \le V_{DDINT} \le 1.43\text{ V}$[2, 3] Min	Max	Unit
Timing Characteristics						
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[4]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[4]	$1 \times t_{SCLK}$		$1 \times t_{SCLK}$		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[5]	5.5		5.0		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[5]	1.5		1.5		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	$1 \times t_{SCLK}$	$(2^{32}-1) \times t_{SCLK}$	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		6.5		6.0	ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.
[4] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PF15 or PPI_CLK signals in PWM output mode.
[5] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

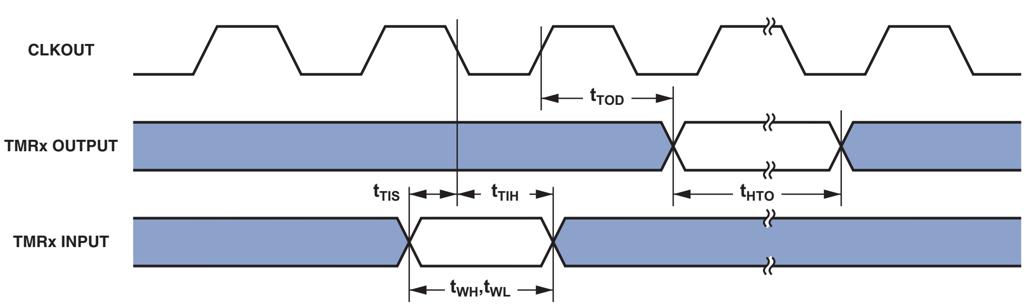


Figure 28. Timer Cycle Timing

10/100 Ethernet MAC Controller Timing

Table 40 through Table 45 and Figure 30 through Figure 35 describe the 10/100 Ethernet MAC controller operations. This feature is only available on the ADSP-BF536 and ADSP-BF537 processors.

Table 40. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Parameter[1]		Min	Max	Unit
f_{ERXCLK}	ERxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1% f_{SCLK} + 1%	MHz
$t_{ERXCLKW}$	ERxCLK Width (t_{ERxCLK} = ERxCLK Period)	$t_{ERxCLK} \times 35\%$	$t_{ERxCLK} \times 65\%$	ns
$t_{ERXCLKIS}$	Rx Input Valid to ERxCLK Rising Edge (Data In Setup)	7.5		ns
$t_{ERXCLKIH}$	ERxCLK Rising Edge to Rx Input Invalid (Data In Hold)	7.5		ns

[1] MII inputs synchronous to ERxCLK are ERxD3–0, ERxDV, and ERxER.

Table 41. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Parameter[1]		Min	Max	Unit
f_{ETXCLK}	ETxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1% f_{SCLK} + 1%	MHz
$t_{ETXCLKW}$	ETxCLK Width (t_{ETXCLK} = ETxCLK Period)	$t_{ETxCLK} \times 35\%$	$t_{ETxCLK} \times 65\%$	ns
$t_{ETXCLKOV}$	ETxCLK Rising Edge to Tx Output Valid (Data Out Valid)		20	ns
$t_{ETXCLKOH}$	ETxCLK Rising Edge to Tx Output Invalid (Data Out Hold)	0		ns

[1] MII outputs synchronous to ETxCLK are ETxD3–0.

Table 42. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
f_{REFCLK}	REF_CLK Frequency (f_{SCLK} = SCLK Frequency)	None	50 + 1% $2 \times f_{SCLK}$ + 1%	MHz
$t_{REFCLKW}$	REF_CLK Width (t_{REFCLK} = REFCLK Period)	$t_{REFCLK} \times 35\%$	$t_{REFCLK} \times 65\%$	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII REF_CLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII REF_CLK Rising Edge to Rx Input Invalid (Data In Hold)	2		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxD1–0, RMII CRS_DV, and ERxER.

Table 43. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
$t_{REFCLKOV}$	RMII REF_CLK Rising Edge to Tx Output Valid (Data Out Valid)		7.5	ns
$t_{REFCLKOH}$	RMII REF_CLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

OUTPUT DRIVE CURRENTS

Figure 36 through Figure 47 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage. See Table 9 on Page 19 for information about which driver type corresponds to a particular pin.

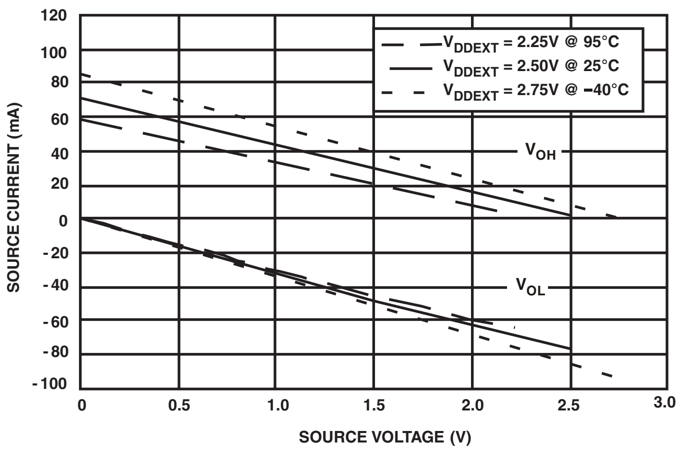


Figure 36. Drive Current A (Low V_{DDEXT})

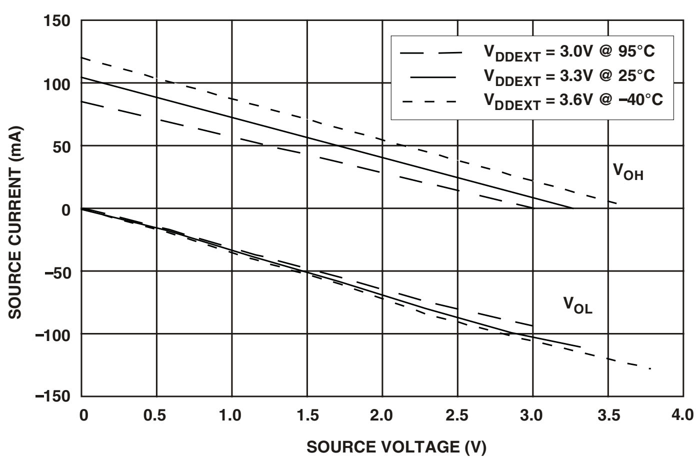


Figure 37. Drive Current A (High V_{DDEXT})

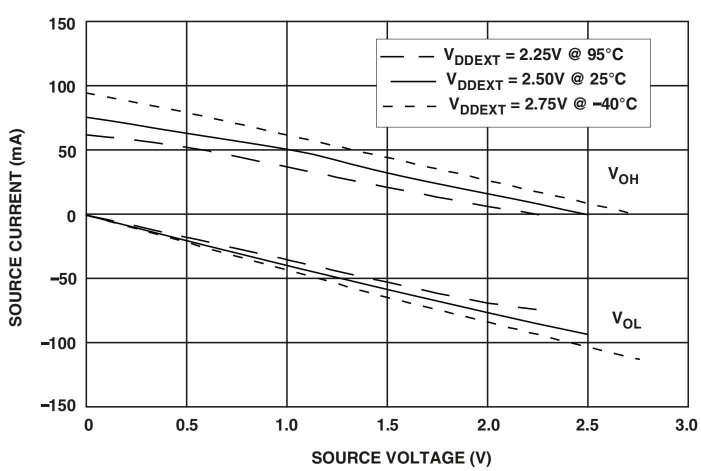


Figure 38. Drive Current B (Low V_{DDEXT})

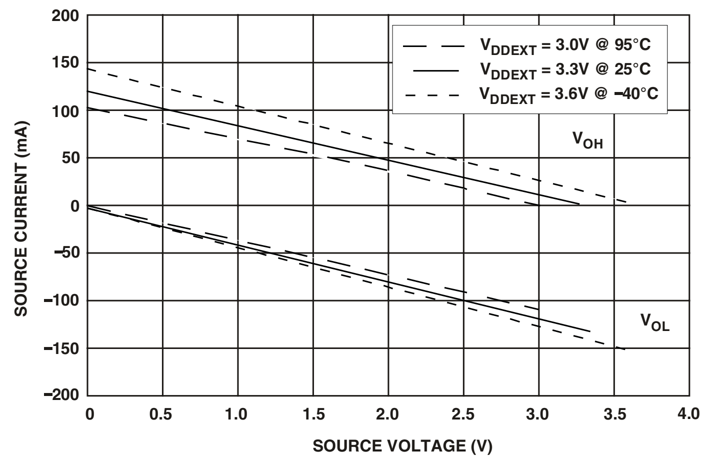


Figure 39. Drive Current B (High V_{DDEXT})

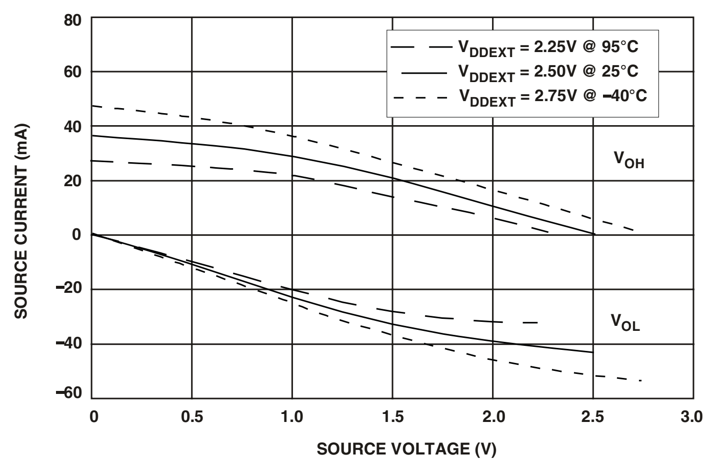


Figure 40. Drive Current C (Low V_{DDEXT})

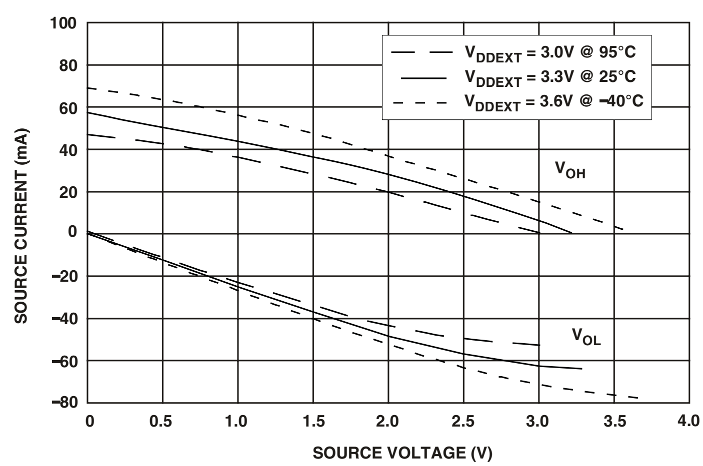


Figure 41. Drive Current C (High V_{DDEXT})

ORDERING GUIDE

In the following table CSP_BGA = Chip Scale Package Ball Grid Array.

Model[1]	Temperature Range[2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF534BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534YBCZ-4B	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBC-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3B	–40°C to +85°C	300 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBCZ3BRL	–40°C to +85°C	300 MHz	208-Ball CSP_BGA, 13" Tape and Reel	BC-208-2
ADSP-BF536BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBCZ-5AV	–40°C to +85°C	533 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5BV	–40°C to +85°C	533 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537KBCZ-6AV	0°C to +70°C	600 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537KBCZ-6BV	0°C to +70°C	600 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 23 for junction temperature (T_J) specification which is the only temperature specification.