Linear Technology - ADSP-BF534YBCZ-4B Datasheet

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

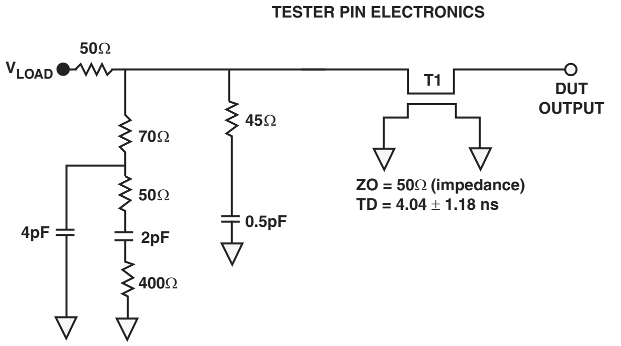
Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Blackfin+
Interface	CAN, Ethernet, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	Boot ROM (2kB)
On-Chip RAM	132kB
Voltage - I/O	3.00V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=adsp-bf534ybcz-4b

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 50). Figure 51 through Figure 60 on Page 55 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

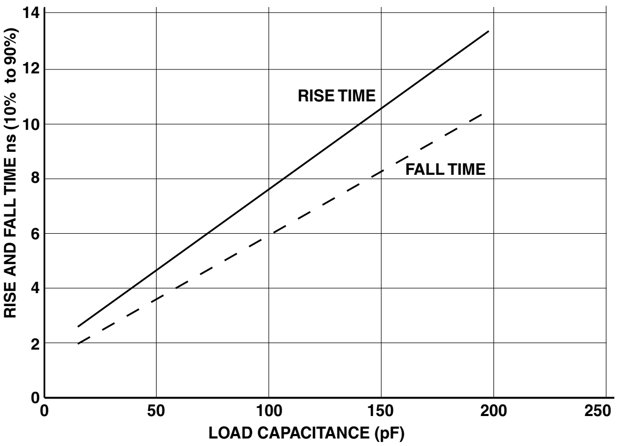


Figure 51. Typical Output Delay or Hold for Driver A at V_{DDEXT} Min

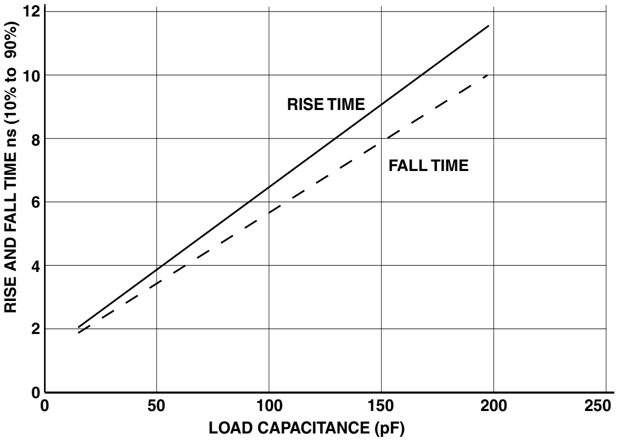


Figure 52. Typical Output Delay or Hold for Driver A at V_{DDEXT} Max