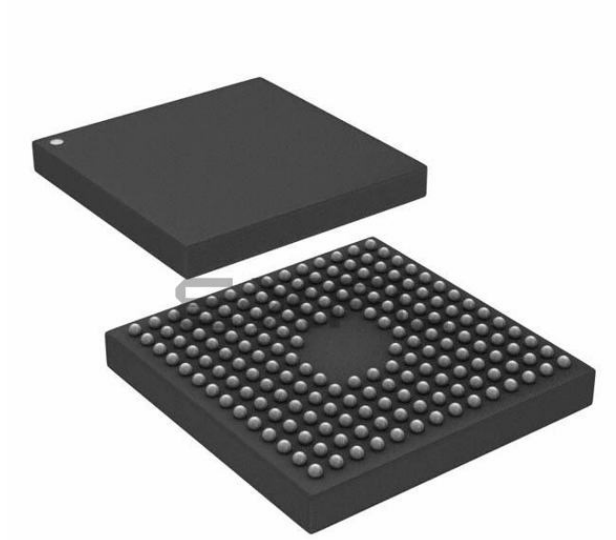

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	100kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	182-LFBGA, CSPBGA
Supplier Device Package	182-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf536bbc-3a

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the Blackfin processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 Is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (IAR). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
PLL Wakeup	IVG7	0
DMA Error (Generic)	IVG7	1
DMAR0 Block Interrupt	IVG7	1
DMAR1 Block Interrupt	IVG7	1
DMAR0 Overflow Error	IVG7	1
DMAR1 Overflow Error	IVG7	1
CAN Error	IVG7	2
Ethernet Error (ADSP-BF536 and ADSP-BF537 only)	IVG7	2
SPORT 0 Error	IVG7	2
SPORT 1 Error	IVG7	2
PPI Error	IVG7	2
SPI Error	IVG7	2
UART0 Error	IVG7	2
UART1 Error	IVG7	2
Real-Time Clock	IVG8	3
DMA Channel 0 (PPI)	IVG8	4
DMA Channel 3 (SPORT 0 Rx)	IVG9	5
DMA Channel 4 (SPORT 0 Tx)	IVG9	6
DMA Channel 5 (SPORT 1 Rx)	IVG9	7
DMA Channel 6 (SPORT 1 Tx)	IVG9	8
TWI	IVG10	9
DMA Channel 7 (SPI)	IVG10	10
DMA Channel 8 (UART0 Rx)	IVG10	11
DMA Channel 9 (UART0 Tx)	IVG10	12
DMA Channel 10 (UART1 Rx)	IVG10	13
DMA Channel 11 (UART1 Tx)	IVG10	14
CAN Rx	IVG11	15
CAN Tx	IVG11	16
DMA Channel 1 (Ethernet Rx, ADSP-BF536 and ADSP-BF537 only)	IVG11	17
Port H Interrupt A	IVG11	17
DMA Channel 2 (Ethernet Tx, ADSP-BF536 and ADSP-BF537 only)	IVG11	18
Port H Interrupt B	IVG11	18
Timer 0	IVG12	19
Timer 1	IVG12	20
Timer 2	IVG12	21
Timer 3	IVG12	22
Timer 4	IVG12	23
Timer 5	IVG12	24
Timer 6	IVG12	25
Timer 7	IVG12	26
Port F, G Interrupt A	IVG12	27
Port G Interrupt B	IVG12	28

- Programmable Rx address filters, including a 64-bit address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames.
- Advanced power management supporting unattended transfer of Rx and Tx frames and status to/from external memory via DMA during low power sleep mode.
- System wake-up from sleep operating mode upon magic packet or any of four user-definable wake-up frame filters.
- Support for 802.3Q tagged VLAN frames.
- Programmable MDC clock rate and preamble suppression.
- In RMII operation, 7 unused pins can be configured as GPIO pins for other purposes.

PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors group the many peripheral signals to four ports—Port F, Port G, Port H, and Port J. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Eight of the pins (Port F7–0) offer high source/high sink current capabilities.

General-Purpose I/O (GPIO)

The processors have 48 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Port J does not provide GPIO functionality. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output or input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processors employ a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode – Frame syncs and data are inputs into the PPI.
2. Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output (If CLKBUF is enabled, does not three-state during hibernate.)	
CLKBUF	O	Buffered XTAL Output (If enabled, does not three-state during hibernate.)	E
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This pin should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2-0 (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive (These pins should be left unconnected when not used and are driven high during hibernate.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	External Ground	

[1] See Output Drive Currents on Page 50 for more information about each driver types.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
V_{OH}[3]	High Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –2.0 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
I_{OH}[6]	High Level Output Current	V_{OH} = V_{DDEXT} – 0.5 V Min			–64			–64	mA
I_{OH}[7]		V_{OH} = V_{DDEXT} – 0.5 V Min			–144			–144	mA
V_{OL}[3]	Low Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA			0.5			0.5	V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OL} = 6 mA			0.5			0.5	V
V_{OL}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.5			0.5	V
I_{OL}[6]	Low Level Output Current	V_{OL} = 0.5 V Max			64			64	mA
I_{OL}[7]		V_{OL} = 0.5 V Max			144			144	mA
I_{IH}	High Level Input Current[8]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{IH5V}	High Level Input Current[9]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{IL}	Low Level Input Current[2]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA
I_{IHP}	High Level Input Current JTAG[10]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			50			50	µA
I_{OZH}	Three-State Leakage Current[11]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{OZH5V}	Three-State Leakage Current[12]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
C_{IN}	Input Capacitance[13, 14]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			8			8	pF
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.0 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.43		14			24		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		100			113		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		125			138		mA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		6			16		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.0 V, f_{SCLK} = 25 MHz, T_J = 25°C		9.5			19.5		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 533 MHz, T_J = 25°C, ASF = 1.00					185		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.30 V, f_{CCLK} = 600 MHz, T_J = 25°C, ASF = 1.00					227		mA
$I_{DDHIBERNATE}$[15, 16]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.60 V, CLKIN=0 MHz, T_J = maximum, with voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J= 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} =0 MHz			Table 16			Table 15	mA
$I_{DDSLEEP}$[15, 17]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})	mA
I_{DDINT}[18]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 18 × ASF)			$I_{DDSLEEP}$ + (Table 18 × ASF)	mA

[1] Applies to all 300 MHz and 400 MHz speed grade models. See Ordering Guide on Page 67.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 67.
[3] Applies to all output and bidirectional pins except port F pins, port G pins, and port H pins.
[4] Applies to port F pins PF7–0.
[5] Applies to port F pins PF15–8, all port G pins, and all port H pins.
[6] Maximum combined current for Port F7–0.
[7] Maximum total current for all port F, port G, and port H pins.
[8] Applies to all input pins except PJ4.
[9] Applies to input pin PJ4 only.
[10] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[11] Applies to three-statable pins.
[12] Applies to bidirectional pins PJ2 and PJ3.
[13] Applies to all signal pins.
[14] Guaranteed, but not tested.
[15] See the *ADSP-BF537 Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[16] CLKIN must be tied to V_{DDEXT} or GND during hibernate.
[17] In the equations, the f_{SCLK} parameter is the system clock in MHz.
[18] See Table 17 for the list of I_{DDINT} power vectors covered.

System designers should refer to *Estimating Power for the ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-297. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 18).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 17).

Table 15. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})													
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
–40	3.9	4.7	6.8	8.2	9.9	12.0	14.6	17.3	20.3	24.1	27.1	28.6	36.3	44.4
0	17.0	19.2	21.9	25.0	28.2	32.1	36.9	41.8	47.7	53.8	61.0	63.8	73.2	84.1
25	35.0	39.2	44.3	50.8	56.1	63.3	69.1	76.4	84.7	93.5	104.5	109.1	123.4	138.8
40	53.0	59.2	65.3	71.9	79.1	88.0	96.6	108.0	120.0	130.7	142.6	148.5	166.5	185.6
55	76.7	84.6	93.6	103.1	113.7	123.9	136.3	148.3	162.8	178.4	194.4	201.4	223.7	247.5
70	110.1	120.0	130.9	142.2	156.5	171.3	185.2	201.7	220.6	239.7	259.8	268.8	295.9	325.2
85	150.1	164.5	178.7	193.2	210.4	228.9	247.7	268.8	291.4	314.1	341.1	351.2	384.6	420.3
100	202.3	219.2	236.5	255.8	277.8	299.8	323.8	351.2	378.8	407.5	440.4	453.4	494.3	538.2
105	223.8	241.4	260.4	282.0	303.4	328.7	354.5	381.7	410.8	443.6	477.8	492.2	535.1	581.5

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Static Current–300 MHz and 400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})											
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–40	2.6	3.2	3.7	4.5	5.5	6.6	7.9	9.3	10.5	12.5	13.9	14.8
0	6.6	7.8	8.4	9.9	10.9	12.3	13.8	15.5	17.5	19.6	21.7	23.1
25	12.2	13.5	14.8	16.4	18.2	19.9	22.7	25.6	28.4	31.8	35.7	37.2
40	17.2	19.0	20.6	22.9	25.9	28.2	31.6	34.9	38.9	42.9	47.6	49.5
55	25.7	27.8	30.9	33.7	37.3	41.4	44.8	50.0	54.8	59.4	66.1	68.4
70	37.6	41.3	44.8	48.9	53.9	58.6	63.9	69.7	76.9	84.0	92.2	94.9
85	53.7	58.3	63.7	69.0	75.9	82.9	90.5	98.4	106.4	115.3	124.6	128.1
100	75.1	82.3	88.5	95.8	104.0	112.5	121.8	130.6	141.3	153.2	164.8	169.7
105	84.5	91.2	98.2	106.0	114.2	123.0	132.4	143.3	155.0	167.4	179.8	185.4
115[2]	103.8	111.8	120.3	127.6	138.0	148.5	159.6	171.4	184.6	198.8	213.4	219.6
120[2]	115.5	123.6	132.2	141.9	152.3	163.7	175.6	189.3	202.8	217.7	232.3	238.6

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Applies to automotive grade models only.

TIMING SPECIFICATIONS

Component specifications are subject to change without notice.

Clock and Reset Timing

Table 22. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	8.0		ns
t_{CKINH}	CLKIN High Pulse	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low	$11 \times t_{CKIN}$		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[5]	$3 \times t_{CKIN}$	$5 \times t_{CKIN}$	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 14. Since by default the PLL is multiplying the CLKIN frequency by 10 MHz, 300 MHz, and 400 MHz speed grade parts can not use the full CLKIN period range.
[2] Applies to PLL bypass mode and PLL non bypass mode.
[3] CLKIN frequency must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

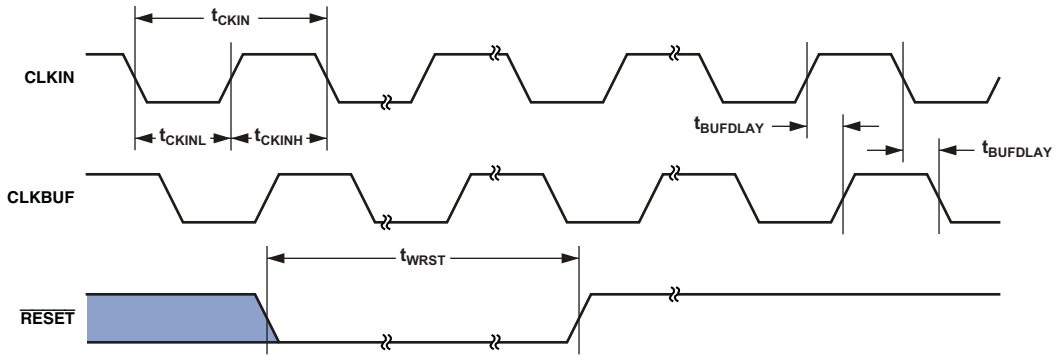
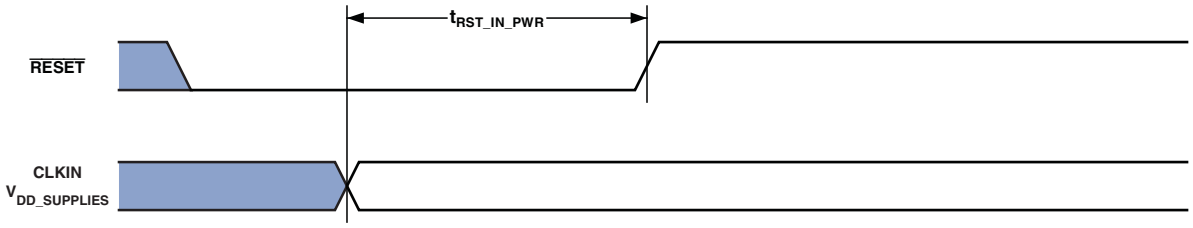


Figure 9. Clock and Reset Timing

Table 23. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



In Figure 10, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 10. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 25. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{AWE}$.

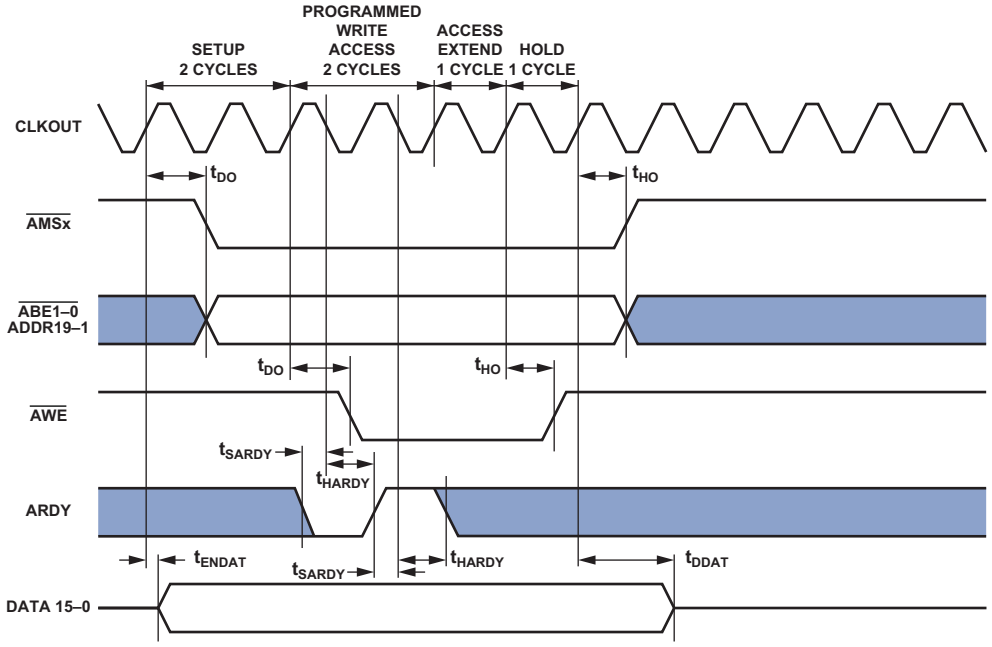


Figure 12. Asynchronous Memory Write Cycle Timing

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 13 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter[1, 2]		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT Low Setup	4.6		ns
t_{BH}	CLKOUT Low to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ Asserted Setup		3.6	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		3.6	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ Asserted Setup		3.6	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		3.6	ns

[1] These timing parameters are based on worst-case operating conditions.
[2] The pad loads for these timing parameters are 20 pF.

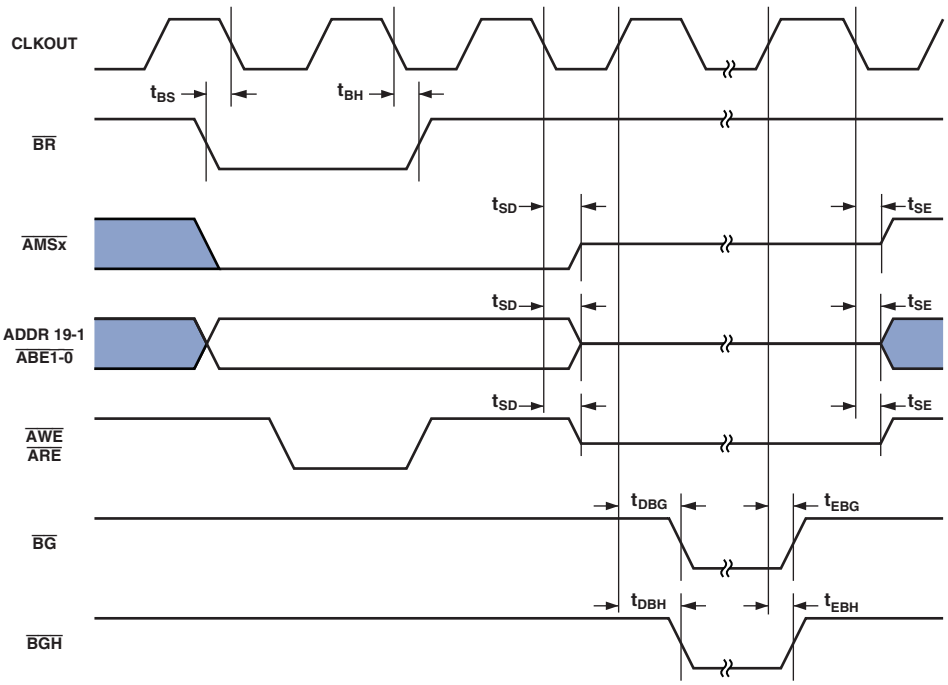


Figure 13. External Port Bus Request and Grant Cycle Timing

Table 33. External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx with MCMEN = 1, MFD = 0[1, 2]		10.0	ns
$t_{DTENLFS}$	Data Enable from Late FS or MCMEN = 1, MFD = 0[1, 2]	0		ns

[1] MCMEN = 1, TFSx enable and TFSx valid follow $t_{DDTENFS}$ and t_{DDTLFS}.
[2] If external RFSx/TFSx setup to RSCLKx/TSCLKx > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply, otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

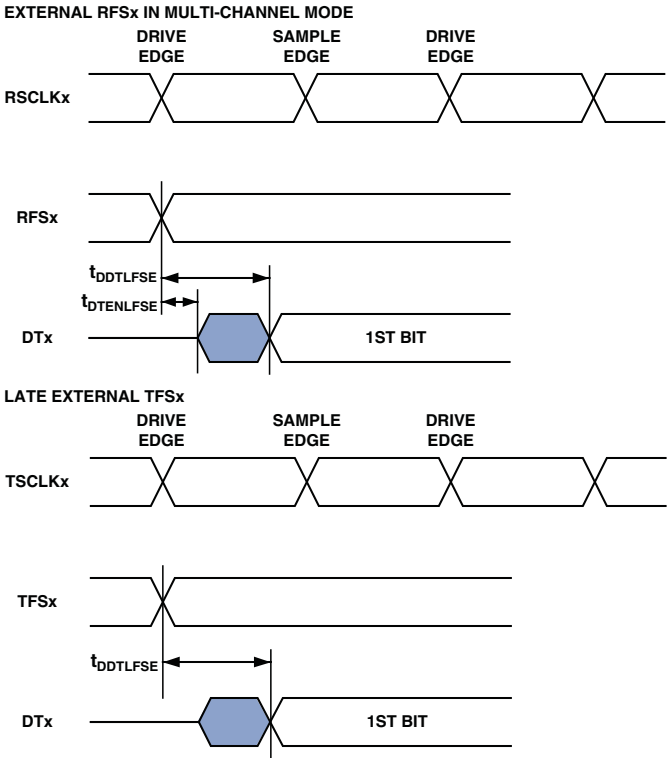


Figure 23. External Late Frame Sync

General-Purpose Port Timing

Table 36 and Figure 26 describe general-purpose port operations.

Table 36. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	0	6	ns

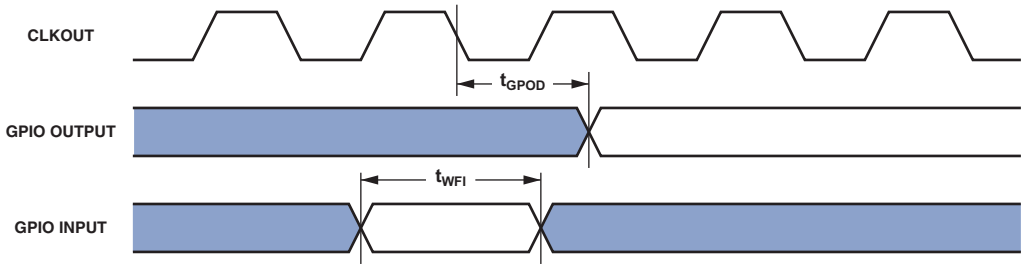


Figure 26. General-Purpose Port Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-BF537 Blackfin Processor Hardware Reference*.

Timer Clock Timing

Table 37 and Figure 27 describe timer clock timing.

Table 37. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

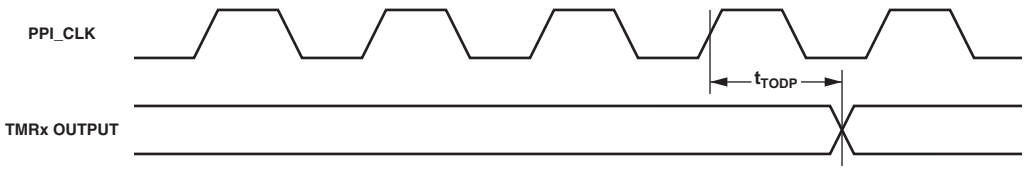


Figure 27. Timer Clock Timing

Timer Cycle Timing

Table 38 and Figure 28 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 38. Timer Cycle Timing

Parameter		2.25 V ≤ V_{DDEXT} < 2.70 V or 0.80 V ≤ V_{DDINT} < 0.95 V[1]		2.70 V ≤ V_{DDEXT} ≤ 3.60 V and 0.95 V ≤ V_{DDINT} ≤ 1.43 V[2, 3]		Unit
		Min	Max	Min	Max	
Timing Characteristics						
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[4]	1 × t_{SCLK}		1 × t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[4]	1 × t_{SCLK}		1 × t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[5]	5.5		5.0		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[5]	1.5		1.5		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	1 × t_{SCLK}	(2^{32}–1) × t_{SCLK}	1 × t_{SCLK}	(2^{32}–1) × t_{SCLK}	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		6.5		6.0	ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.
[4] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PF15 or PPI_CLK signals in PWM output mode.
[5] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

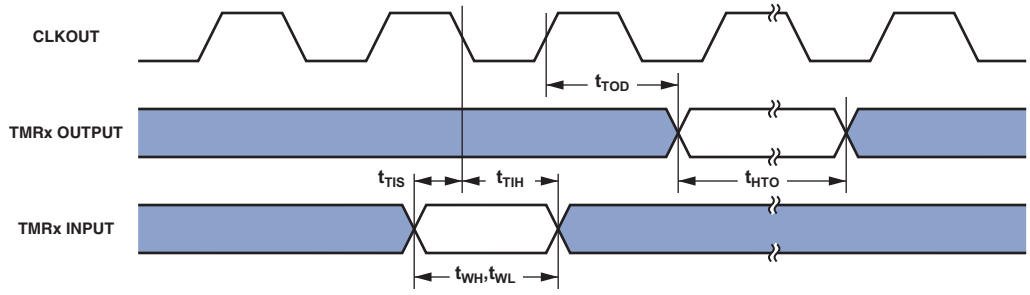


Figure 28. Timer Cycle Timing

Table 44. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 45. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	10		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	10		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

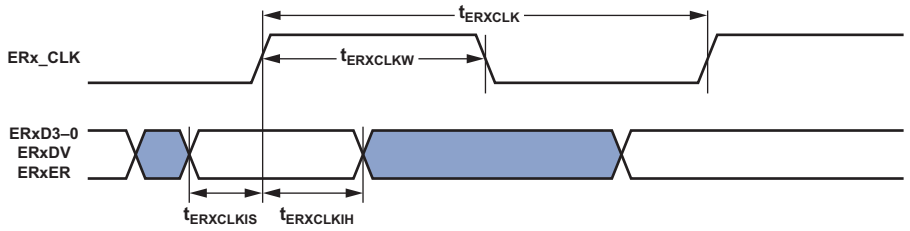


Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

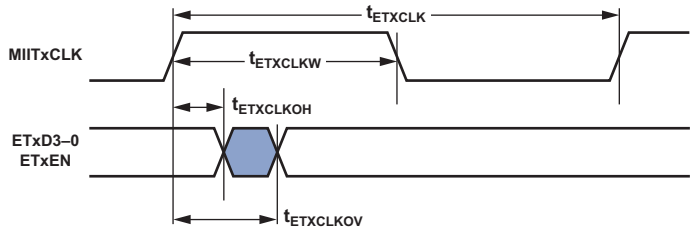


Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 48 shows the measurement point for ac measurements (other than output enable/disable). The measurement point is $V_{MEAS} = V_{DDEXT}/2$.

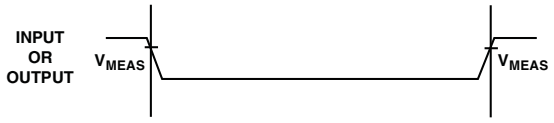


Figure 48. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the Output Enable/Disable diagram (Figure 49). The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches 2.0 V (output high) or 1.0 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.0 V or 2.0 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 49. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output-high or output-low voltage. The time t_{DECAY} is calculated with the test loads C_L and I_L, and with ΔV equal to 0.5 V.

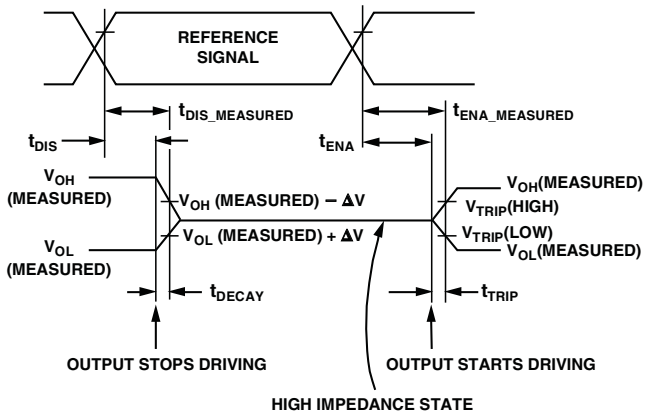


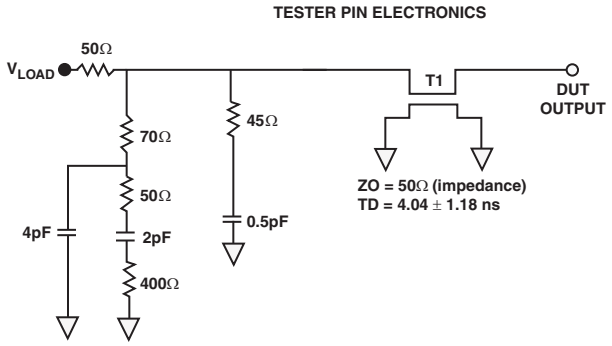
Figure 49. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV is 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the minimum disable time (for example, t_{DSDAT} for an SDRAM write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 50). Figure 51 through Figure 60 on Page 55 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

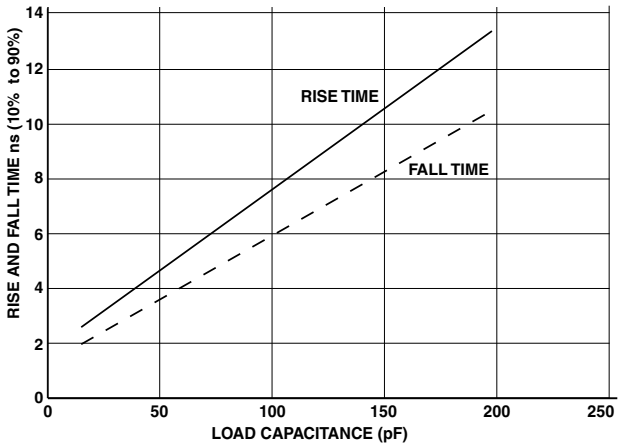


Figure 51. Typical Output Delay or Hold for Driver A at V_{DDEXT} Min

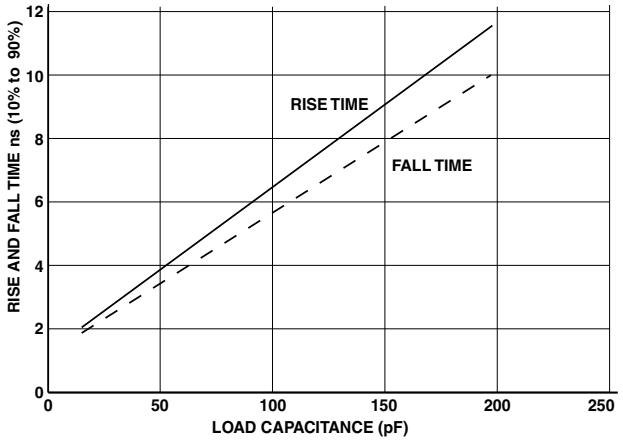


Figure 52. Typical Output Delay or Hold for Driver A at V_{DDEXT} Max

182-BALL CSP_BGA BALL ASSIGNMENT

Table 49 lists the CSP_BGA ball assignment by signal mnemonic. Table 50 on Page 58 lists the CSP_BGA ball assignment by ball number.

Table 49. 182-Ball CSP_BGA Ball Assignment (Alphabetically by Signal Mnemonic)

Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.
$\overline{ABE0}$	H13	CLKOUT	B14	GND	L6	PG8	E3	$\overline{SRAS}$	D13
$\overline{ABE1}$	H12	DATA0	M9	GND	L8	PG9	E4	$\overline{SWE}$	D12
ADDR1	J14	DATA1	N9	GND	L10	PH0	C2	TCK	P2
ADDR10	M13	DATA10	N6	GND	M4	PH1	C3	TDI	M3
ADDR11	M14	DATA11	P6	GND	M10	PH10	B6	TDO	N3
ADDR12	N14	DATA12	M5	GND	P14	PH11	A2	TMS	N2
ADDR13	N13	DATA13	N5	$\overline{NMI}$	B10	PH12	A3	$\overline{TRST}$	N1
ADDR14	N12	DATA14	P5	PF0	M1	PH13	A4	V_{DDEXT}	A1
ADDR15	M11	DATA15	P4	PF1	L1	PH14	A5	V_{DDEXT}	C12
ADDR16	N11	DATA2	P9	PF10	J2	PH15	A6	V_{DDEXT}	E6
ADDR17	P13	DATA3	M8	PF11	J3	PH2	C4	V_{DDEXT}	E11
ADDR18	P12	DATA4	N8	PF12	H1	PH3	C5	V_{DDEXT}	F4
ADDR19	P11	DATA5	P8	PF13	H2	PH4	C6	V_{DDEXT}	F12
ADDR2	K14	DATA6	M7	PF14	H3	PH5	B1	V_{DDEXT}	H5
ADDR3	L14	DATA7	N7	PF15	H4	PH6	B2	V_{DDEXT}	H10
ADDR4	J13	DATA8	P7	PF2	L2	PH7	B3	V_{DDEXT}	J11
ADDR5	K13	DATA9	M6	PF3	L3	PH8	B4	V_{DDEXT}	J12
ADDR6	L13	$\overline{EMU}$	M2	PF4	L4	PH9	B5	V_{DDEXT}	K7
ADDR7	K12	GND	A10	PF5	K1	PJ0	C7	V_{DDEXT}	K9
ADDR8	L12	GND	A14	PF6	K2	PJ1	B7	V_{DDEXT}	L7
ADDR9	M12	GND	D4	PF7	K3	PJ10	D10	V_{DDEXT}	L9
$\overline{AMS0}$	E14	GND	E7	PF8	K4	PJ11	D11	V_{DDEXT}	L11
$\overline{AMS1}$	F14	GND	E9	PF9	J1	PJ2	B11	V_{DDEXT}	P1
$\overline{AMS2}$	F13	GND	F5	PG0	G1	PJ3	C11	V_{DDINT}	E5
$\overline{AMS3}$	G12	GND	F6	PG1	G2	PJ4	D7	V_{DDINT}	E8
$\overline{AOE}$	G13	GND	F10	PG10	D1	PJ5	D8	V_{DDINT}	E10
ARDY	E13	GND	F11	PG11	D2	PJ6	C8	V_{DDINT}	G10
$\overline{ARE}$	G14	GND	G4	PG12	D3	PJ7	B8	V_{DDINT}	K5
$\overline{AWE}$	H14	GND	G5	PG13	D5	PJ8	D9	V_{DDINT}	K8
$\overline{BG}$	P10	GND	G11	PG14	D6	PJ9	C9	V_{DDINT}	K10
$\overline{BGH}$	N10	GND	H11	PG15	C1	$\overline{RESET}$	C10	V_{DDRTC}	B9
BMODE0	N4	GND	J4	PG2	G3	RTXO	A8	VROUT0	A13
BMODE1	P3	GND	J5	PG3	F1	RTXI	A9	VROUT1	B12
BMODE2	L5	GND	J9	PG4	F2	SA10	E12	XTAL	A11
$\overline{BR}$	D14	GND	J10	PG5	F3	$\overline{SCAS}$	C14		
CLKBUF	A7	GND	K6	PG6	E1	SCKE	B13		
CLKIN	A12	GND	K11	PG7	E2	$\overline{SMS}$	C13		

Table 50. 182-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	V_{DDEXT}	C10	$\overline{RESET}$	F5	GND	J14	ADDR1	M9	DATA0
A2	PH11	C11	PJ3	F6	GND	K1	PF5	M10	GND
A3	PH12	C12	V_{DDEXT}	F10	GND	K2	PF6	M11	ADDR15
A4	PH13	C13	$\overline{SMS}$	F11	GND	K3	PF7	M12	ADDR9
A5	PH14	C14	$\overline{SCAS}$	F12	V_{DDEXT}	K4	PF8	M13	ADDR10
A6	PH15	D1	PG10	F13	$\overline{AMS2}$	K5	V_{DDINT}	M14	ADDR11
A7	CLKBUF	D2	PG11	F14	$\overline{AMS1}$	K6	GND	N1	$\overline{TRST}$
A8	RTXO	D3	PG12	G1	PG0	K7	V_{DDEXT}	N2	TMS
A9	RTXI	D4	GND	G2	PG1	K8	V_{DDINT}	N3	TDO
A10	GND	D5	PG13	G3	PG2	K9	V_{DDEXT}	N4	BMODE0
A11	XTAL	D6	PG14	G4	GND	K10	V_{DDINT}	N5	DATA13
A12	CLKIN	D7	PJ4	G5	GND	K11	GND	N6	DATA10
A13	VROUT0	D8	PJ5	G10	V_{DDINT}	K12	ADDR7	N7	DATA7
A14	GND	D9	PJ8	G11	GND	K13	ADDR5	N8	DATA4
B1	PH5	D10	PJ10	G12	$\overline{AMS3}$	K14	ADDR2	N9	DATA1
B2	PH6	D11	PJ11	G13	$\overline{AOE}$	L1	PF1	N10	$\overline{BGH}$
B3	PH7	D12	$\overline{SWE}$	G14	$\overline{ARE}$	L2	PF2	N11	ADDR16
B4	PH8	D13	$\overline{SRAS}$	H1	PF12	L3	PF3	N12	ADDR14
B5	PH9	D14	$\overline{BR}$	H2	PF13	L4	PF4	N13	ADDR13
B6	PH10	E1	PG6	H3	PF14	L5	BMODE2	N14	ADDR12
B7	PJ1	E2	PG7	H4	PF15	L6	GND	P1	V_{DDEXT}
B8	PJ7	E3	PG8	H5	V_{DDEXT}	L7	V_{DDEXT}	P2	TCK
B9	V_{DDRTC}	E4	PG9	H10	V_{DDEXT}	L8	GND	P3	BMODE1
B10	$\overline{NMI}$	E5	V_{DDINT}	H11	GND	L9	V_{DDEXT}	P4	DATA15
B11	PJ2	E6	V_{DDEXT}	H12	$\overline{ABE1}$	L10	GND	P5	DATA14
B12	VROUT1	E7	GND	H13	$\overline{ABE0}$	L11	V_{DDEXT}	P6	DATA11
B13	SCKE	E8	V_{DDINT}	H14	$\overline{AWE}$	L12	ADDR8	P7	DATA8
B14	CLKOUT	E9	GND	J1	PF9	L13	ADDR6	P8	DATA5
C1	PG15	E10	V_{DDINT}	J2	PF10	L14	ADDR3	P9	DATA2
C2	PH0	E11	V_{DDEXT}	J3	PF11	M1	PF0	P10	$\overline{BG}$
C3	PH1	E12	SA10	J4	GND	M2	$\overline{EMU}$	P11	ADDR19
C4	PH2	E13	ARDY	J5	GND	M3	TDI	P12	ADDR18
C5	PH3	E14	$\overline{AMS0}$	J9	GND	M4	GND	P13	ADDR17
C6	PH4	F1	PG3	J10	GND	M5	DATA12	P14	GND
C7	PJ0	F2	PG4	J11	V_{DDEXT}	M6	DATA9		
C8	PJ6	F3	PG5	J12	V_{DDEXT}	M7	DATA6		
C9	PJ9	F4	V_{DDEXT}	J13	ADDR4	M8	DATA3		

SURFACE-MOUNT DESIGN

The following table is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
182-Ball CSP_BGA (BC-182)	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
208-Ball CSP_BGA (BC-208-2)	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter

AUTOMOTIVE PRODUCTS

The ADBF534W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 53 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 53. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF534WBBCZ4Axx	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADBF534WBBCZ4Bxx	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADBF534WYBCZ4Bxx	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature.

ORDERING GUIDE

In the following table CSP_BGA = Chip Scale Package Ball Grid Array.

Model [1]	Temperature Range [2]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF534BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF534BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534YBCZ-4B	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF534BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBC-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3A	–40°C to +85°C	300 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBC-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-4A	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF536BBCZ-3B	–40°C to +85°C	300 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF536BBCZ3BRL	–40°C to +85°C	300 MHz	208-Ball CSP_BGA, 13" Tape and Reel	BC-208-2
ADSP-BF536BBCZ-4B	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBC-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5A	–40°C to +85°C	500 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5B	–40°C to +85°C	500 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537BBCZ-5AV	–40°C to +85°C	533 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537BBCZ-5BV	–40°C to +85°C	533 MHz	208-Ball CSP_BGA	BC-208-2
ADSP-BF537KBCZ-6AV	0°C to +70°C	600 MHz	182-Ball CSP_BGA	BC-182
ADSP-BF537KBCZ-6BV	0°C to +70°C	600 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 23 for junction temperature (T_J) specification which is the only temperature specification.