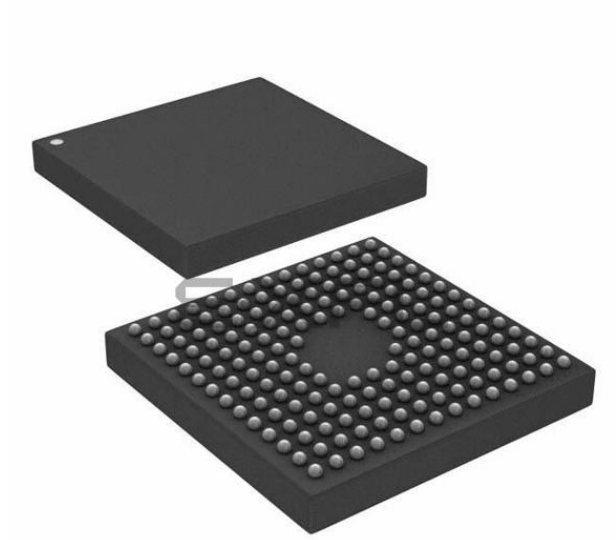

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	100kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	182-LFBGA, CSPBGA
Supplier Device Package	182-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf536bbcz-3a

In conjunction with the general-purpose timer functions, autobaud detection is supported.

The capabilities of the UARTs are further extended with support for the infrared data association (IrDA®) serial infrared physical layer link specification (SIR) protocol.

CONTROLLER AREA NETWORK (CAN)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors offer a CAN controller that is a communication controller implementing the CAN 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well-suited for control applications due to its capability to communicate reliably over a network, since the protocol incorporates CRC checking message error tracking, and fault node confinement.

The CAN controller offers the following features:

- 32 mailboxes (eight receive only, eight transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wake-up from hibernation mode (lowest static power consumption mode).
- Interrupts, including: Tx complete, Rx complete, error, global.

The electrical characteristics of each network connection are very demanding so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high-speed, fault-tolerant, single-wire transceivers.

TWI CONTROLLER INTERFACE

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 2-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I^2C® bus standard. The TWI module offers the capabilities of simultaneous master and slave operation, support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the processor's TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

10/100 ETHERNET MAC

The ADSP-BF536 and ADSP-BF537 processors offer the capability to directly connect to a network by way of an embedded fast Ethernet Media Access Controller (MAC) that supports both 10-BaseT (10 Mbps) and 100-BaseT (100 Mbps) operation. The 10/100 Ethernet MAC peripheral is fully compliant to the IEEE 802.3-2002 standard, and it provides programmable features designed to minimize supervision, bus use, or message processing by the rest of the processor system.

Some standard features are

- Support of MII and RMII protocols for external PHYs.
- Full duplex and half duplex modes.
- Data framing and encapsulation: generation and detection of preamble, length padding, and FCS.
- Media access management (in half-duplex operation): collision and contention handling, including control of retransmission of collision frames and of back-off timing.
- Flow control (in full-duplex operation): generation and detection of PAUSE frames.
- Station management: generation of MDC/MDIO frames for read-write access to PHY registers.
- SCLK operating range down to 25 MHz (active and sleep operating modes).
- Internal loopback from Tx to Rx.

Some advanced features are

- Buffered crystal output to external PHY for support of a single crystal system.
- Automatic checksum computation of IP header and IP payload fields of Rx frames.
- Independent 32-bit descriptor-driven Rx and Tx DMA channels.
- Frame status delivery to memory via DMA, including frame completion semaphores, for efficient buffer queue management in software.
- Tx DMA support for separate descriptors for MAC header and payload to eliminate buffer copy operations.
- Convenient frame alignment modes support even 32-bit alignment of encapsulated Rx or Tx IP packet data in memory after the 14-byte MAC header.
- Programmable Ethernet event interrupt supports any combination of
  - Any selected Rx or Tx frame status conditions.
  - PHY interrupt condition.
  - Wake-up frame detected.
  - Any selected MAC management counter(s) at half-full.
  - DMA descriptor error.
- 47 MAC management statistics counters with selectable clear-on-read behavior and programmable interrupts on half maximum value.

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

1. Active video only mode
2. Vertical blanking only mode
3. Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide five operating modes, each with a different performance and power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode. Also, see Table 16, Table 15 and Table 17.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wake-up causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

hibernate state, V_{DDEXT} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by asserting the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. The regulator can also be disabled and bypassed at the user's discretion. For additional information on voltage regulation, see *Switching Regulator Design Considerations for the ADSP-BF533 Blackfin Processors (EE-228)*.

CLOCK SIGNALS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the processors include an on-chip oscillator circuit, an external crystal can be used. For fundamental frequency operation, use the circuit shown in Figure 6. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Further parallel resistors are typically not recommended. The two capacitors and the series resistor shown in Figure 6 fine-tune phase and amplitude of the sine frequency.

The capacitor and resistor values shown in Figure 6 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. The user should verify the customized values based on careful investigations of multiple devices over temperature range.

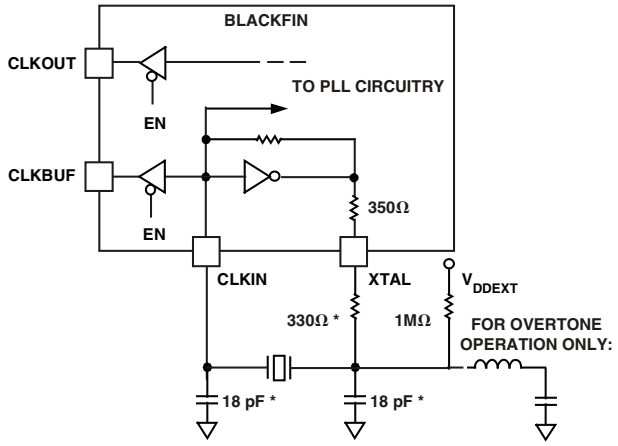


Figure 6. External Crystal Connections

A third-overtone crystal can be used for frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone, by adding a tuned inductor circuit as shown in Figure 6. A design procedure for third-overtone operation is discussed in detail in the application note *Using Third Overtone Crystals with the ADSP-218x DSP (EE-168)*.

The CLKBUF pin is an output pin, and is a buffer version of the input clock. This pin is particularly useful in Ethernet applications to limit the number of required clock sources in the system. In this type of application, a single 25 MHz or 50 MHz crystal can be applied directly to the processors. The 25 MHz or 50 MHz output of CLKBUF can then be connected to an external Ethernet MII or RMII PHY device.

Because of the default 10× PLL multiplier, providing a 50 MHz CLKIN exceeds the recommended operating conditions of the lower speed grades. Because of this restriction, an RMII PHY requiring a 50 MHz clock input cannot be clocked directly from the CLKBUF pin for the lower speed grades. In this case, either provide a separate 50 MHz clock source, or use an RMII PHY with 25 MHz clock input options. The CLKBUF output is active by default and can be disabled using the VR_CTL register for power savings.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 7, the core clock (CCLK) and system peripheral clock (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 10×, but it can be modified by a software instruction sequence in the PLL_CTL register.

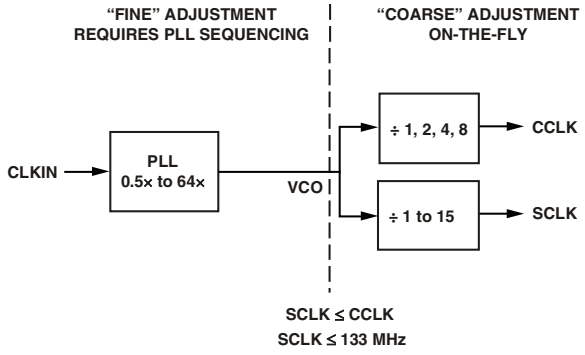


Figure 7. Frequency Modification Methods

On-the-fly CCLK and SCLK frequency changes can be effected by simply writing to the PLL_DIV register. Whereas the maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}, the VCO is always permitted to run up to the frequency specified by the part's speed grade. The CLKOUT pin reflects the SCLK frequency to the off-chip world. It belongs to the SDRAM interface, but it functions as a reference signal in other timing specifications as well. While active by default, it can be disabled using the EBIU_SDGCTL and EBIU_AMGCTL registers.

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output

- Boot from serial TWI memory (EEPROM/flash) – The Blackfin processor operates in master mode and selects the TWI slave with the unique ID 0xA0. It submits successive read commands to the memory device starting at 2-byte internal address 0x0000 and begins clocking data into the processor. The TWI memory device should comply with Philips I^2C Bus Specification version 2.1 and have the capability to auto-increment its internal address counter such that the contents of the memory device can be read sequentially.
- Boot from TWI host – The TWI host agent selects the slave with the unique ID 0x5F. The processor replies with an acknowledgement and the host can then download the boot stream. The TWI host agent should comply with Philips I^2C Bus Specification version 2.1. An I^2C multiplexer can be used to select one processor at a time when booting multiple processors from a single TWI.

For each of the boot modes, a 10-byte header is first brought in from an external device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks can be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the start of L1 instruction SRAM.

In addition, Bit 4 of the reset configuration register can be set by application code to bypass the normal boot sequence during a software reset. For this case, the processor jumps directly to the beginning of L1 instruction memory.

To augment the boot modes, a secondary software loader can be added to provide additional booting mechanisms. This secondary loader could provide the capability to boot from flash, variable baud rate, and other sources. In all boot modes except bypass, program execution starts from on-chip L1 memory address 0xFFA0 0000.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16-bit and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation

suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF534/ADSP-BF536/ADSP-BF537 processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *Getting Started with Blackfin Processors*
- *ADSP-BF537 Blackfin Processor Hardware Reference*
- *ADSP-BF53x/ADSP-BF56x Blackfin Processor Programming Reference*
- *ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin Processor Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN DESCRIPTIONS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors pin definitions are listed in Table 9. In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics. Pins shown with an asterisk after their name (*) offer high source/high sink current capabilities.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

All I/O pins have their input buffers disabled with the exception of the pins noted in the data sheet that need pull-ups or pull-downs if unused.

The SDA (serial data) and SCL (serial clock) pins are open drain and therefore require a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high when not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable(Requires a pull-down if hibernate with SDRAM self-refresh is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/UART1–0/Timer7–0/SPI/ External DMA Request/PPI (= High Source/High Sink Pin)*			
PF0* – GPIO/*UART0 TX/DMAR0*	I/O	GPIO/*UART0 Transmit/DMA Request 0*	C
PF1* – GPIO/*UART0 RX/DMAR1/TACI1*	I/O	GPIO/*UART0 Receive/DMA Request 1/Timer1 Alternate Input Capture*	C
PF2* – GPIO/*UART1 TX/TMR7*	I/O	GPIO/*UART1 Transmit/Timer7*	C
PF3* – GPIO/*UART1 RX/TMR6/TACI6*	I/O	GPIO/*UART1 Receive/Timer6/Timer6 Alternate Input Capture*	C
PF4* – GPIO/*TMR5/SPI SSEL6*	I/O	GPIO/*Timer5/SPI Slave Select Enable 6*	C
PF5* – GPIO/*TMR4/SPI SSEL5*	I/O	GPIO/*Timer4/SPI Slave Select Enable 5*	C
PF6* – GPIO/*TMR3/SPI SSEL4*	I/O	GPIO/*Timer3/SPI Slave Select Enable 4*	C
PF7* – GPIO/*TMR2/PPI FS3*	I/O	GPIO/*Timer2/PPI Frame Sync 3*	C
PF8 – GPIO/*TMR1/PPI FS2*	I/O	GPIO/*Timer1/PPI Frame Sync 2*	C
PF9 – GPIO/*TMR0/PPI FS1*	I/O	GPIO/*Timer0/PPI Frame Sync 1*	C
PF10 – GPIO/*SPI SSEL1*	I/O	GPIO/*SPI Slave Select Enable 1*	C
PF11 – GPIO/*SPI MOSI*	I/O	GPIO/*SPI Master Out Slave In*	C
PF12 – GPIO/*SPI MISO*	I/O	GPIO/*SPI Master In Slave Out* (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
PF13 – GPIO/*SPI SCK*	I/O	GPIO/*SPI Clock*	D
PF14 – GPIO/*SPI SS/TACLK0*	I/O	GPIO/*SPI Slave Select/Alternate Timer0 Clock Input*	C
PF15 – GPIO/*PPI CLK/TMRCLK*	I/O	GPIO/*PPI Clock/External Timer Reference*	C
Port G: GPIO/PPI/SPORT1			
PG0 – GPIO/*PPI D0*	I/O	GPIO/*PPI Data 0*	C
PG1 – GPIO/*PPI D1*	I/O	GPIO/*PPI Data 1*	C
PG2 – GPIO/*PPI D2*	I/O	GPIO/*PPI Data 2*	C
PG3 – GPIO/*PPI D3*	I/O	GPIO/*PPI Data 3*	C
PG4 – GPIO/*PPI D4*	I/O	GPIO/*PPI Data 4*	C
PG5 – GPIO/*PPI D5*	I/O	GPIO/*PPI Data 5*	C
PG6 – GPIO/*PPI D6*	I/O	GPIO/*PPI Data 6*	C
PG7 – GPIO/*PPI D7*	I/O	GPIO/*PPI Data 7*	C
PG8 – GPIO/*PPI D8/DR1SEC*	I/O	GPIO/*PPI Data 8/SPORT1 Receive Data Secondary*	C
PG9 – GPIO/*PPI D9/DT1SEC*	I/O	GPIO/*PPI Data 9/SPORT1 Transmit Data Secondary*	C
PG10 – GPIO/*PPI D10/RSCLK1*	I/O	GPIO/*PPI Data 10/SPORT1 Receive Serial Clock*	D
PG11 – GPIO/*PPI D11/RFS1*	I/O	GPIO/*PPI Data 11/SPORT1 Receive Frame Sync*	C
PG12 – GPIO/*PPI D12/DR1PRI*	I/O	GPIO/*PPI Data 12/SPORT1 Receive Data Primary*	C
PG13 – GPIO/*PPI D13/TSCLK1*	I/O	GPIO/*PPI Data 13/SPORT1 Transmit Serial Clock*	D
PG14 – GPIO/*PPI D14/TFS1*	I/O	GPIO/*PPI Data 14/SPORT1 Transmit Frame Sync*	C
PG15 – GPIO/*PPI D15/DT1PRI*	I/O	GPIO/*PPI Data 15/SPORT1 Transmit Data Primary*	C

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
C_{IN}	Input Capacitance[13, 14]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V			8			8	pF
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.0 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.43		14			24		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 300 MHz, T_J = 25°C, ASF = 1.00		100			113		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.14 V, f_{CCLK} = 400 MHz, T_J = 25°C, ASF = 1.00		125			138		mA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		6			16		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.0 V, f_{SCLK} = 25 MHz, T_J = 25°C		9.5			19.5		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 533 MHz, T_J = 25°C, ASF = 1.00					185		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.30 V, f_{CCLK} = 600 MHz, T_J = 25°C, ASF = 1.00					227		mA
$I_{DDHIBERNATE}$[15, 16]	V_{DDEXT} Current in Hibernate State	V_{DDEXT} = 3.60 V, CLKIN=0 MHz, T_J = maximum, with voltage regulator off (V_{DDINT} = 0 V)		50	100		50	100	µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J= 25°C		20			20		µA
$I_{DDDEEPSLEEP}$[15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} =0 MHz			Table 16			Table 15	mA
$I_{DDSLEEP}$[15, 17]	V_{DDINT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})			$I_{DDDEEPSLEEP}$ + (0.14 × V_{DDINT} × f_{SCLK})	mA
I_{DDINT}[18]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 18 × ASF)			$I_{DDSLEEP}$ + (Table 18 × ASF)	mA

[1] Applies to all 300 MHz and 400 MHz speed grade models. See Ordering Guide on Page 67.
[2] Applies to all 500 MHz, 533 MHz, and 600 MHz speed grade models. See Ordering Guide on Page 67.
[3] Applies to all output and bidirectional pins except port F pins, port G pins, and port H pins.
[4] Applies to port F pins PF7–0.
[5] Applies to port F pins PF15–8, all port G pins, and all port H pins.
[6] Maximum combined current for Port F7–0.
[7] Maximum total current for all port F, port G, and port H pins.
[8] Applies to all input pins except PJ4.
[9] Applies to input pin PJ4 only.
[10] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[11] Applies to three-statable pins.
[12] Applies to bidirectional pins PJ2 and PJ3.
[13] Applies to all signal pins.
[14] Guaranteed, but not tested.
[15] See the *ADSP-BF537 Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[16] CLKIN must be tied to V_{DDEXT} or GND during hibernate.
[17] In the equations, the f_{SCLK} parameter is the system clock in MHz.
[18] See Table 17 for the list of I_{DDINT} power vectors covered.

Table 17. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.33
$I_{DD-HIGH}$	1.29
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.43

[1] See EE-297 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 18. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})													
Frequency (MHz)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
50	11.0	13.7	19.13	18.2	18.67	19.13	19.6	21.2	24.1	25.5	28.5	28.6	28.85	29.2
100	27.9	22.7	30.8	28.4	29.3	30.8	32.9	35.3	37.8	40.6	43.5	43.7	44.1	45.8
200	36.9	42.6	55.0	49.2	51.5	55.0	58.3	62.9	67.0	69.7	73.0	74.0	75.7	80.7
300	N/A	61.5	79.2	70.4	74.6	79.2	84.4	90.7	94.3	99.1	103.9	105.5	108.0	113.4
400	N/A	N/A	N/A	92.4	97.2	104.3	109.8	116.5	121.9	128.0	134.6	136.6	139.8	145.1
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	142.3	149.3	157.5	164.7	166.7	169.8	176.9
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	158.6	167.0	174.3	176.6	180.1	187.9
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	193.7	196.5	200.7	210.0

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 19 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 19. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	−0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	−0.3 V to +3.8 V
Input Voltage[1]	−0.5 V to +3.6 V
Input Voltage[1, 2]	−0.5 V to +5.5 V
Output Voltage Swing	−0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.
[2] Applies to 5 V tolerant pins SCL, SDA, and PJ4. For duty cycles, see Table 20.

Table 20. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
−0.50	+3.80	100%
−0.70	+4.00	40%
−0.80	+4.10	25%
−0.90	+4.20	15%
−1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, and VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 8 and Table 21 provide details about the package branding for the Blackfin processors. For a complete listing of product availability, see Ordering Guide on Page 67.

Figure 8. Product Information on Package

Table 21. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Nonautomotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

TIMING SPECIFICATIONS

Component specifications are subject to change without notice.

Clock and Reset Timing

Table 22. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse	8.0		ns
t_{CKINH}	CLKIN High Pulse	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low	$11 \times t_{CKIN}$		ns
t_{NOBOOT}	$\overline{\text{RESET}}$ Deassertion to First External Access Delay[5]	$3 \times t_{CKIN}$	$5 \times t_{CKIN}$	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 10 through Table 14. Since by default the PLL is multiplying the CLKIN frequency by 10 MHz, 300 MHz, and 400 MHz speed grade parts can not use the full CLKIN period range.
[2] Applies to PLL bypass mode and PLL non bypass mode.
[3] CLKIN frequency must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies when processor is configured in No Boot Mode (BMODE2-0 = b#000).

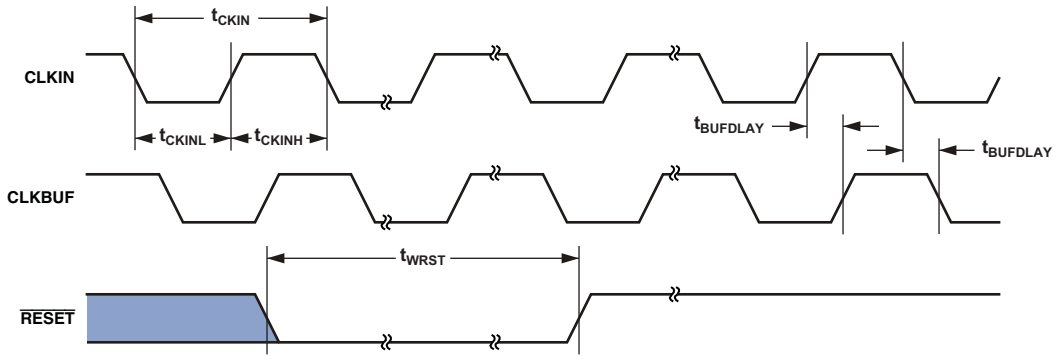
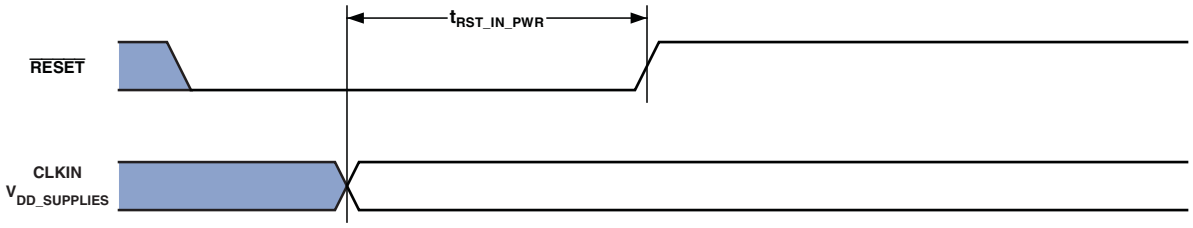


Figure 9. Clock and Reset Timing

Table 23. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDRTC}, and CLKIN Pins Are Stable and Within Specification	$3500 \times t_{CKIN}$		ns



In Figure 10, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDRTC}

Figure 10. Power-Up Reset Timing

Parallel Peripheral Interface Timing

Table 29 and Figure 16 on Page 36, Figure 20 on Page 39, and Figure 23 on Page 41 describe parallel peripheral interface operations.

Table 29. Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPI_CLK Width[1]	6.0		ns
t_{PCLK}	PPI_CLK Period[1]	15.0		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPI_CLK	6.7		ns
t_{HFSPE}	External Frame Sync Hold After PPI_CLK	1.0		ns
t_{SDRPE}	Receive Data Setup Before PPI_CLK	3.5		ns
t_{HDRPE}	Receive Data Hold After PPI_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPI_CLK		8.0	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPI_CLK	1.7		ns
t_{DDTPE}	Transmit Data Delay After PPI_CLK		8.0	ns
t_{HDTPE}	Transmit Data Hold After PPI_CLK	1.8		ns

[1] PPI_CLK frequency cannot exceed $f_{SCLK}/2$.

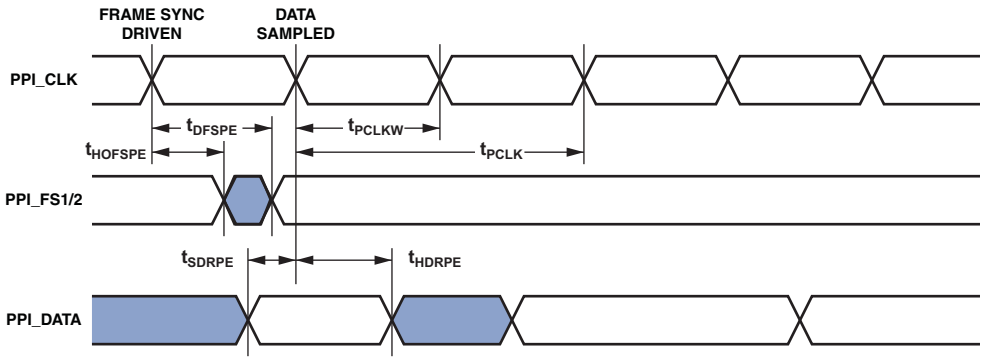


Figure 16. PPI GP Rx Mode with Internal Frame Sync Timing

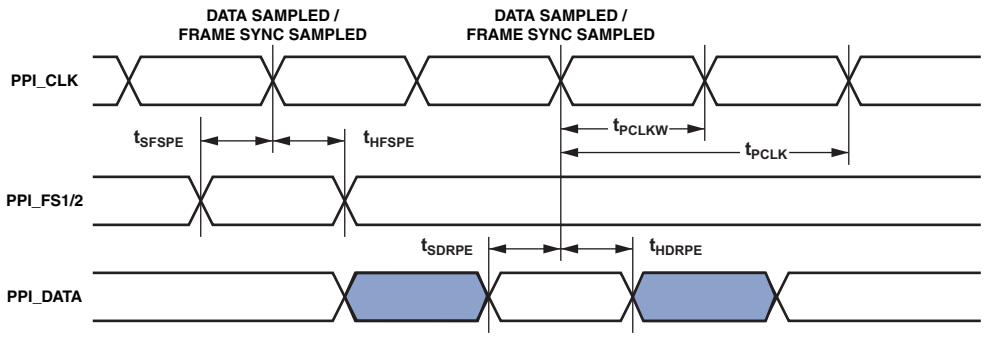


Figure 17. PPI GP Rx Mode with External Frame Sync Timing

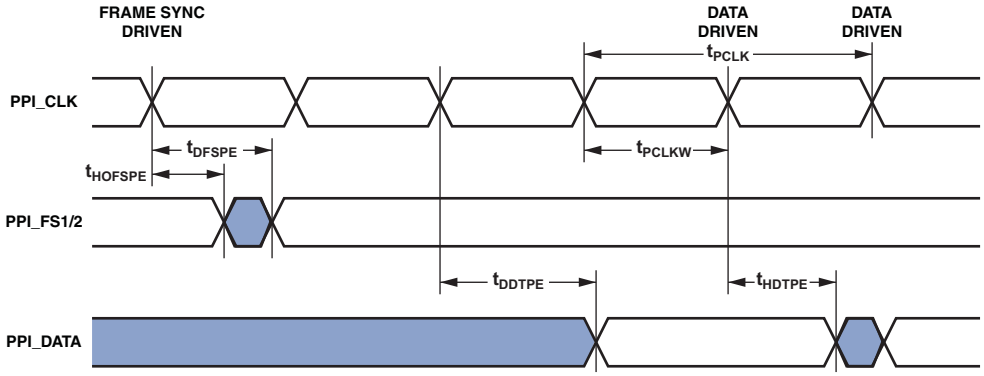


Figure 18. PPI GP Tx Mode with Internal Frame Sync Timing

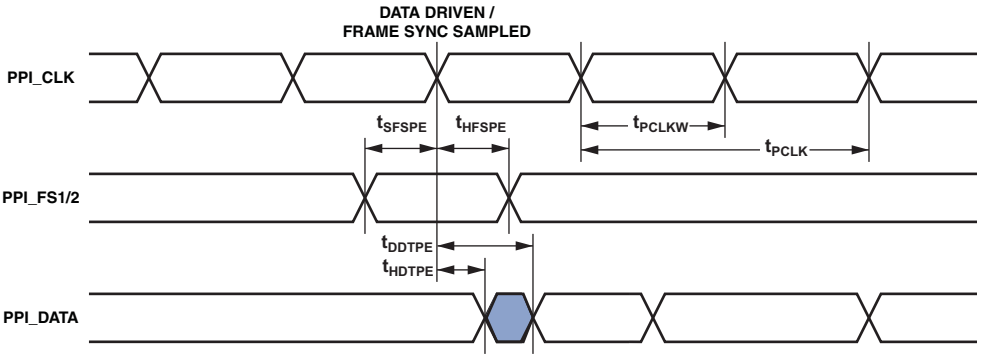


Figure 19. PPI GP Tx Mode with External Frame Sync Timing

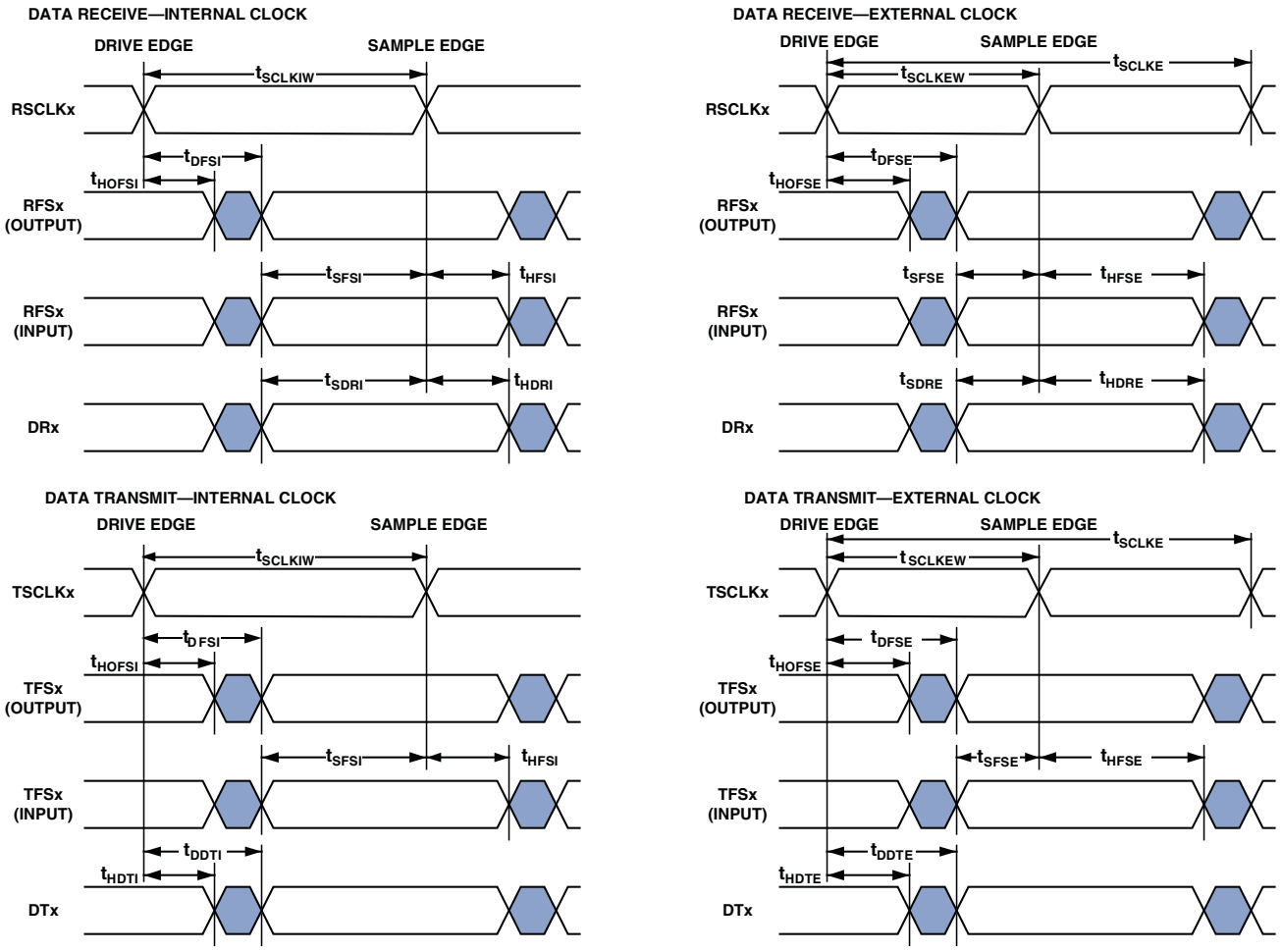


Figure 20. Serial Ports

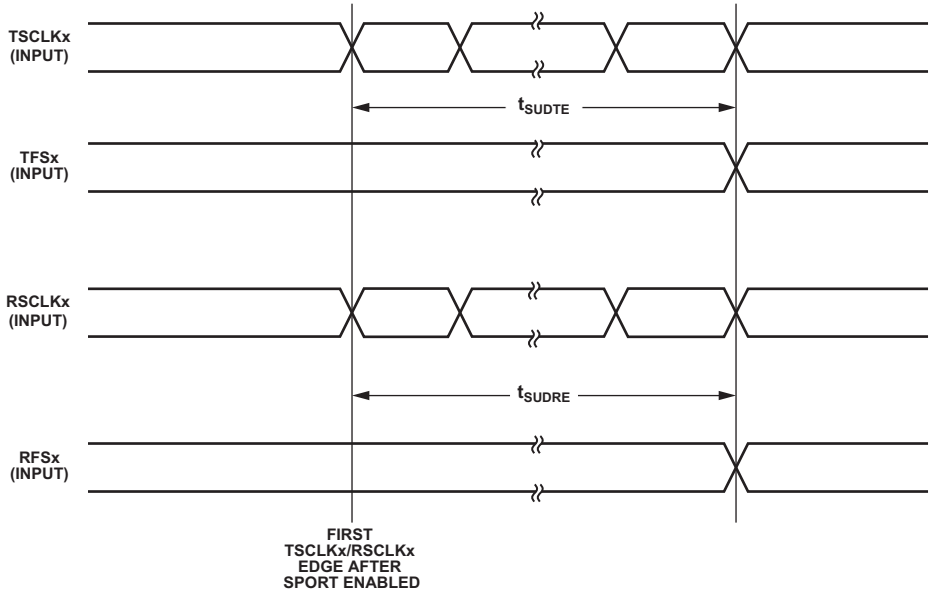


Figure 21. Serial Port Start Up with External Clock and Frame Sync

Serial Peripheral Interface Port—Master Timing

Table 34 and Figure 24 describe SPI port master operations.

Table 34. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		$2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1] Min	Max	$2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3] Min	Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	8.7		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	−1.5		−1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISEL}$x Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISEL}$x High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	−1.0		−1.0		ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.

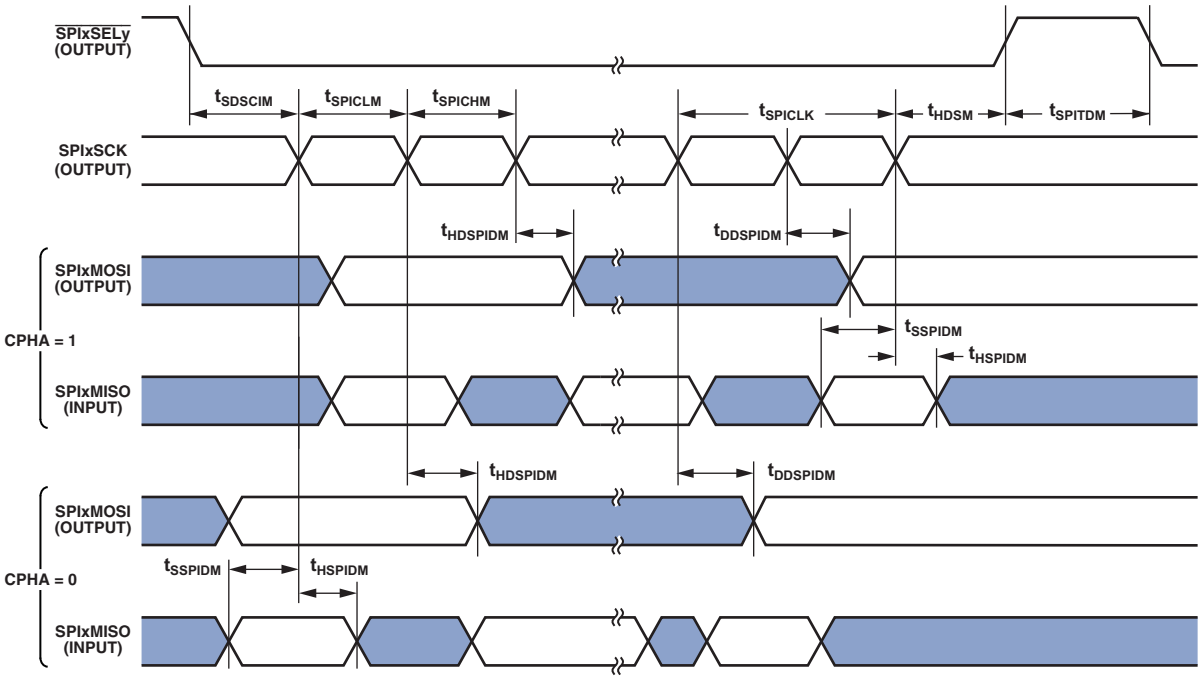


Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

Timer Clock Timing

Table 37 and Figure 27 describe timer clock timing.

Table 37. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		12	ns

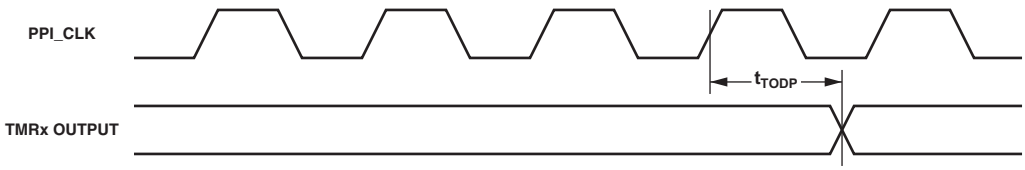


Figure 27. Timer Clock Timing

Timer Cycle Timing

Table 38 and Figure 28 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 38. Timer Cycle Timing

Parameter		2.25 V ≤ V_{DDEXT} < 2.70 V or 0.80 V ≤ V_{DDINT} < 0.95 V[1]		2.70 V ≤ V_{DDEXT} ≤ 3.60 V and 0.95 V ≤ V_{DDINT} ≤ 1.43 V[2, 3]		Unit
		Min	Max	Min	Max	
Timing Characteristics						
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK Cycles)[4]	1 × t_{SCLK}		1 × t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK Cycles)[4]	1 × t_{SCLK}		1 × t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[5]	5.5		5.0		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[5]	1.5		1.5		ns
Switching Characteristics						
t_{HTO}	Timer Pulse Width Output (Measured In SCLK Cycles)	1 × t_{SCLK}	(2^{32}–1) × t_{SCLK}	1 × t_{SCLK}	(2^{32}–1) × t_{SCLK}	ns
t_{TOD}	Timer Output Update Delay After CLKOUT High		6.5		6.0	ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.
[4] The minimum pulse widths apply for TMRx signals in width capture and external clock modes. They also apply to the PF15 or PPI_CLK signals in PWM output mode.
[5] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize programmable flag inputs.

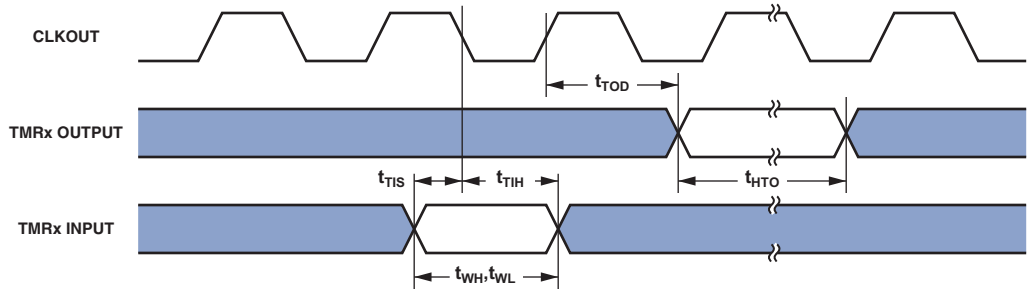
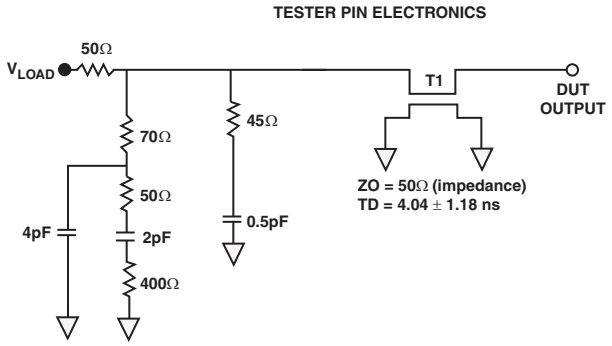


Figure 28. Timer Cycle Timing

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 50). Figure 51 through Figure 60 on Page 55 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

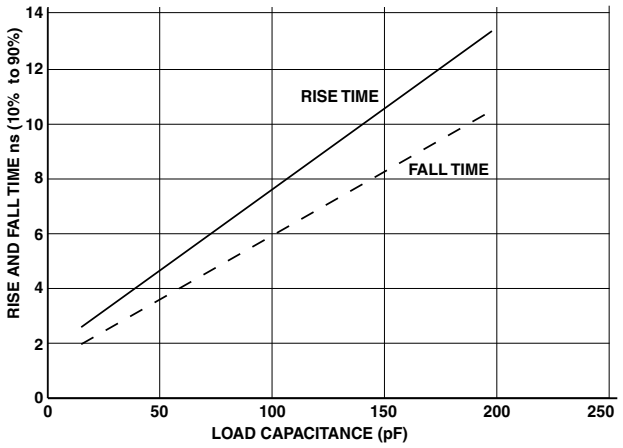


Figure 51. Typical Output Delay or Hold for Driver A at V_{DDEXT} Min

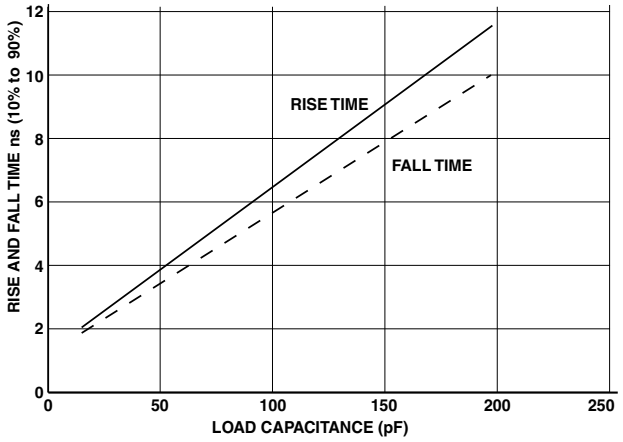


Figure 52. Typical Output Delay or Hold for Driver A at V_{DDEXT} Max

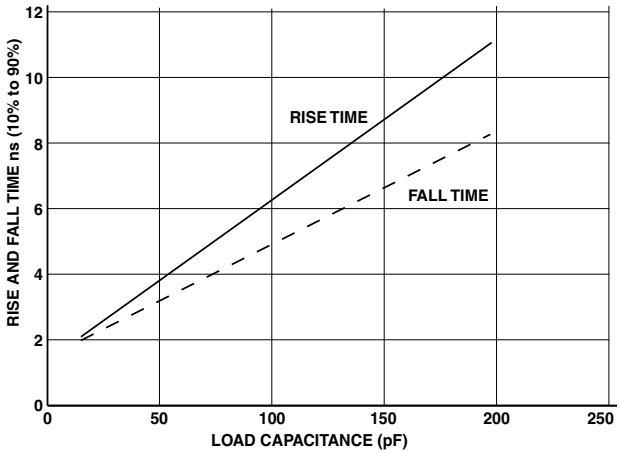


Figure 53. Typical Output Delay or Hold for Driver B at V_{DDEXT} Min

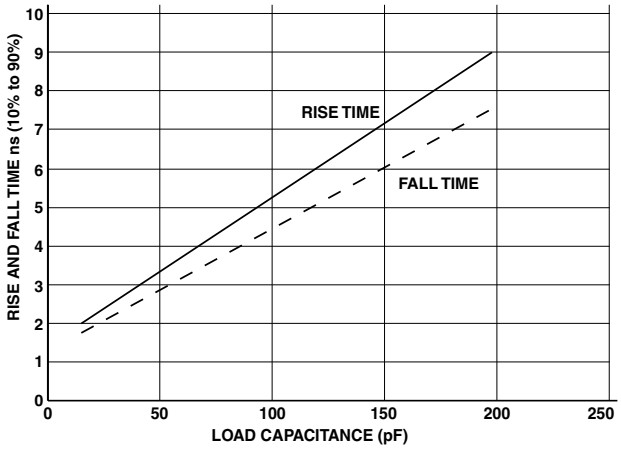


Figure 54. Typical Output Delay or Hold for Driver B at V_{DDEXT} Max

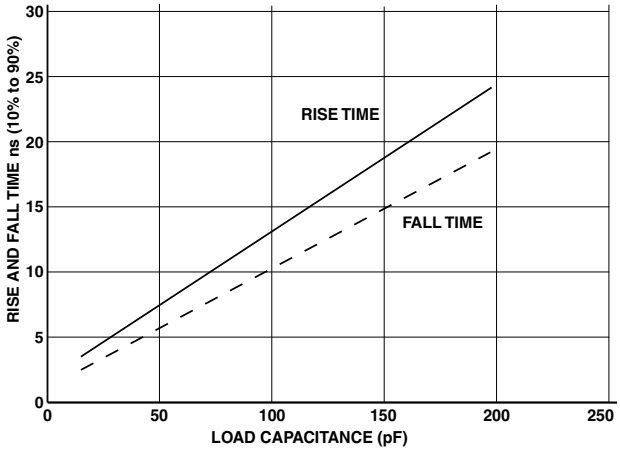


Figure 55. Typical Output Delay or Hold for Driver C at V_{DDEXT} Min

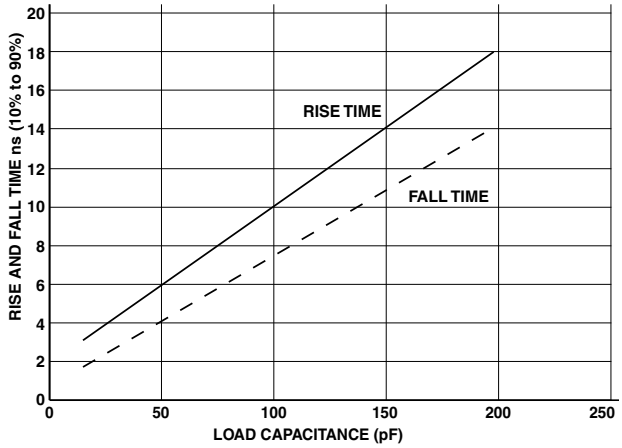


Figure 56. Typical Output Delay or Hold for Driver C at V_{DDEXT} Max

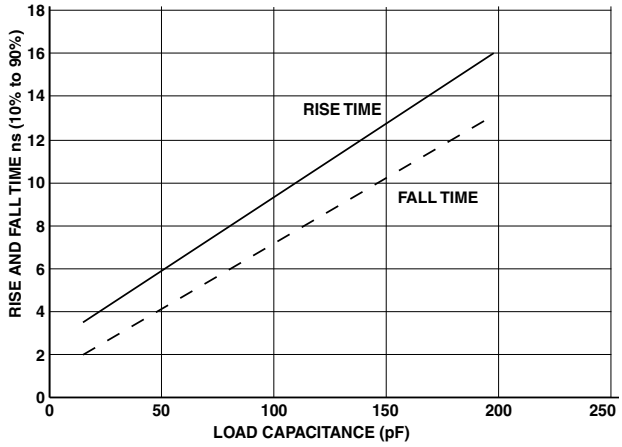


Figure 57. Typical Output Delay or Hold for Driver D at V_{DDEXT} Min

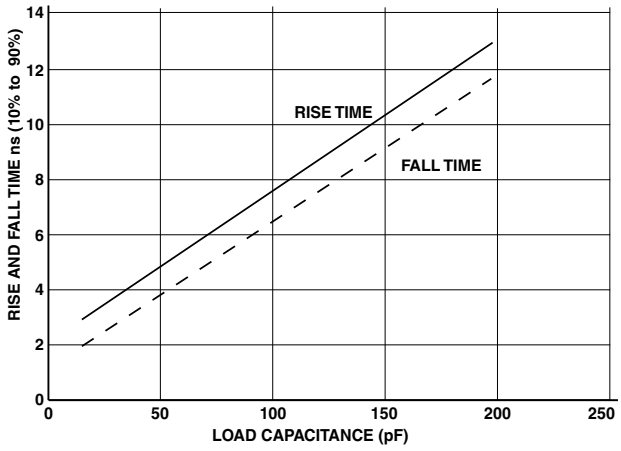


Figure 58. Typical Output Delay or Hold for Driver D at V_{DDEXT} Max

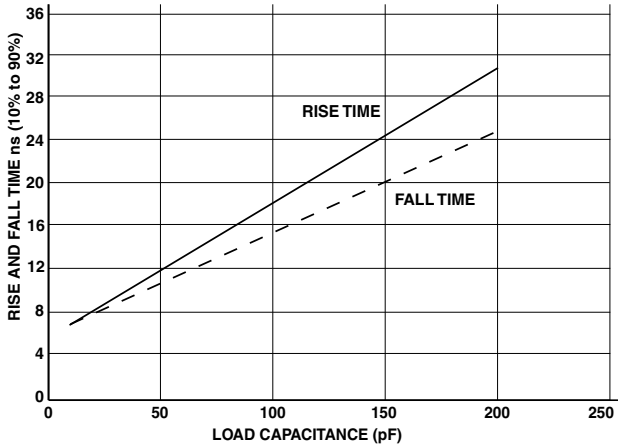


Figure 59. Typical Output Delay or Hold for Driver E at V_{DDEXT} Min

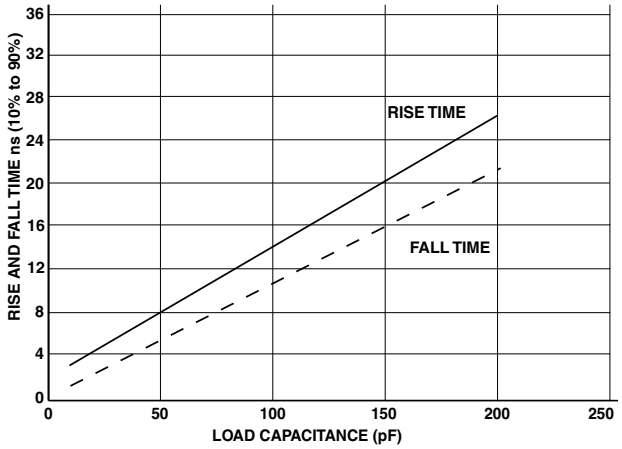


Figure 60. Typical Output Delay or Hold for Driver E at V_{DDEXT} Max

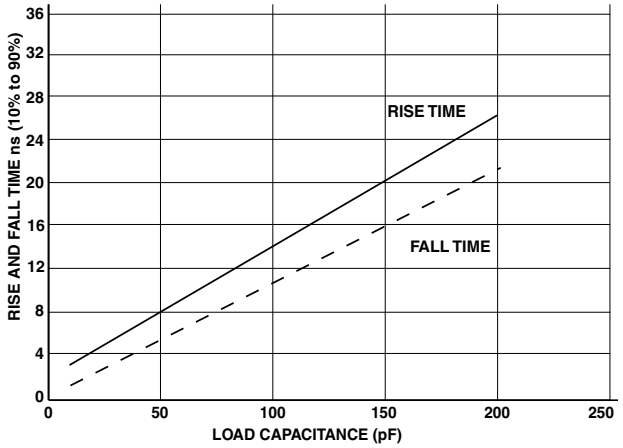


Figure 61. Typical Output Delay or Hold for Driver F at V_{DDEXT} Min

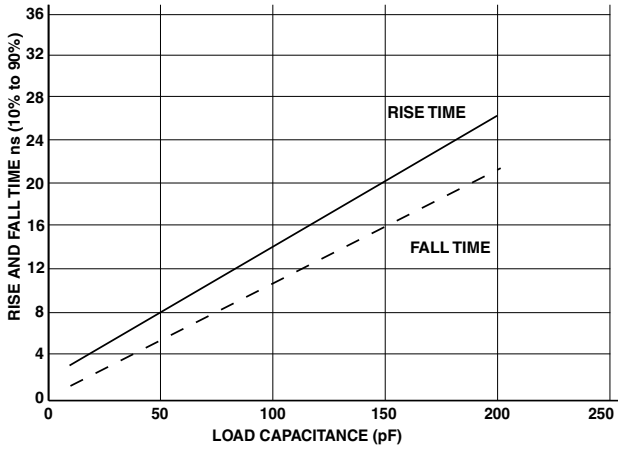


Figure 62. Typical Output Delay or Hold for Driver F at V_{DDEXT} Max

Table 52 lists the CSP_BGA ball assignment by ball number. Table 51 on Page 60 lists the CSP_BGA ball assignment by signal mnemonic.

Table 52. 208-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	GND	C19	PJ11	J9	GND	M19	$\overline{AMS1}$	W1	TCK
A2	PG12	C20	$\overline{NMI}$	J10	GND	M20	$\overline{AMS0}$	W2	GND
A3	PG13	D1	PG7	J11	GND	N1	PF5	W3	DATA15
A4	PG15	D2	PG8	J12	GND	N2	PF6	W4	DATA13
A5	PH1	D19	PJ2	J13	GND	N7	V_{DDEXT}	W5	DATA11
A6	PH3	D20	$\overline{RESET}$	J14	V_{DDINT}	N8	V_{DDEXT}	W6	DATA9
A7	PH5	E1	PG5	J19	ARDY	N9	GND	W7	DATA7
A8	PH7	E2	PG6	J20	$\overline{SMS}$	N10	GND	W8	DATA5
A9	PH9	E19	PJ3	K1	PF11	N11	GND	W9	DATA3
A10	PH11	E20	VROUT0	K2	PF12	N12	GND	W10	DATA1
A11	PH13	F1	PG3	K7	V_{DDEXT}	N13	GND	W11	BMODE2
A12	PH15	F2	PG4	K8	V_{DDEXT}	N14	V_{DDINT}	W12	BMODE1
A13	GND	F19	$\overline{BR}$	K9	GND	N19	$\overline{ARE}$	W13	BMODE0
A14	RTXI	F20	VROUT1	K10	GND	N20	$\overline{AOE}$	W14	ADDR18
A15	RTXO	G1	PG1	K11	GND	P1	PF3	W15	ADDR16
A16	V_{DDRTC}	G2	PG2	K12	GND	P2	PF4	W16	ADDR14
A17	XTAL	G7	V_{DDEXT}	K13	GND	P7	V_{DDEXT}	W17	ADDR12
A18	CLKIN	G8	V_{DDEXT}	K14	V_{DDINT}	P8	V_{DDEXT}	W18	ADDR10
A19	PJ5	G9	V_{DDEXT}	K19	$\overline{SRAS}$	P9	V_{DDEXT}	W19	GND
A20	GND	G10	V_{DDEXT}	K20	$\overline{SCAS}$	P10	V_{DDEXT}	W20	ADDR8
B1	PG11	G11	GND	L1	PF9	P11	GND	Y1	GND
B2	GND	G12	V_{DDINT}	L2	PF10	P12	V_{DDINT}	Y2	TDO
B3	PG14	G13	V_{DDINT}	L7	V_{DDEXT}	P13	V_{DDINT}	Y3	DATA14
B4	PH0	G14	V_{DDINT}	L8	V_{DDEXT}	P14	V_{DDINT}	Y4	DATA12
B5	PH2	G19	$\overline{AMS3}$	L9	GND	P19	$\overline{ABE0}$	Y5	DATA10
B6	PH4	G20	$\overline{AMS2}$	L10	GND	P20	$\overline{ABE1}$	Y6	DATA8
B7	PH6	H1	PF15	L11	GND	R1	PF1	Y7	DATA6
B8	PH8	H2	PG0	L12	GND	R2	PF2	Y8	DATA4
B9	PH10	H7	V_{DDEXT}	L13	GND	R19	ADDR1	Y9	DATA2
B10	PH12	H8	V_{DDEXT}	L14	V_{DDINT}	R20	$\overline{AWE}$	Y10	DATA0
B11	PH14	H9	GND	L19	$\overline{SWE}$	T1	$\overline{EMU}$	Y11	$\overline{BG}$
B12	PJ0	H10	GND	L20	SA10	T2	PF0	Y12	$\overline{BGH}$
B13	PJ1	H11	GND	M1	PF7	T19	ADDR3	Y13	GND
B14	CLKBUF	H12	GND	M2	PF8	T20	ADDR2	Y14	ADDR19
B15	PJ6	H13	GND	M7	V_{DDEXT}	U1	$\overline{TRST}$	Y15	ADDR17
B16	PJ7	H14	V_{DDINT}	M8	V_{DDEXT}	U2	TMS	Y16	ADDR15
B17	PJ8	H19	CLKOUT	M9	GND	U19	ADDR5	Y17	ADDR13
B18	PJ4	H20	SCKE	M10	GND	U20	ADDR4	Y18	ADDR11
B19	PJ10	J1	PF13	M11	GND	V1	TDI	Y19	ADDR9
B20	PJ9	J2	PF14	M12	GND	V2	GND	Y20	GND
C1	PG9	J7	V_{DDEXT}	M13	GND	V19	ADDR7		
C2	PG10	J8	V_{DDEXT}	M14	V_{DDINT}	V20	ADDR6		