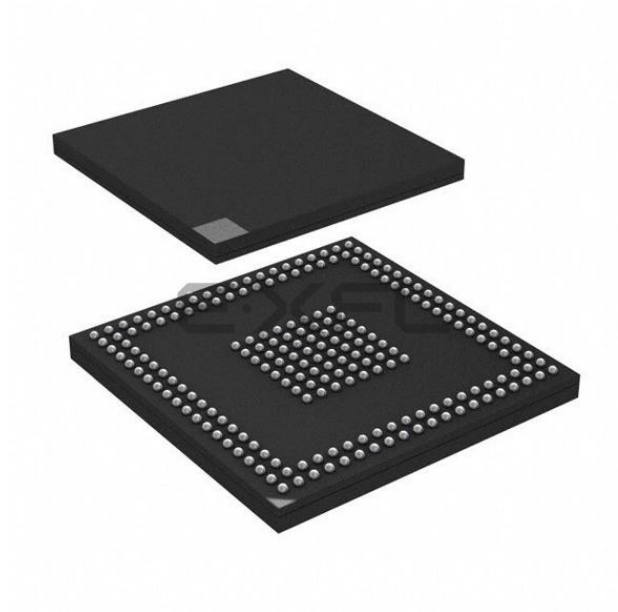

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	100kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf536bbcz-3b

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the Blackfin processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 Is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (IAR). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
PLL Wakeup	IVG7	0
DMA Error (Generic)	IVG7	1
DMAR0 Block Interrupt	IVG7	1
DMAR1 Block Interrupt	IVG7	1
DMAR0 Overflow Error	IVG7	1
DMAR1 Overflow Error	IVG7	1
CAN Error	IVG7	2
Ethernet Error (ADSP-BF536 and ADSP-BF537 only)	IVG7	2
SPORT 0 Error	IVG7	2
SPORT 1 Error	IVG7	2
PPI Error	IVG7	2
SPI Error	IVG7	2
UART0 Error	IVG7	2
UART1 Error	IVG7	2
Real-Time Clock	IVG8	3
DMA Channel 0 (PPI)	IVG8	4
DMA Channel 3 (SPORT 0 Rx)	IVG9	5
DMA Channel 4 (SPORT 0 Tx)	IVG9	6
DMA Channel 5 (SPORT 1 Rx)	IVG9	7
DMA Channel 6 (SPORT 1 Tx)	IVG9	8
TWI	IVG10	9
DMA Channel 7 (SPI)	IVG10	10
DMA Channel 8 (UART0 Rx)	IVG10	11
DMA Channel 9 (UART0 Tx)	IVG10	12
DMA Channel 10 (UART1 Rx)	IVG10	13
DMA Channel 11 (UART1 Tx)	IVG10	14
CAN Rx	IVG11	15
CAN Tx	IVG11	16
DMA Channel 1 (Ethernet Rx, ADSP-BF536 and ADSP-BF537 only)	IVG11	17
Port H Interrupt A	IVG11	17
DMA Channel 2 (Ethernet Tx, ADSP-BF536 and ADSP-BF537 only)	IVG11	18
Port H Interrupt B	IVG11	18
Timer 0	IVG12	19
Timer 1	IVG12	20
Timer 2	IVG12	21
Timer 3	IVG12	22
Timer 4	IVG12	23
Timer 5	IVG12	24
Timer 6	IVG12	25
Timer 7	IVG12	26
Port F, G Interrupt A	IVG12	27
Port G Interrupt B	IVG12	28

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors also have an external DMA controller capability via dual external DMA request pins when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals such as USB 2.0. It allows control of the number of data transfers for memDMA. The number of transfers per edge is programmable. This feature can be programmed to allow memDMA to have an increased priority on the external bus relative to the core.

REAL-TIME CLOCK

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day, while the second alarm is for a day and time of that day.

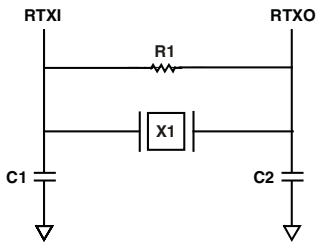
The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wake-up event. Additionally, an RTC wake-up event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from the hibernate operating mode.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 4.

WATCHDOG TIMER

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 4. External Components for RTC

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the processor. Eight timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic interrupts in an operating system.

- Programmable Rx address filters, including a 64-bit address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames.
- Advanced power management supporting unattended transfer of Rx and Tx frames and status to/from external memory via DMA during low power sleep mode.
- System wake-up from sleep operating mode upon magic packet or any of four user-definable wake-up frame filters.
- Support for 802.3Q tagged VLAN frames.
- Programmable MDC clock rate and preamble suppression.
- In RMII operation, 7 unused pins can be configured as GPIO pins for other purposes.

PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors group the many peripheral signals to four ports—Port F, Port G, Port H, and Port J. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Eight of the pins (Port F7–0) offer high source/high sink current capabilities.

General-Purpose I/O (GPIO)

The processors have 48 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Port J does not provide GPIO functionality. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output or input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processors employ a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode – Frame syncs and data are inputs into the PPI.
2. Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all of the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by writing b#00 to the FREQ bits of the VR_CTL register. This disables both CCLK and SCLK. Furthermore, it sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings. To preserve the processor state, prior to removing power, any critical information stored internally (memory contents, register contents, etc.) must be written to a nonvolatile storage device.

Since V_{DDEXT} is still supplied in this state, all of the external pins three-state, unless otherwise specified. This allows other devices that are connected to the processor to still have power applied without drawing unwanted current.

The Ethernet or CAN modules can wake up the internal supply regulator. If the PH6 pin does not connect as the $\overline{\text{PHYINT}}$ signal to an external PHY device, it can be pulled low by any other device to wake the processor up. The regulator can also be woken up by a real-time clock wake-up event or by asserting the $\overline{\text{RESET}}$ pin. All hibernate wake-up events initiate the hardware reset sequence. Individual sources are enabled by the VR_CTL register.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in the hibernate state. State variables can be held in external SRAM or SDRAM. The SCKELOW bit in the VR_CTL register provides a means of waking from hibernate state without disrupting a self-refreshing SDRAM, provided that there is also an external pull-down on the SCKE pin.

Power Savings

As shown in Table 5, the processors support three different power domains which maximizes flexibility, while maintaining compliance with industry standards and conventions. By isolating the internal logic of the processor into its own power domain, separate from the RTC and other I/O, the processor can take advantage of dynamic power management, without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	V_{DD} Range
All internal logic, except RTC	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
All other I/O	V_{DDEXT}

The dynamic power management feature allows both the processor's input voltage (V_{DDINT}) and clock frequency (f_{CCLK}) to be dynamically controlled.

The power dissipated by a processor is largely a function of its clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in power dissipation, while reducing the voltage by 25% reduces power dissipation by more than 40%. Further, these power savings are additive, in that if the clock frequency and supply voltage are both reduced, the power savings can be dramatic, as shown in the following equations.

The power savings factor (PSF) is calculated as:

$$PSF = \frac{f_{CCLKRED}}{f_{CCLKNOM}} \times \left(\frac{V_{DDINTRED}}{V_{DDINTNOM}}\right)^2 \times \left(\frac{t_{RED}}{t_{NOM}}\right)$$

where:

$f_{CCLKNOM}$ is the nominal core clock frequency

$f_{CCLKRED}$ is the reduced core clock frequency

$V_{DDINTNOM}$ is the nominal internal supply voltage

$V_{DDINTRED}$ is the reduced internal supply voltage

t_{NOM} is the duration running at $f_{CCLKNOM}$

t_{RED} is the duration running at $f_{CCLKRED}$

The percent power savings is calculated as

$$\%\ power\ savings = (1 - PSF) \times 100\%$$

VOLTAGE REGULATION

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide an on-chip voltage regulator that can generate appropriate V_{DDINT} voltage levels from the V_{DDEXT} supply. See Operating Conditions on Page 23 for regulator tolerances and acceptable V_{DDEXT} ranges for specific models.

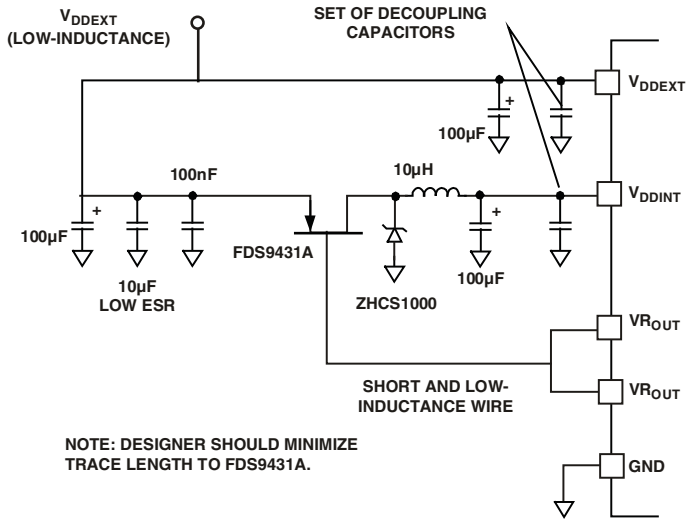


Figure 5. Voltage Regulator Circuit

Figure 5 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/UART1–0/Timer7–0/SPI/ External DMA Request/PPI (= High Source/High Sink Pin)*			
PF0* – GPIO/*UART0 TX/DMAR0*	I/O	GPIO/*UART0 Transmit/DMA Request 0*	C
PF1* – GPIO/*UART0 RX/DMAR1/TACI1*	I/O	GPIO/*UART0 Receive/DMA Request 1/Timer1 Alternate Input Capture*	C
PF2* – GPIO/*UART1 TX/TMR7*	I/O	GPIO/*UART1 Transmit/Timer7*	C
PF3* – GPIO/*UART1 RX/TMR6/TACI6*	I/O	GPIO/*UART1 Receive/Timer6/Timer6 Alternate Input Capture*	C
PF4* – GPIO/*TMR5/SPI SSEL6*	I/O	GPIO/*Timer5/SPI Slave Select Enable 6*	C
PF5* – GPIO/*TMR4/SPI SSEL5*	I/O	GPIO/*Timer4/SPI Slave Select Enable 5*	C
PF6* – GPIO/*TMR3/SPI SSEL4*	I/O	GPIO/*Timer3/SPI Slave Select Enable 4*	C
PF7* – GPIO/*TMR2/PPI FS3*	I/O	GPIO/*Timer2/PPI Frame Sync 3*	C
PF8 – GPIO/*TMR1/PPI FS2*	I/O	GPIO/*Timer1/PPI Frame Sync 2*	C
PF9 – GPIO/*TMR0/PPI FS1*	I/O	GPIO/*Timer0/PPI Frame Sync 1*	C
PF10 – GPIO/*SPI SSEL1*	I/O	GPIO/*SPI Slave Select Enable 1*	C
PF11 – GPIO/*SPI MOSI*	I/O	GPIO/*SPI Master Out Slave In*	C
PF12 – GPIO/*SPI MISO*	I/O	GPIO/*SPI Master In Slave Out* (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
PF13 – GPIO/*SPI SCK*	I/O	GPIO/*SPI Clock*	D
PF14 – GPIO/*SPI SS/TACLK0*	I/O	GPIO/*SPI Slave Select/Alternate Timer0 Clock Input*	C
PF15 – GPIO/*PPI CLK/TMRCLK*	I/O	GPIO/*PPI Clock/External Timer Reference*	C
Port G: GPIO/PPI/SPORT1			
PG0 – GPIO/*PPI D0*	I/O	GPIO/*PPI Data 0*	C
PG1 – GPIO/*PPI D1*	I/O	GPIO/*PPI Data 1*	C
PG2 – GPIO/*PPI D2*	I/O	GPIO/*PPI Data 2*	C
PG3 – GPIO/*PPI D3*	I/O	GPIO/*PPI Data 3*	C
PG4 – GPIO/*PPI D4*	I/O	GPIO/*PPI Data 4*	C
PG5 – GPIO/*PPI D5*	I/O	GPIO/*PPI Data 5*	C
PG6 – GPIO/*PPI D6*	I/O	GPIO/*PPI Data 6*	C
PG7 – GPIO/*PPI D7*	I/O	GPIO/*PPI Data 7*	C
PG8 – GPIO/*PPI D8/DR1SEC*	I/O	GPIO/*PPI Data 8/SPORT1 Receive Data Secondary*	C
PG9 – GPIO/*PPI D9/DT1SEC*	I/O	GPIO/*PPI Data 9/SPORT1 Transmit Data Secondary*	C
PG10 – GPIO/*PPI D10/RSCLK1*	I/O	GPIO/*PPI Data 10/SPORT1 Receive Serial Clock*	D
PG11 – GPIO/*PPI D11/RFS1*	I/O	GPIO/*PPI Data 11/SPORT1 Receive Frame Sync*	C
PG12 – GPIO/*PPI D12/DR1PRI*	I/O	GPIO/*PPI Data 12/SPORT1 Receive Data Primary*	C
PG13 – GPIO/*PPI D13/TSCLK1*	I/O	GPIO/*PPI Data 13/SPORT1 Transmit Serial Clock*	D
PG14 – GPIO/*PPI D14/TFS1*	I/O	GPIO/*PPI Data 14/SPORT1 Transmit Frame Sync*	C
PG15 – GPIO/*PPI D15/DT1PRI*	I/O	GPIO/*PPI Data 15/SPORT1 Transmit Data Primary*	C

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 300 MHz, 400 MHz, and 500 MHz speed grade models[2]	0.8	1.2	1.32	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 600 MHz speed grade models[2]	0.8	1.3	1.43	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive grade models and +105°C nonautomotive grade models[2]	0.95	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Nonautomotive grade models[2]	2.25	2.5 or 3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models and +105°C nonautomotive grade models[2]	2.7	3.0 or 3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[3, 4]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.2			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[6]		$0.7 \times V_{DDEXT}$			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[7]	V_{DDEXT} = Maximum	2.0			V
V_{IL}	Low Level Input Voltage[3, 8]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[6]				$0.3 \times V_{DDEXT}$	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[7]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+120	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance. The required V_{DDINT} is a function of speed grade and operating frequency. See Table 10, Table 11, and Table 12 for details.

[2] See Ordering Guide on Page 67.

[3] Bidirectional pins (DATA15–0, PF15–0, PG15–0, PH15–0, TFS0, TSCLK0, RSCLK0, RFS0, MDIO) and input pins ($\overline{BR}$, ARDY, DR0PRI, DR0SEC, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF534/ADSP-BF536/ADSP-BF537 are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[4] Parameter value applies to all input and bidirectional pins except CLKIN, SDA, and SCL.

[5] Parameter value applies to CLKIN pin only.

[6] Applies to pins PJ2/SCL and PJ3/SDA which are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[7] Applies to pin PJ4/DR0SEC/CANRX/TACI0 which is 5.0 V tolerant (always accepts up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Parameter value applies to all input and bidirectional pins except SDA and SCL.

Table 10 through Table 12 describe the voltage/frequency requirements for the ADSP-BF534/ADSP-BF536/ADSP-BF537 processor clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 13 describes phase-locked loop operating conditions.

Table 10. Core Clock Requirements—500 MHz, 533 MHz, and 600 MHz Speed Grades[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.30 V Minimum)[2]	1.30 V	600	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.20 V Minimum)[3]	1.25 V	533	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	500	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	444	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	250	MHz

[1] See Ordering Guide on Page 67.
[2] Applies to 600 MHz models only. See Ordering Guide on Page 67.
[3] Applies to 533 MHz and 600 MHz models only. See Ordering Guide on Page 67.

Table 11. Core Clock Requirements—400 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	120°C ≥ T_J > 105°C Max	All[2] Other T_J Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	400	400	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	333	363	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	295	333	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V		280	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V		250	MHz

[1] See Ordering Guide on Page 67.
[2] See Operating Conditions on Page 23.

Table 12. Core Clock Requirements—300 MHz Speed Grade[1]

Parameter		Internal Regulator Setting	Max	Unit
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.14 V Minimum)	1.20 V	300	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 1.045 V Minimum)	1.10 V	255	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.95 V Minimum)	1.00 V	210	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.85 V Minimum)	0.90 V	180	MHz
f_{CCLK}	Core Clock Frequency (V_{DDINT} = 0.8 V Minimum)	0.85 V	160	MHz

[1] See Ordering Guide on Page 67.

Table 13. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Max f_{CCLK}	MHz

Table 14. System Clock Requirements

Parameter	Condition	Max	Unit
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, V_{DDINT} ≥ 1.14 V	133[2]	MHz
f_{SCLK}[1]	V_{DDEXT} = 3.3 V or 2.5 V, V_{DDINT} < 1.14 V	100	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK} and is subject to additional restrictions for SDRAM interface operation. See Table 27 on Page 34.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 27 on Page 34.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
V_{OH}[3]	High Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –2.0 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
I_{OH}[6]	High Level Output Current	V_{OH} = V_{DDEXT} – 0.5 V Min			–64			–64	mA
I_{OH}[7]		V_{OH} = V_{DDEXT} – 0.5 V Min			–144			–144	mA
V_{OL}[3]	Low Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA			0.5			0.5	V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OL} = 6 mA			0.5			0.5	V
V_{OL}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.5			0.5	V
I_{OL}[6]	Low Level Output Current	V_{OL} = 0.5 V Max			64			64	mA
I_{OL}[7]		V_{OL} = 0.5 V Max			144			144	mA
I_{IH}	High Level Input Current[8]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{IH5V}	High Level Input Current[9]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{IL}	Low Level Input Current[2]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA
I_{IHP}	High Level Input Current JTAG[10]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			50			50	µA
I_{OZH}	Three-State Leakage Current[11]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{OZH5V}	Three-State Leakage Current[12]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA

Table 17. Activity Scaling Factors

I_{DDINT} Power Vector[1]	Activity Scaling Factor (ASF)[2]
$I_{DD-PEAK}$	1.33
$I_{DD-HIGH}$	1.29
I_{DD-TYP}	1.00
I_{DD-APP}	0.88
I_{DD-NOP}	0.72
$I_{DD-IDLE}$	0.43

[1] See EE-297 for power vector definitions.
[2] All ASF values determined using a 10:1 CCLK:SCLK ratio.

Table 18. Dynamic Current (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})													
Frequency (MHz)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
50	11.0	13.7	19.13	18.2	18.67	19.13	19.6	21.2	24.1	25.5	28.5	28.6	28.85	29.2
100	27.9	22.7	30.8	28.4	29.3	30.8	32.9	35.3	37.8	40.6	43.5	43.7	44.1	45.8
200	36.9	42.6	55.0	49.2	51.5	55.0	58.3	62.9	67.0	69.7	73.0	74.0	75.7	80.7
300	N/A	61.5	79.2	70.4	74.6	79.2	84.4	90.7	94.3	99.1	103.9	105.5	108.0	113.4
400	N/A	N/A	N/A	92.4	97.2	104.3	109.8	116.5	121.9	128.0	134.6	136.6	139.8	145.1
500	N/A	N/A	N/A	N/A	N/A	N/A	N/A	142.3	149.3	157.5	164.7	166.7	169.8	176.9
533	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	158.6	167.0	174.3	176.6	180.1	187.9
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	193.7	196.5	200.7	210.0

[1] The values are not guaranteed as stand-alone maximum specifications, they must be combined with static current per the equations of Electrical Characteristics on Page 25.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 19 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 19. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	−0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	−0.3 V to +3.8 V
Input Voltage[1]	−0.5 V to +3.6 V
Input Voltage[1, 2]	−0.5 V to +5.5 V
Output Voltage Swing	−0.5 V to V_{DDEXT} + 0.5 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature While Biased	+125°C

[1] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.
[2] Applies to 5 V tolerant pins SCL, SDA, and PJ4. For duty cycles, see Table 20.

Table 20. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Min (V)[2]	V_{IN} Max (V)[2]	Maximum Duty Cycle[3]
−0.50	+3.80	100%
−0.70	+4.00	40%
−0.80	+4.10	25%
−0.90	+4.20	15%
−1.00	+4.30	10%

[1] Applies to all signal pins with the exception of CLKIN, XTAL, and VROUT1–0.
[2] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.
[3] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 8 and Table 21 provide details about the package branding for the Blackfin processors. For a complete listing of product availability, see Ordering Guide on Page 67.

Figure 8. Product Information on Package

Table 21. Package Brand Information[1]

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Designation
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

[1] Nonautomotive only. For branding information specific to Automotive products, contact Analog Devices Inc.

External Port Bus Request and Grant Cycle Timing

Table 26 and Figure 13 describe external port bus request and bus grant operations.

Table 26. External Port Bus Request and Grant Cycle Timing

Parameter[1, 2]		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT Low Setup	4.6		ns
t_{BH}	CLKOUT Low to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		4.5	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		4.5	ns
t_{DBG}	CLKOUT High to $\overline{BG}$ Asserted Setup		3.6	ns
t_{EBG}	CLKOUT High to $\overline{BG}$ Deasserted Hold Time		3.6	ns
t_{DBH}	CLKOUT High to $\overline{BGH}$ Asserted Setup		3.6	ns
t_{EBH}	CLKOUT High to $\overline{BGH}$ Deasserted Hold Time		3.6	ns

[1] These timing parameters are based on worst-case operating conditions.
[2] The pad loads for these timing parameters are 20 pF.

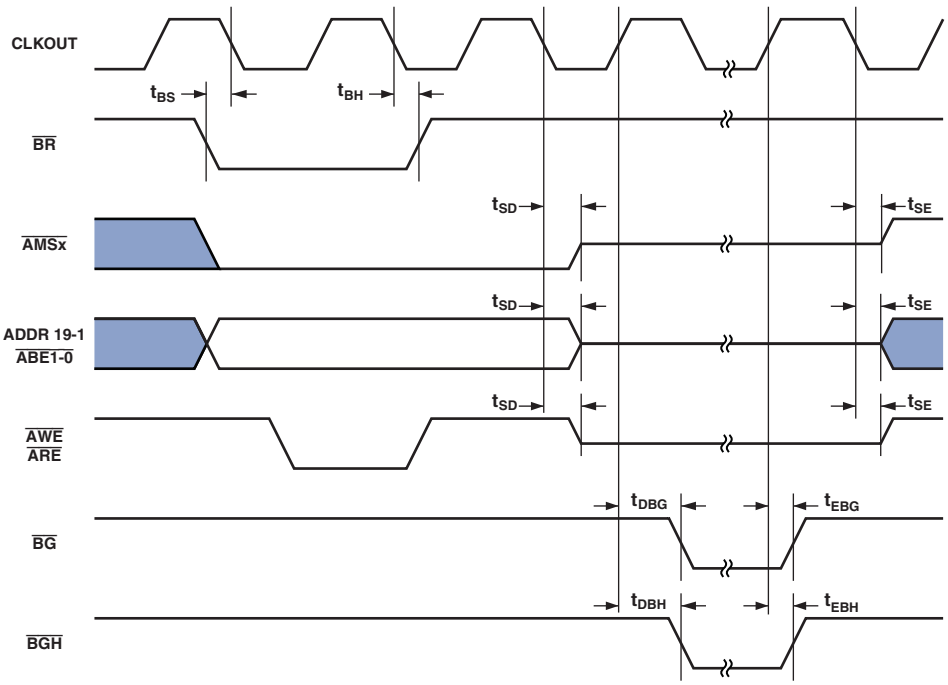


Figure 13. External Port Bus Request and Grant Cycle Timing

SDRAM Interface Timing

Table 27. SDRAM Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDAT}	DATA15–0 Setup Before CLKOUT	1.5		ns
t_{HSDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
Switching Characteristics				
t_{DCAD}	COMMAND[1], ADDR19–1, DATA15–0 Delay After CLKOUT		4.0	ns
t_{HCAD}	COMMAND[1], ADDR19–1, DATA15–0 Hold After CLKOUT	1.0		ns
t_{DSDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENSDAT}	DATA15–0 Enable After CLKOUT	0.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J \leq +105°C$	7.5		ns
t_{SCLK}[2]	CLKOUT Period when $T_J > +105°C$	10		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] Command pins include: $\overline{SRAS}$, $\overline{SCAS}$, $\overline{SWE}$, SDQM, $\overline{SMS}$, SA10, SCKE.
[2] These limits are specific to the SDRAM interface only. In addition, CLKOUT must always comply with the limits in Table 14 on Page 24.

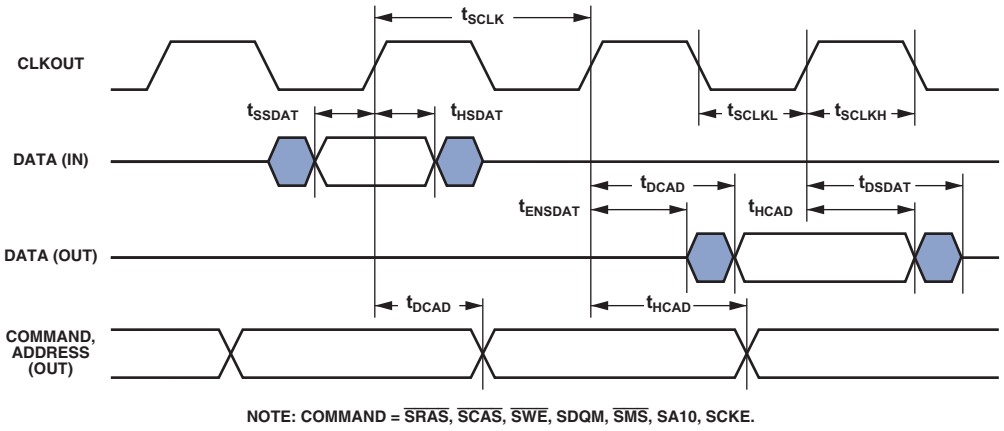


Figure 14. SDRAM Interface Timing

Serial Port Timing

Table 30 through Table 33 on Page 41 and Figure 20 on Page 39 through Figure 23 on Page 41 describe serial port operations.

Table 30. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	15.0		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx[2]	$4.0 \times t_{SCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx[2]	$4.0 \times t_{SCLKE}$		ns
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLK (Internally Generated TFSx/RFSx)[3]		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLK (Internally Generated TFSx/RFSx)[2]	0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[2]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[2]	0		ns

[1] Referenced to sample edge.
[2] Verified in design but untested. After being enabled, the serial port requires external clock pulses—before the first external frame sync edge—to initialize the serial port.
[3] Referenced to drive edge.

Table 31. Serial Ports—Internal Clock

Parameter		$2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1]		$2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3]		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx[4]	8.5		8.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx[4]	−1.5		−1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[4]	8.5		8.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[4]	−1.5		−1.5		ns
Switching Characteristics						
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[5]		3.0		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[5]	−1.0		−1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[5]		3.0		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[5]	−1.0		−1.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		4.5		ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.
[4] Referenced to sample edge.
[5] Referenced to drive edge.

Table 32. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2]		10.0	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2.0		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2]		3.0	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only. TSCLKx is tied to RSCLKx.

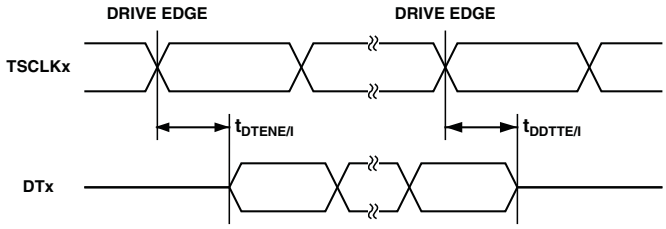


Figure 22. Enable and Three-State

Serial Peripheral Interface Port—Master Timing

Table 34 and Figure 24 describe SPI port master operations.

Table 34. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		$2.25\ V \le V_{DDEXT} < 2.70\ V$ or $0.80\ V \le V_{DDINT} < 0.95\ V$[1] Min	Max	$2.70\ V \le V_{DDEXT} \le 3.60\ V$ and $0.95\ V \le V_{DDINT} \le 1.43\ V$[2, 3] Min	Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SCK Edge (Data Input Setup)	8.7		7.5		ns
t_{HSPIDM}	SCK Sampling Edge to Data Input Invalid	−1.5		−1.5		ns
Switching Characteristics						
t_{SDSCIM}	$\overline{SPISEL}$x Low to First SCK Edge	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICHM}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLM}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK} - 1.5$		$4 \times t_{SCLK} - 1.5$		ns
t_{HDSM}	Last SCK Edge to $\overline{SPISEL}$x High	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDM}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		$2 \times t_{SCLK} - 1.5$		ns
$t_{DDSPIDM}$	SCK Edge to Data Out Valid (Data Out Delay)		6		6	ns
$t_{HDSPIDM}$	SCK Edge to Data Out Invalid (Data Out Hold)	−1.0		−1.0		ns

[1] Applies to all nonautomotive-grade devices when operated within either of these voltage ranges.
[2] Applies to all nonautomotive-grade devices when operated within these voltage ranges.
[3] All automotive-grade devices are within these specifications.

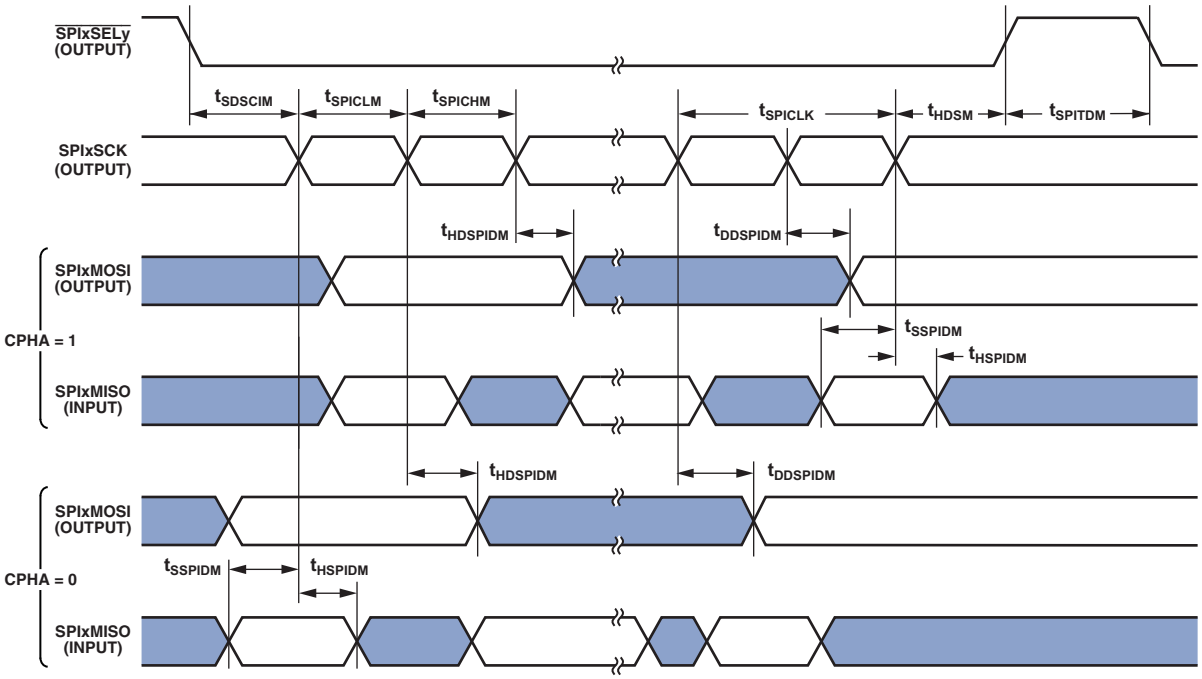


Figure 24. Serial Peripheral Interface (SPI) Port—Master Timing

JTAG Test and Emulation Port Timing

Table 39 and Figure 29 describe JTAG port operations.

Table 39. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay From TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA15–0, $\overline{\text{BR}}$, ARDY, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH15–0, MDIO, TCK, $\overline{\text{TRST}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, RTXI, BMODE2–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{\text{ABE1–0}}$, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, SCL, SDA, MDC, MDIO, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH15–0, RTXO, TDO, $\overline{\text{EMU}}$, XTAL, VROUT1–0.

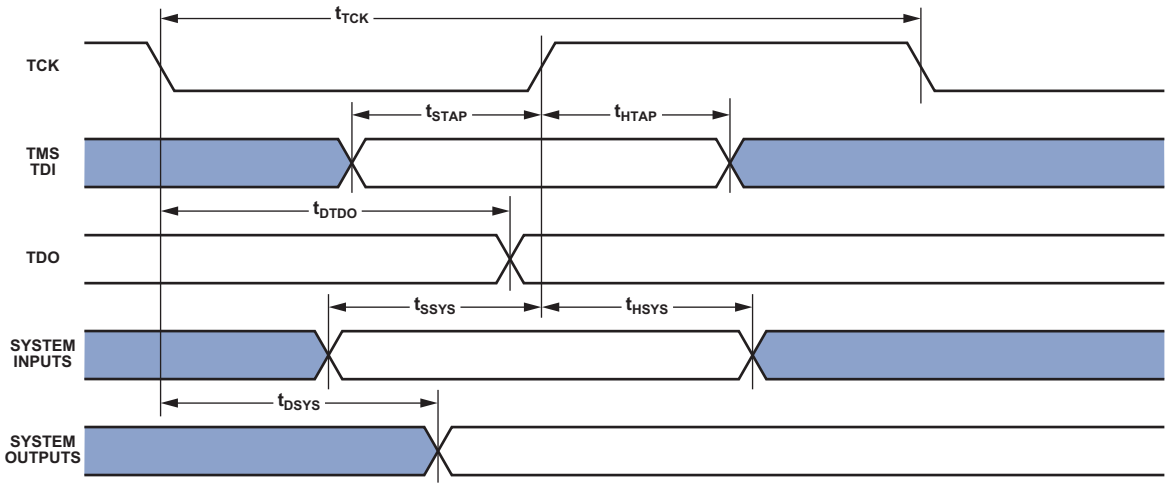


Figure 29. JTAG Port Timing

Table 44. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 45. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	10		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	10		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

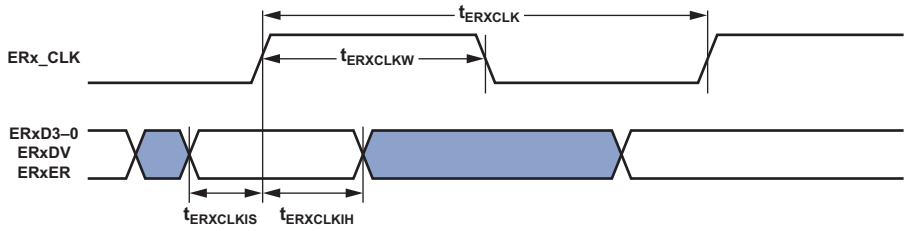


Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

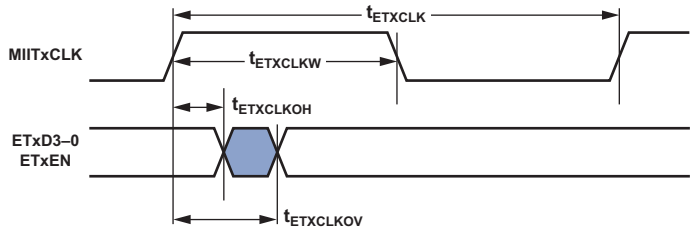


Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

OUTLINE DIMENSIONS

Dimensions in Figure 67 and Figure 68 are shown in millimeters.

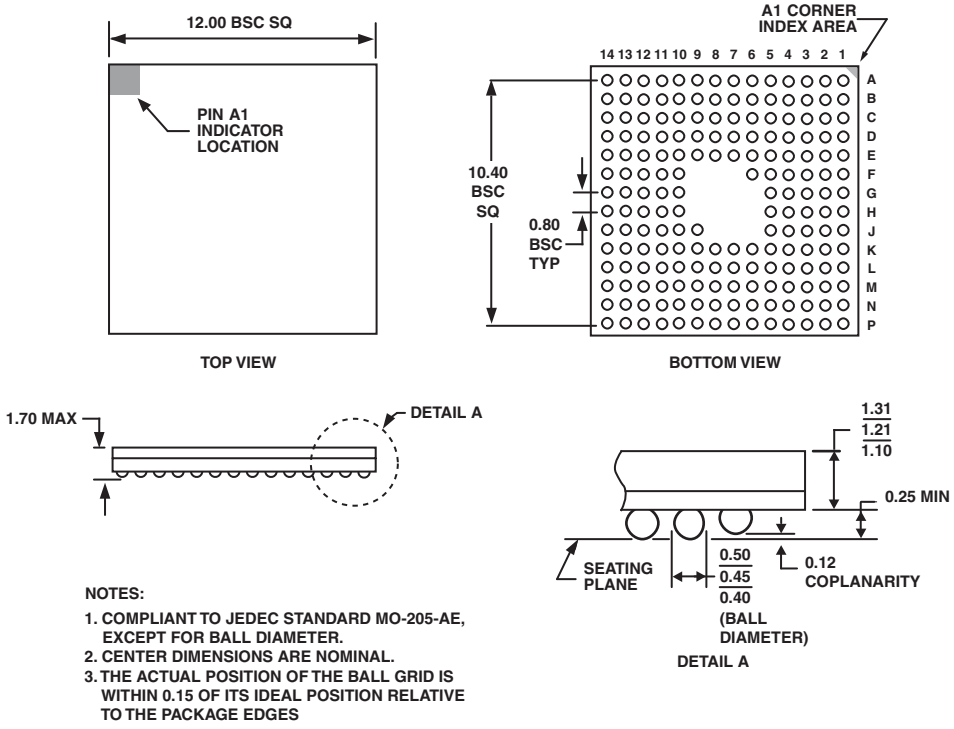


Figure 67. 182-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-182)
Dimensions shown in millimeters

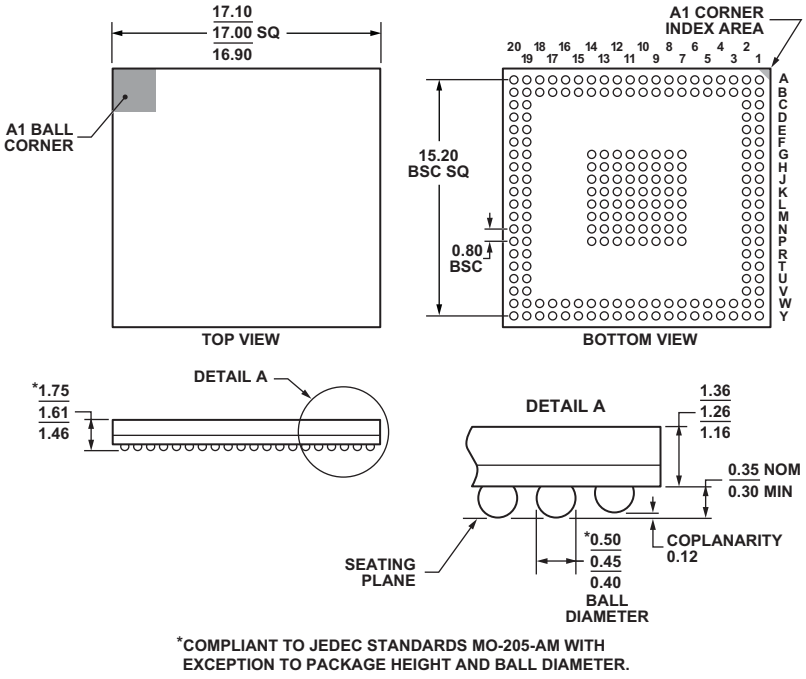


Figure 68. 208-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-208-2)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

The following table is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard.*

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
182-Ball CSP_BGA (BC-182)	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter
208-Ball CSP_BGA (BC-208-2)	Solder Mask Defined	0.40 mm diameter	0.55 mm diameter