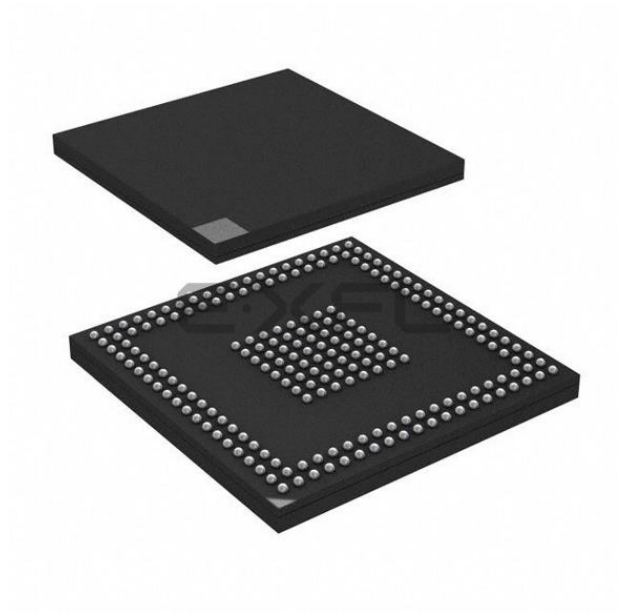

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	100kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf536bbcz3brl

In addition to the dedicated peripheral DMA channels, there are two memory DMA channels provided for transfers between the various memories of the processor system. This enables transfers of blocks of data between any of the memories—including external SDRAM, ROM, SRAM, and flash memory—with minimal processor intervention. Memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors also have an external DMA controller capability via dual external DMA request pins when used in conjunction with the external bus interface unit (EBIU). This functionality can be used when a high speed interface is required for external FIFOs and high bandwidth communications peripherals such as USB 2.0. It allows control of the number of data transfers for memDMA. The number of transfers per edge is programmable. This feature can be programmed to allow memDMA to have an increased priority on the external bus relative to the core.

REAL-TIME CLOCK

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the processor. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and an 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day, while the second alarm is for a day and time of that day.

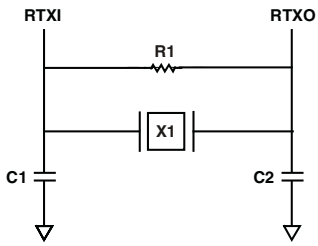
The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the processor from sleep mode upon generation of any RTC wake-up event. Additionally, an RTC wake-up event can wake up the processor from deep sleep mode, and wake up the on-chip internal voltage regulator from the hibernate operating mode.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 4.

WATCHDOG TIMER

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a system reset, nonmaskable interrupt (NMI), or general-purpose interrupt, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.



SUGGESTED COMPONENTS:
X1 = ECLIPTEK EC38J (THROUGH-HOLE PACKAGE) OR
EPSON MC405 12 pF LOAD (SURFACE-MOUNT PACKAGE)
C1 = 22 pF
C2 = 22 pF
R1 = 10 MΩ

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 4. External Components for RTC

If configured to generate a hardware reset, the watchdog timer resets both the core and the processor peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK), at a maximum frequency of f_{SCLK}.

TIMERS

There are nine general-purpose programmable timer units in the processor. Eight timers have an external pin that can be configured either as a pulse-width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input to the several other associated PF pins, to an external clock input to the PPI_CLK input pin, or to the internal SCLK.

The timer units can be used in conjunction with the two UARTs and the CAN controller to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core providing periodic events for synchronization, either to the system clock or to a count of external signals.

In addition to the eight general-purpose programmable timers, a ninth timer is also provided. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic interrupts in an operating system.

- Programmable Rx address filters, including a 64-bit address hash table for multicast and/or unicast frames, and programmable filter modes for broadcast, multicast, unicast, control, and damaged frames.
- Advanced power management supporting unattended transfer of Rx and Tx frames and status to/from external memory via DMA during low power sleep mode.
- System wake-up from sleep operating mode upon magic packet or any of four user-definable wake-up frame filters.
- Support for 802.3Q tagged VLAN frames.
- Programmable MDC clock rate and preamble suppression.
- In RMII operation, 7 unused pins can be configured as GPIO pins for other purposes.

PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors group the many peripheral signals to four ports—Port F, Port G, Port H, and Port J. Most of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Eight of the pins (Port F7–0) offer high source/high sink current capabilities.

General-Purpose I/O (GPIO)

The processors have 48 bidirectional, general-purpose I/O (GPIO) pins allocated across three separate GPIO modules—PORTFIO, PORTGIO, and PORTHIO, associated with Port F, Port G, and Port H, respectively. Port J does not provide GPIO functionality. Each GPIO-capable pin shares functionality with other processor peripherals via a multiplexing scheme; however, the GPIO functionality is the default state of the device upon power-up. Neither GPIO output or input drivers are active by default. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers:

- GPIO direction control register – Specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers – The processors employ a "write one to modify" mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins. Four control registers are provided. One register is written in order to set pin values, one register is written in order to clear pin values, one register is written in order to toggle pin values, and one register is written in order to specify a pin value. Reading the GPIO status register allows software to interrogate the sense of the pins.
- GPIO interrupt mask registers – The two GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processor. Similar to the two GPIO control registers that are used to set and clear individual pin values, one GPIO interrupt mask register sets bits to enable interrupt function, and the other GPIO interrupt mask register clears bits to disable interrupt function. GPIO pins defined as inputs can be configured to generate hardware interrupts, while output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers – The two GPIO interrupt sensitivity registers specify whether individual pins are level- or edge-sensitive and specify—if edge-sensitive—whether just the rising edge or both the rising and falling edges of the signal are significant. One register selects the type of sensitivity, and one register selects which edges are significant for edge-sensitivity.

PARALLEL PERIPHERAL INTERFACE (PPI)

The processor provides a parallel peripheral interface (PPI) that can connect directly to parallel ADC and DAC converters, video encoders and decoders, and other general-purpose peripherals. The PPI consists of a dedicated input clock pin, up to three frame synchronization pins, and up to 16 data pins. The input clock supports parallel data rates up to half the system clock rate and the synchronization signals can be configured as either inputs or outputs.

The PPI supports a variety of general-purpose and ITU-R 656 modes of operation. In general-purpose mode, the PPI provides half-duplex, bidirectional data transfer with up to 16 bits of data. Up to three frame synchronization signals are also provided. In ITU-R 656 mode, the PPI provides half-duplex bidirectional transfer of 8- or 10-bit video data. Additionally, on-chip decode of embedded start-of-line (SOL) and start-of-field (SOF) preamble packets is supported.

General-Purpose Mode Descriptions

The general-purpose modes of the PPI are intended to suit a wide variety of data capture and transmission applications. Three distinct submodes are supported:

1. Input mode – Frame syncs and data are inputs into the PPI.
2. Frame capture mode – Frame syncs are outputs from the PPI, but data are inputs.
3. Output mode – Frame syncs and data are outputs from the PPI.

Input Mode

Input mode is intended for ADC applications, as well as video communication with hardware signaling. In its simplest form, PPI_FS1 is an external frame sync input that controls when to read data. The PPI_DELAY MMR allows for a delay (in PPI_CLK cycles) between reception of this frame sync and the initiation of data reads. The number of input data samples is user programmable and defined by the contents of the PPI_COUNT register. The PPI supports 8-bit and 10-bit through 16-bit data, programmable in the PPI_CONTROL register.

Frame Capture Mode

Frame capture mode allows the video source(s) to act as a slave (for frame capture for example). The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors control when to read from the video source(s). PPI_FS1 is an HSYNC output and PPI_FS2 is a VSYNC output.

PIN DESCRIPTIONS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors pin definitions are listed in Table 9. In order to maintain maximum functionality and reduce package size and pin count, some pins have dual, multiplexed functions. In cases where pin function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics. Pins shown with an asterisk after their name (*) offer high source/high sink current capabilities.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. If $\overline{BR}$ is active (whether or not $\overline{RESET}$ is asserted), the memory pins are also three-stated. During hibernate, all outputs are three-stated unless otherwise noted in Table 9.

All I/O pins have their input buffers disabled with the exception of the pins noted in the data sheet that need pull-ups or pull-downs if unused.

The SDA (serial data) and SCL (serial clock) pins are open drain and therefore require a pull-up resistor. Consult version 2.1 of the I^2C specification for the proper resistor value.

Table 9. Pin Descriptions

Pin Name	Type	Function	Driver Type[1]
Memory Interface			
ADDR19–1	O	Address Bus for Async Access	A
DATA15–0	I/O	Data Bus for Async/Sync Access	A
$\overline{ABE1–0}$/SDQM1–0	O	Byte Enables/Data Masks for Async/Sync Access	A
$\overline{BR}$	I	Bus Request (This pin should be pulled high when not used.)	
$\overline{BG}$	O	Bus Grant	A
$\overline{BGH}$	O	Bus Grant Hang	A
Asynchronous Memory Control			
$\overline{AMS3–0}$	O	Bank Select (Require pull-ups if hibernate is used.)	A
ARDY	I	Hardware Ready Control	
$\overline{AOE}$	O	Output Enable	A
$\overline{ARE}$	O	Read Enable	A
$\overline{AWE}$	O	Write Enable	A
Synchronous Memory Control			
$\overline{SRAS}$	O	Row Address Strobe	A
$\overline{SCAS}$	O	Column Address Strobe	A
$\overline{SWE}$	O	Write Enable	A
SCKE	O	Clock Enable(Requires a pull-down if hibernate with SDRAM self-refresh is used.)	A
CLKOUT	O	Clock Output	B
SA10	O	A10 Pin	A
$\overline{SMS}$	O	Bank Select	A

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port F: GPIO/UART1–0/Timer7–0/SPI/ External DMA Request/PPI (= High Source/High Sink Pin)*			
PF0* – GPIO/*UART0 TX/DMAR0*	I/O	GPIO/*UART0 Transmit/DMA Request 0*	C
PF1* – GPIO/*UART0 RX/DMAR1/TACI1*	I/O	GPIO/*UART0 Receive/DMA Request 1/Timer1 Alternate Input Capture*	C
PF2* – GPIO/*UART1 TX/TMR7*	I/O	GPIO/*UART1 Transmit/Timer7*	C
PF3* – GPIO/*UART1 RX/TMR6/TACI6*	I/O	GPIO/*UART1 Receive/Timer6/Timer6 Alternate Input Capture*	C
PF4* – GPIO/*TMR5/SPI SSEL6*	I/O	GPIO/*Timer5/SPI Slave Select Enable 6*	C
PF5* – GPIO/*TMR4/SPI SSEL5*	I/O	GPIO/*Timer4/SPI Slave Select Enable 5*	C
PF6* – GPIO/*TMR3/SPI SSEL4*	I/O	GPIO/*Timer3/SPI Slave Select Enable 4*	C
PF7* – GPIO/*TMR2/PPI FS3*	I/O	GPIO/*Timer2/PPI Frame Sync 3*	C
PF8 – GPIO/*TMR1/PPI FS2*	I/O	GPIO/*Timer1/PPI Frame Sync 2*	C
PF9 – GPIO/*TMR0/PPI FS1*	I/O	GPIO/*Timer0/PPI Frame Sync 1*	C
PF10 – GPIO/*SPI SSEL1*	I/O	GPIO/*SPI Slave Select Enable 1*	C
PF11 – GPIO/*SPI MOSI*	I/O	GPIO/*SPI Master Out Slave In*	C
PF12 – GPIO/*SPI MISO*	I/O	GPIO/*SPI Master In Slave Out* (This pin should be pulled high through a 4.7 kΩ resistor if booting via the SPI port.)	C
PF13 – GPIO/*SPI SCK*	I/O	GPIO/*SPI Clock*	D
PF14 – GPIO/*SPI SS/TACLK0*	I/O	GPIO/*SPI Slave Select/Alternate Timer0 Clock Input*	C
PF15 – GPIO/*PPI CLK/TMRCLK*	I/O	GPIO/*PPI Clock/External Timer Reference*	C
Port G: GPIO/PPI/SPORT1			
PG0 – GPIO/*PPI D0*	I/O	GPIO/*PPI Data 0*	C
PG1 – GPIO/*PPI D1*	I/O	GPIO/*PPI Data 1*	C
PG2 – GPIO/*PPI D2*	I/O	GPIO/*PPI Data 2*	C
PG3 – GPIO/*PPI D3*	I/O	GPIO/*PPI Data 3*	C
PG4 – GPIO/*PPI D4*	I/O	GPIO/*PPI Data 4*	C
PG5 – GPIO/*PPI D5*	I/O	GPIO/*PPI Data 5*	C
PG6 – GPIO/*PPI D6*	I/O	GPIO/*PPI Data 6*	C
PG7 – GPIO/*PPI D7*	I/O	GPIO/*PPI Data 7*	C
PG8 – GPIO/*PPI D8/DR1SEC*	I/O	GPIO/*PPI Data 8/SPORT1 Receive Data Secondary*	C
PG9 – GPIO/*PPI D9/DT1SEC*	I/O	GPIO/*PPI Data 9/SPORT1 Transmit Data Secondary*	C
PG10 – GPIO/*PPI D10/RSCLK1*	I/O	GPIO/*PPI Data 10/SPORT1 Receive Serial Clock*	D
PG11 – GPIO/*PPI D11/RFS1*	I/O	GPIO/*PPI Data 11/SPORT1 Receive Frame Sync*	C
PG12 – GPIO/*PPI D12/DR1PRI*	I/O	GPIO/*PPI Data 12/SPORT1 Receive Data Primary*	C
PG13 – GPIO/*PPI D13/TSCLK1*	I/O	GPIO/*PPI Data 13/SPORT1 Transmit Serial Clock*	D
PG14 – GPIO/*PPI D14/TFS1*	I/O	GPIO/*PPI Data 14/SPORT1 Transmit Frame Sync*	C
PG15 – GPIO/*PPI D15/DT1PRI*	I/O	GPIO/*PPI Data 15/SPORT1 Transmit Data Primary*	C

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 300 MHz, 400 MHz, and 500 MHz speed grade models[2]	0.8	1.2	1.32	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 600 MHz speed grade models[2]	0.8	1.3	1.43	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive grade models and +105°C nonautomotive grade models[2]	0.95	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Nonautomotive grade models[2]	2.25	2.5 or 3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models and +105°C nonautomotive grade models[2]	2.7	3.0 or 3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[3, 4]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.2			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[6]		$0.7 \times V_{DDEXT}$			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[7]	V_{DDEXT} = Maximum	2.0			V
V_{IL}	Low Level Input Voltage[3, 8]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[6]				$0.3 \times V_{DDEXT}$	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[7]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+120	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance. The required V_{DDINT} is a function of speed grade and operating frequency. See Table 10, Table 11, and Table 12 for details.

[2] See Ordering Guide on Page 67.

[3] Bidirectional pins (DATA15–0, PF15–0, PG15–0, PH15–0, TFS0, TSCLK0, RSCLK0, RFS0, MDIO) and input pins ($\overline{BR}$, ARDY, DR0PRI, DR0SEC, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF534/ADSP-BF536/ADSP-BF537 are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[4] Parameter value applies to all input and bidirectional pins except CLKIN, SDA, and SCL.

[5] Parameter value applies to CLKIN pin only.

[6] Applies to pins PJ2/SCL and PJ3/SDA which are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[7] Applies to pin PJ4/DR0SEC/CANRX/TACI0 which is 5.0 V tolerant (always accepts up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Parameter value applies to all input and bidirectional pins except SDA and SCL.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
V_{OH}[3]	High Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –2.0 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
I_{OH}[6]	High Level Output Current	V_{OH} = V_{DDEXT} – 0.5 V Min			–64			–64	mA
I_{OH}[7]		V_{OH} = V_{DDEXT} – 0.5 V Min			–144			–144	mA
V_{OL}[3]	Low Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA			0.5			0.5	V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OL} = 6 mA			0.5			0.5	V
V_{OL}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.5			0.5	V
I_{OL}[6]	Low Level Output Current	V_{OL} = 0.5 V Max			64			64	mA
I_{OL}[7]		V_{OL} = 0.5 V Max			144			144	mA
I_{IH}	High Level Input Current[8]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{IH5V}	High Level Input Current[9]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{IL}	Low Level Input Current[2]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA
I_{IHP}	High Level Input Current JTAG[10]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			50			50	µA
I_{OZH}	Three-State Leakage Current[11]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{OZH5V}	Three-State Leakage Current[12]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA

System designers should refer to *Estimating Power for the ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*, which provides detailed information for optimizing designs for lowest power. All topics discussed in this section are described in detail in EE-297. Total power dissipation has two components:

1. Static, including leakage current
2. Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 25 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 or Table 15), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 18).

The dynamic component is also subject to an Activity Scaling Factor (ASF) which represents application code running on the processor (Table 17).

Table 15. Static Current–500 MHz, 533 MHz, and 600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})													
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V	1.375 V	1.43 V
–40	3.9	4.7	6.8	8.2	9.9	12.0	14.6	17.3	20.3	24.1	27.1	28.6	36.3	44.4
0	17.0	19.2	21.9	25.0	28.2	32.1	36.9	41.8	47.7	53.8	61.0	63.8	73.2	84.1
25	35.0	39.2	44.3	50.8	56.1	63.3	69.1	76.4	84.7	93.5	104.5	109.1	123.4	138.8
40	53.0	59.2	65.3	71.9	79.1	88.0	96.6	108.0	120.0	130.7	142.6	148.5	166.5	185.6
55	76.7	84.6	93.6	103.1	113.7	123.9	136.3	148.3	162.8	178.4	194.4	201.4	223.7	247.5
70	110.1	120.0	130.9	142.2	156.5	171.3	185.2	201.7	220.6	239.7	259.8	268.8	295.9	325.2
85	150.1	164.5	178.7	193.2	210.4	228.9	247.7	268.8	291.4	314.1	341.1	351.2	384.6	420.3
100	202.3	219.2	236.5	255.8	277.8	299.8	323.8	351.2	378.8	407.5	440.4	453.4	494.3	538.2
105	223.8	241.4	260.4	282.0	303.4	328.7	354.5	381.7	410.8	443.6	477.8	492.2	535.1	581.5

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.

Table 16. Static Current–300 MHz and 400 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})											
T_J (°C)	0.80 V	0.85 V	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.32 V
–40	2.6	3.2	3.7	4.5	5.5	6.6	7.9	9.3	10.5	12.5	13.9	14.8
0	6.6	7.8	8.4	9.9	10.9	12.3	13.8	15.5	17.5	19.6	21.7	23.1
25	12.2	13.5	14.8	16.4	18.2	19.9	22.7	25.6	28.4	31.8	35.7	37.2
40	17.2	19.0	20.6	22.9	25.9	28.2	31.6	34.9	38.9	42.9	47.6	49.5
55	25.7	27.8	30.9	33.7	37.3	41.4	44.8	50.0	54.8	59.4	66.1	68.4
70	37.6	41.3	44.8	48.9	53.9	58.6	63.9	69.7	76.9	84.0	92.2	94.9
85	53.7	58.3	63.7	69.0	75.9	82.9	90.5	98.4	106.4	115.3	124.6	128.1
100	75.1	82.3	88.5	95.8	104.0	112.5	121.8	130.6	141.3	153.2	164.8	169.7
105	84.5	91.2	98.2	106.0	114.2	123.0	132.4	143.3	155.0	167.4	179.8	185.4
115[2]	103.8	111.8	120.3	127.6	138.0	148.5	159.6	171.4	184.6	198.8	213.4	219.6
120[2]	115.5	123.6	132.2	141.9	152.3	163.7	175.6	189.3	202.8	217.7	232.3	238.6

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ specifications.
[2] Applies to automotive grade models only.

Asynchronous Memory Write Cycle Timing

Table 25. Asynchronous Memory Write Cycle Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before CLKOUT	4.0		ns
t_{HARDY}	ARDY Hold After CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	1.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.8		ns

[1] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, $\overline{AWE}$.

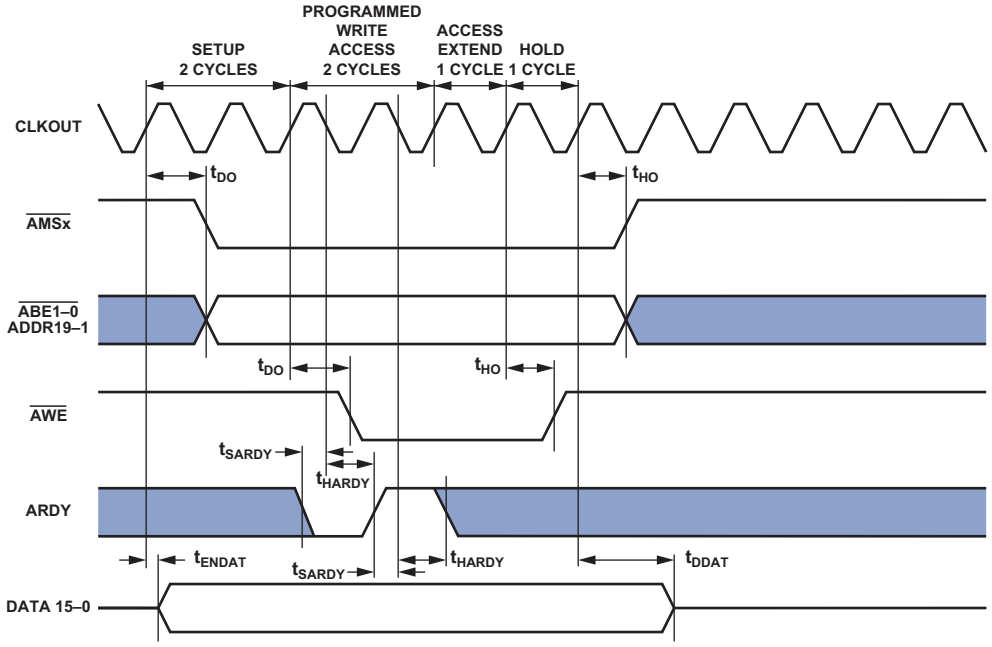


Figure 12. Asynchronous Memory Write Cycle Timing

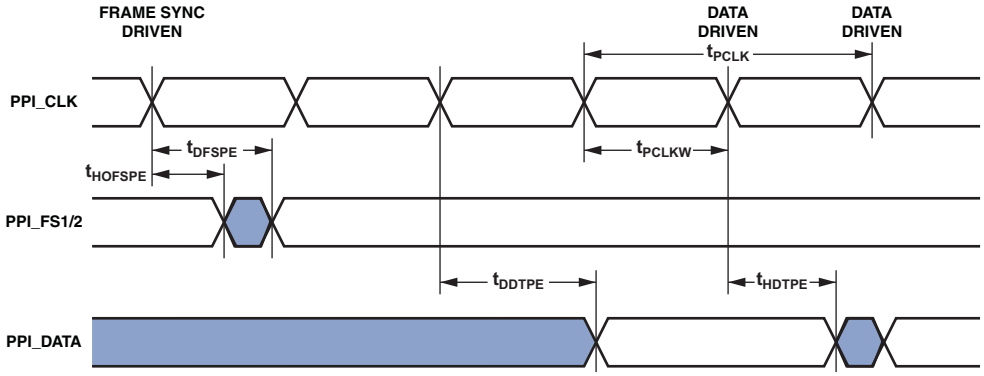


Figure 18. PPI GP Tx Mode with Internal Frame Sync Timing

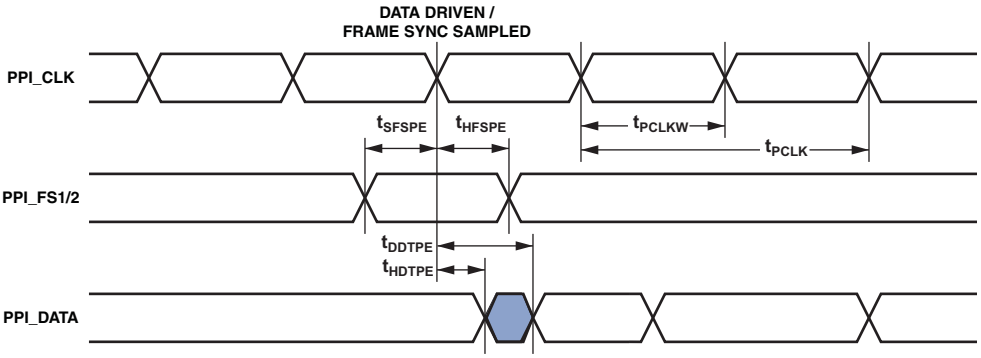


Figure 19. PPI GP Tx Mode with External Frame Sync Timing

Serial Peripheral Interface Port—Slave Timing

Table 35 and Figure 25 describe SPI port slave operations.

Table 35. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	Serial Clock High Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{SCLK} - 1.5$		ns
t_{SPICLK}	Serial Clock Period	$4 \times t_{SCLK}$		ns
t_{HDS}	Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2 \times t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2 \times t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{SPISS}$ Assertion to First SCK Edge	$2 \times t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPISS}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{SPISS}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SCK Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SCK Edge to Data Out Invalid (Data Out Hold)	0		ns

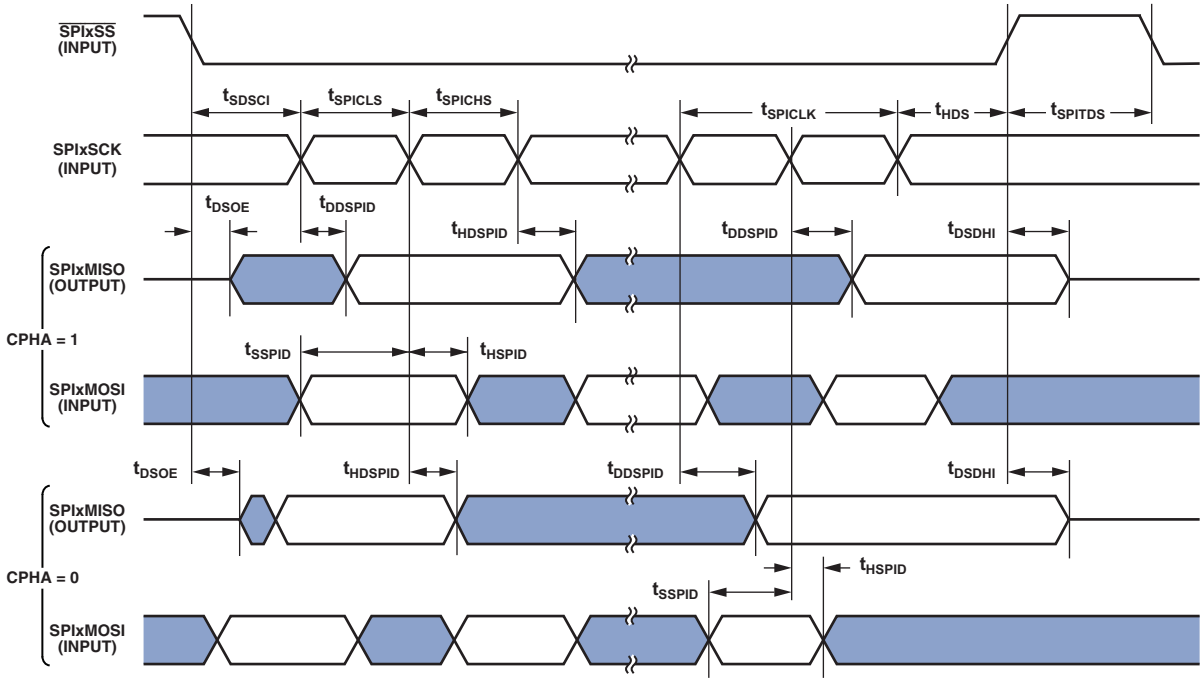


Figure 25. Serial Peripheral Interface (SPI) Port—Slave Timing

JTAG Test and Emulation Port Timing

Table 39 and Figure 29 describe JTAG port operations.

Table 39. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Parameters				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	5		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width[2] (Measured in TCK Cycles)	4		TCK
Switching Characteristics				
t_{DTDO}	TDO Delay From TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	12	ns

[1] System Inputs = DATA15–0, $\overline{\text{BR}}$, ARDY, SCL, SDA, TFS0, TSCLK0, RSCLK0, RFS0, DR0PRI, DR0SEC, PF15–0, PG15–0, PH15–0, MDIO, TCK, $\overline{\text{TRST}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, RTXI, BMODE2–0.

[2] 50 MHz maximum.

[3] System Outputs = DATA15–0, ADDR19–1, $\overline{\text{ABE1–0}}$, $\overline{\text{BG}}$, $\overline{\text{BGH}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{SWE}}$, SCKE, CLKOUT, SA10, $\overline{\text{SMS}}$, SCL, SDA, MDC, MDIO, TSCLK0, TFS0, RFS0, RSCLK0, DT0PRI, DT0SEC, PF15–0, PG15–0, PH15–0, RTXO, TDO, $\overline{\text{EMU}}$, XTAL, VROUT1–0.

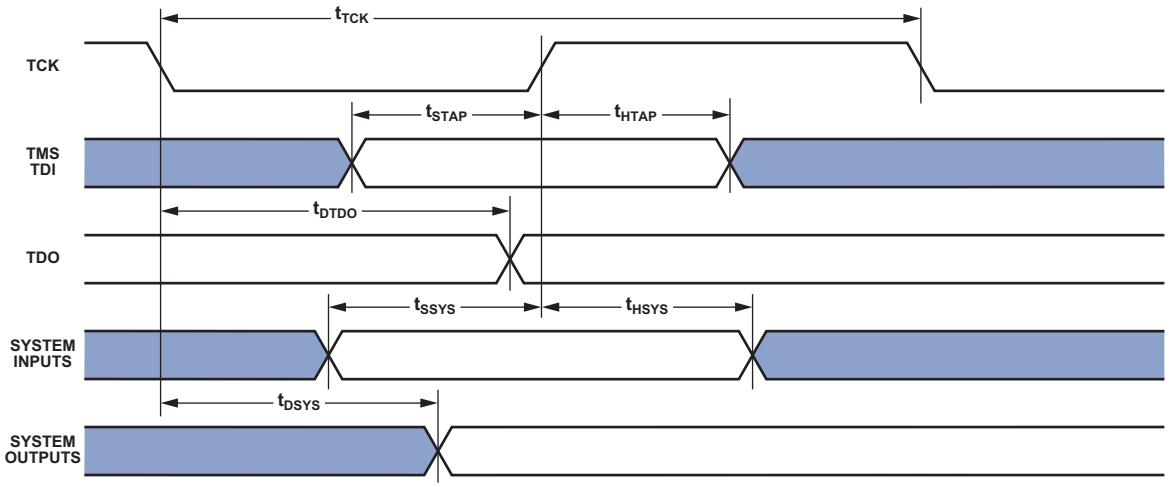


Figure 29. JTAG Port Timing

Table 44. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 45. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	10		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	10		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

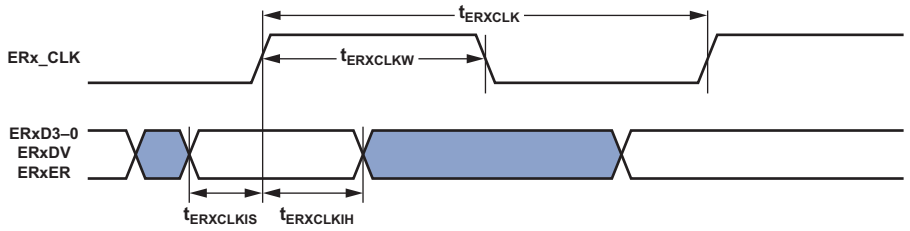


Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

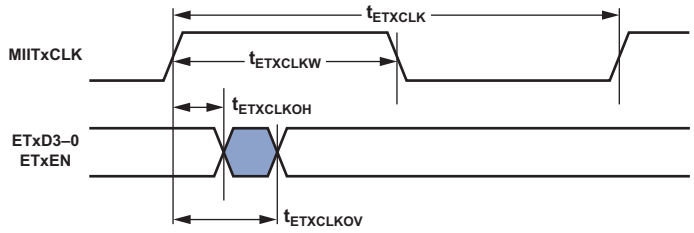


Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

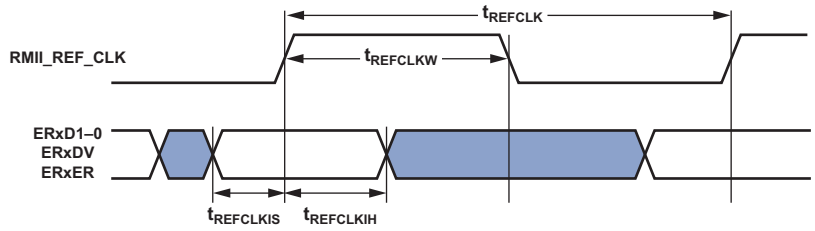


Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

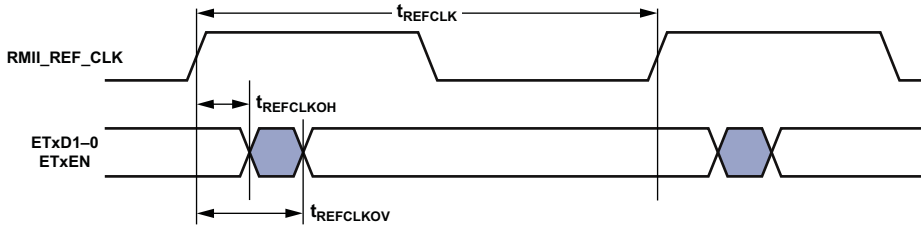


Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

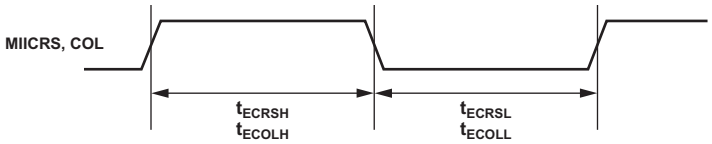


Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

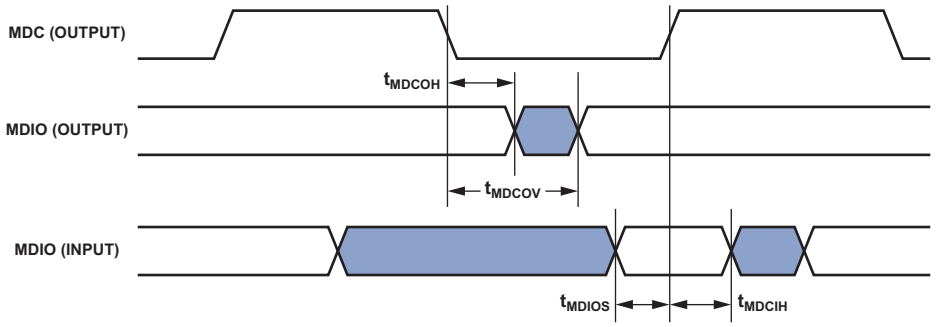
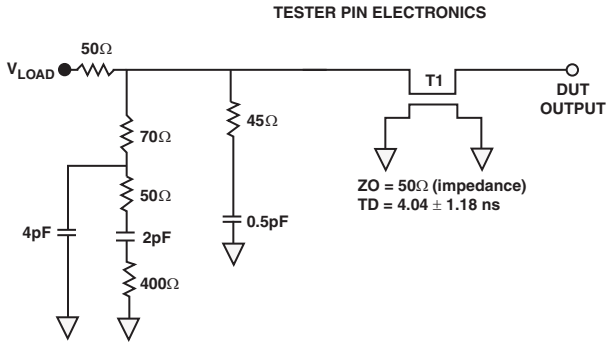


Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 50). Figure 51 through Figure 60 on Page 55 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

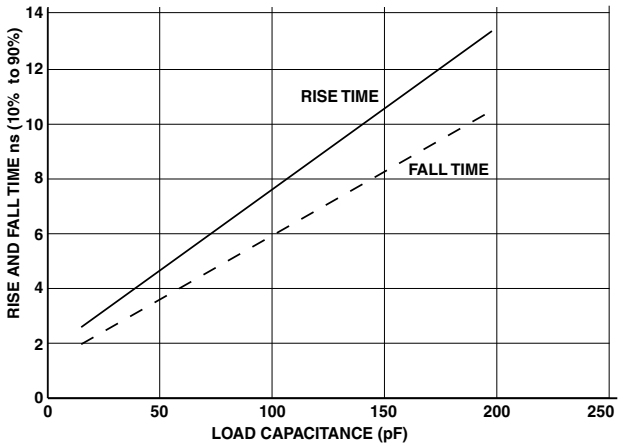


Figure 51. Typical Output Delay or Hold for Driver A at V_{DDEXT} Min

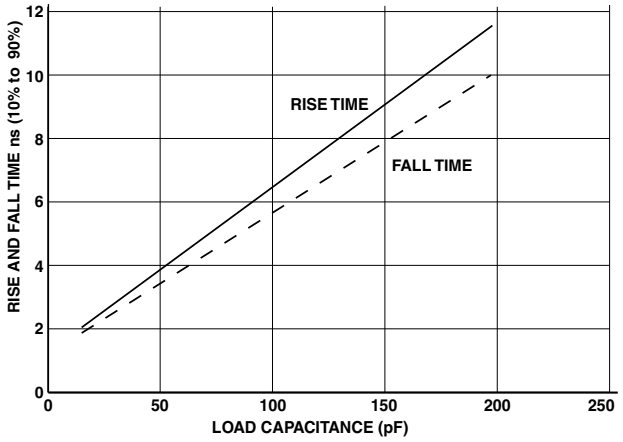


Figure 52. Typical Output Delay or Hold for Driver A at V_{DDEXT} Max

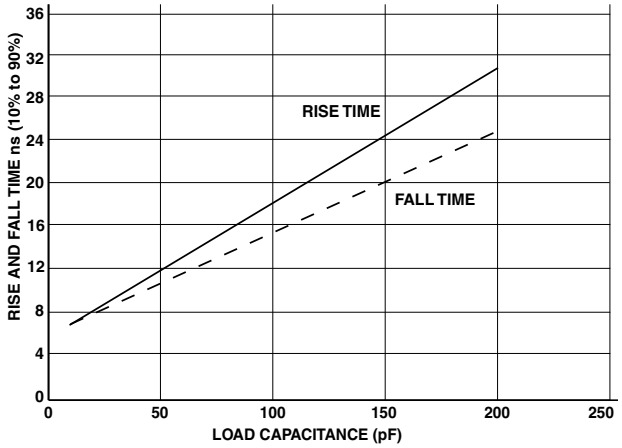


Figure 59. Typical Output Delay or Hold for Driver E at V_{DDEXT} Min

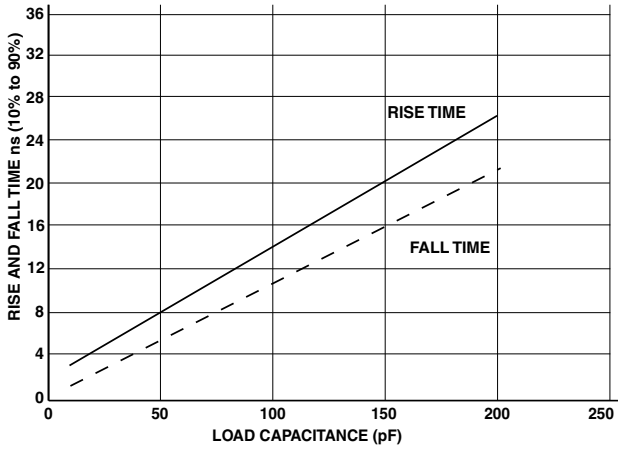


Figure 60. Typical Output Delay or Hold for Driver E at V_{DDEXT} Max

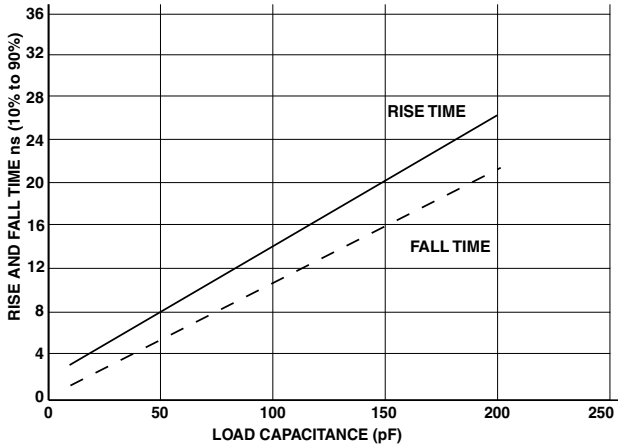


Figure 61. Typical Output Delay or Hold for Driver F at V_{DDEXT} Min

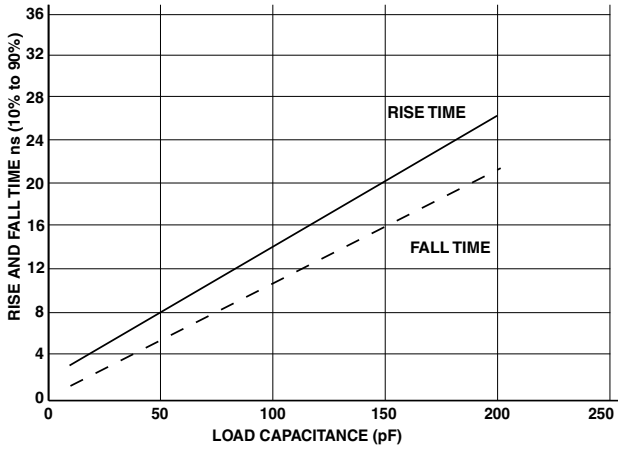


Figure 62. Typical Output Delay or Hold for Driver F at V_{DDEXT} Max

Table 50. 182-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	V_{DDEXT}	C10	$\overline{RESET}$	F5	GND	J14	ADDR1	M9	DATA0
A2	PH11	C11	PJ3	F6	GND	K1	PF5	M10	GND
A3	PH12	C12	V_{DDEXT}	F10	GND	K2	PF6	M11	ADDR15
A4	PH13	C13	$\overline{SMS}$	F11	GND	K3	PF7	M12	ADDR9
A5	PH14	C14	$\overline{SCAS}$	F12	V_{DDEXT}	K4	PF8	M13	ADDR10
A6	PH15	D1	PG10	F13	$\overline{AMS2}$	K5	V_{DDINT}	M14	ADDR11
A7	CLKBUF	D2	PG11	F14	$\overline{AMS1}$	K6	GND	N1	$\overline{TRST}$
A8	RTXO	D3	PG12	G1	PG0	K7	V_{DDEXT}	N2	TMS
A9	RTXI	D4	GND	G2	PG1	K8	V_{DDINT}	N3	TDO
A10	GND	D5	PG13	G3	PG2	K9	V_{DDEXT}	N4	BMODE0
A11	XTAL	D6	PG14	G4	GND	K10	V_{DDINT}	N5	DATA13
A12	CLKIN	D7	PJ4	G5	GND	K11	GND	N6	DATA10
A13	VROUT0	D8	PJ5	G10	V_{DDINT}	K12	ADDR7	N7	DATA7
A14	GND	D9	PJ8	G11	GND	K13	ADDR5	N8	DATA4
B1	PH5	D10	PJ10	G12	$\overline{AMS3}$	K14	ADDR2	N9	DATA1
B2	PH6	D11	PJ11	G13	$\overline{AOE}$	L1	PF1	N10	$\overline{BGH}$
B3	PH7	D12	$\overline{SWE}$	G14	$\overline{ARE}$	L2	PF2	N11	ADDR16
B4	PH8	D13	$\overline{SRAS}$	H1	PF12	L3	PF3	N12	ADDR14
B5	PH9	D14	$\overline{BR}$	H2	PF13	L4	PF4	N13	ADDR13
B6	PH10	E1	PG6	H3	PF14	L5	BMODE2	N14	ADDR12
B7	PJ1	E2	PG7	H4	PF15	L6	GND	P1	V_{DDEXT}
B8	PJ7	E3	PG8	H5	V_{DDEXT}	L7	V_{DDEXT}	P2	TCK
B9	V_{DDRTC}	E4	PG9	H10	V_{DDEXT}	L8	GND	P3	BMODE1
B10	$\overline{NMI}$	E5	V_{DDINT}	H11	GND	L9	V_{DDEXT}	P4	DATA15
B11	PJ2	E6	V_{DDEXT}	H12	$\overline{ABE1}$	L10	GND	P5	DATA14
B12	VROUT1	E7	GND	H13	$\overline{ABE0}$	L11	V_{DDEXT}	P6	DATA11
B13	SCKE	E8	V_{DDINT}	H14	$\overline{AWE}$	L12	ADDR8	P7	DATA8
B14	CLKOUT	E9	GND	J1	PF9	L13	ADDR6	P8	DATA5
C1	PG15	E10	V_{DDINT}	J2	PF10	L14	ADDR3	P9	DATA2
C2	PH0	E11	V_{DDEXT}	J3	PF11	M1	PF0	P10	$\overline{BG}$
C3	PH1	E12	SA10	J4	GND	M2	$\overline{EMU}$	P11	ADDR19
C4	PH2	E13	ARDY	J5	GND	M3	TDI	P12	ADDR18
C5	PH3	E14	$\overline{AMS0}$	J9	GND	M4	GND	P13	ADDR17
C6	PH4	F1	PG3	J10	GND	M5	DATA12	P14	GND
C7	PJ0	F2	PG4	J11	V_{DDEXT}	M6	DATA9		
C8	PJ6	F3	PG5	J12	V_{DDEXT}	M7	DATA6		
C9	PJ9	F4	V_{DDEXT}	J13	ADDR4	M8	DATA3		

208-BALL CSP_BGA BALL ASSIGNMENT

Table 51 lists the CSP_BGA ball assignment by signal mnemonic. Table 52 on Page 61 lists the CSP_BGA ball assignment by ball number.

Table 51. 208-Ball CSP_BGA Ball Assignment (Alphabetically by Signal Mnemonic)

Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.
$\overline{ABE0}$	P19	DATA12	Y4	GND	M13	PG6	E2	TDI	V1
$\overline{ABE1}$	P20	DATA13	W4	GND	N9	PG7	D1	TDO	Y2
ADDR1	R19	DATA14	Y3	GND	N10	PG8	D2	TMS	U2
ADDR10	W18	DATA15	W3	GND	N11	PG9	C1	$\overline{TRST}$	U1
ADDR11	Y18	DATA2	Y9	GND	N12	PH0	B4	V_{DDEXT}	G7
ADDR12	W17	DATA3	W9	GND	N13	PH1	A5	V_{DDEXT}	G8
ADDR13	Y17	DATA4	Y8	GND	P11	PH10	B9	V_{DDEXT}	G9
ADDR14	W16	DATA5	W8	GND	V2	PH11	A10	V_{DDEXT}	G10
ADDR15	Y16	DATA6	Y7	GND	W2	PH12	B10	V_{DDEXT}	H7
ADDR16	W15	DATA7	W7	GND	W19	PH13	A11	V_{DDEXT}	H8
ADDR17	Y15	DATA8	Y6	GND	Y1	PH14	B11	V_{DDEXT}	J7
ADDR18	W14	DATA9	W6	GND	Y13	PH15	A12	V_{DDEXT}	J8
ADDR19	Y14	$\overline{EMU}$	T1	GND	Y20	PH2	B5	V_{DDEXT}	K7
ADDR2	T20	GND	A1	$\overline{NMI}$	C20	PH3	A6	V_{DDEXT}	K8
ADDR3	T19	GND	A13	PF0	T2	PH4	B6	V_{DDEXT}	L7
ADDR4	U20	GND	A20	PF1	R1	PH5	A7	V_{DDEXT}	L8
ADDR5	U19	GND	B2	PF10	L2	PH6	B7	V_{DDEXT}	M7
ADDR6	V20	GND	G11	PF11	K1	PH7	A8	V_{DDEXT}	M8
ADDR7	V19	GND	H9	PF12	K2	PH8	B8	V_{DDEXT}	N7
ADDR8	W20	GND	H10	PF13	J1	PH9	A9	V_{DDEXT}	N8
ADDR9	Y19	GND	H11	PF14	J2	PJ0	B12	V_{DDEXT}	P7
$\overline{AMS0}$	M20	GND	H12	PF15	H1	PJ1	B13	V_{DDEXT}	P8
$\overline{AMS1}$	M19	GND	H13	PF2	R2	PJ10	B19	V_{DDEXT}	P9
$\overline{AMS2}$	G20	GND	J9	PF3	P1	PJ11	C19	V_{DDEXT}	P10
$\overline{AMS3}$	G19	GND	J10	PF4	P2	PJ2	D19	V_{DDINT}	G12
$\overline{AOE}$	N20	GND	J11	PF5	N1	PJ3	E19	V_{DDINT}	G13
ARDY	J19	GND	J12	PF6	N2	PJ4	B18	V_{DDINT}	G14
$\overline{ARE}$	N19	GND	J13	PF7	M1	PJ5	A19	V_{DDINT}	H14
$\overline{AWE}$	R20	GND	K9	PF8	M2	PJ6	B15	V_{DDINT}	J14
$\overline{BG}$	Y11	GND	K10	PF9	L1	PJ7	B16	V_{DDINT}	K14
$\overline{BGH}$	Y12	GND	K11	PG0	H2	PJ8	B17	V_{DDINT}	L14
BMODE0	W13	GND	K12	PG1	G1	PJ9	B20	V_{DDINT}	M14
BMODE1	W12	GND	K13	PG10	C2	$\overline{RESET}$	D20	V_{DDINT}	N14
BMODE2	W11	GND	L9	PG11	B1	RTXO	A15	V_{DDINT}	P12
$\overline{BR}$	F19	GND	L10	PG12	A2	RTXI	A14	V_{DDINT}	P13
CLKBUF	B14	GND	L11	PG13	A3	SA10	L20	V_{DDINT}	P14
CLKIN	A18	GND	L12	PG14	B3	$\overline{SCAS}$	K20	V_{DDRTC}	A16
CLKOUT	H19	GND	L13	PG15	A4	SCKE	H20	VROUT0	E20
DATA0	Y10	GND	M9	PG2	G2	$\overline{SMS}$	J20	VROUT1	F20
DATA1	W10	GND	M10	PG3	F1	$\overline{SRAS}$	K19	XTAL	A17
DATA10	Y5	GND	M11	PG4	F2	$\overline{SWE}$	L19		
DATA11	W5	GND	M12	PG5	E1	TCK	W1		

Table 52 lists the CSP_BGA ball assignment by ball number. Table 51 on Page 60 lists the CSP_BGA ball assignment by signal mnemonic.

Table 52. 208-Ball CSP_BGA Ball Assignment (Numerically by Ball Number)

Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic	Ball No.	Mnemonic
A1	GND	C19	PJ11	J9	GND	M19	$\overline{AMS1}$	W1	TCK
A2	PG12	C20	$\overline{NMI}$	J10	GND	M20	$\overline{AMS0}$	W2	GND
A3	PG13	D1	PG7	J11	GND	N1	PF5	W3	DATA15
A4	PG15	D2	PG8	J12	GND	N2	PF6	W4	DATA13
A5	PH1	D19	PJ2	J13	GND	N7	V_{DDEXT}	W5	DATA11
A6	PH3	D20	$\overline{RESET}$	J14	V_{DDINT}	N8	V_{DDEXT}	W6	DATA9
A7	PH5	E1	PG5	J19	ARDY	N9	GND	W7	DATA7
A8	PH7	E2	PG6	J20	$\overline{SMS}$	N10	GND	W8	DATA5
A9	PH9	E19	PJ3	K1	PF11	N11	GND	W9	DATA3
A10	PH11	E20	VROUT0	K2	PF12	N12	GND	W10	DATA1
A11	PH13	F1	PG3	K7	V_{DDEXT}	N13	GND	W11	BMODE2
A12	PH15	F2	PG4	K8	V_{DDEXT}	N14	V_{DDINT}	W12	BMODE1
A13	GND	F19	$\overline{BR}$	K9	GND	N19	$\overline{ARE}$	W13	BMODE0
A14	RTXI	F20	VROUT1	K10	GND	N20	$\overline{AOE}$	W14	ADDR18
A15	RTXO	G1	PG1	K11	GND	P1	PF3	W15	ADDR16
A16	V_{DDRTC}	G2	PG2	K12	GND	P2	PF4	W16	ADDR14
A17	XTAL	G7	V_{DDEXT}	K13	GND	P7	V_{DDEXT}	W17	ADDR12
A18	CLKIN	G8	V_{DDEXT}	K14	V_{DDINT}	P8	V_{DDEXT}	W18	ADDR10
A19	PJ5	G9	V_{DDEXT}	K19	$\overline{SRAS}$	P9	V_{DDEXT}	W19	GND
A20	GND	G10	V_{DDEXT}	K20	$\overline{SCAS}$	P10	V_{DDEXT}	W20	ADDR8
B1	PG11	G11	GND	L1	PF9	P11	GND	Y1	GND
B2	GND	G12	V_{DDINT}	L2	PF10	P12	V_{DDINT}	Y2	TDO
B3	PG14	G13	V_{DDINT}	L7	V_{DDEXT}	P13	V_{DDINT}	Y3	DATA14
B4	PH0	G14	V_{DDINT}	L8	V_{DDEXT}	P14	V_{DDINT}	Y4	DATA12
B5	PH2	G19	$\overline{AMS3}$	L9	GND	P19	$\overline{ABE0}$	Y5	DATA10
B6	PH4	G20	$\overline{AMS2}$	L10	GND	P20	$\overline{ABE1}$	Y6	DATA8
B7	PH6	H1	PF15	L11	GND	R1	PF1	Y7	DATA6
B8	PH8	H2	PG0	L12	GND	R2	PF2	Y8	DATA4
B9	PH10	H7	V_{DDEXT}	L13	GND	R19	ADDR1	Y9	DATA2
B10	PH12	H8	V_{DDEXT}	L14	V_{DDINT}	R20	$\overline{AWE}$	Y10	DATA0
B11	PH14	H9	GND	L19	$\overline{SWE}$	T1	$\overline{EMU}$	Y11	$\overline{BG}$
B12	PJ0	H10	GND	L20	SA10	T2	PF0	Y12	$\overline{BGH}$
B13	PJ1	H11	GND	M1	PF7	T19	ADDR3	Y13	GND
B14	CLKBUF	H12	GND	M2	PF8	T20	ADDR2	Y14	ADDR19
B15	PJ6	H13	GND	M7	V_{DDEXT}	U1	$\overline{TRST}$	Y15	ADDR17
B16	PJ7	H14	V_{DDINT}	M8	V_{DDEXT}	U2	TMS	Y16	ADDR15
B17	PJ8	H19	CLKOUT	M9	GND	U19	ADDR5	Y17	ADDR13
B18	PJ4	H20	SCKE	M10	GND	U20	ADDR4	Y18	ADDR11
B19	PJ10	J1	PF13	M11	GND	V1	TDI	Y19	ADDR9
B20	PJ9	J2	PF14	M12	GND	V2	GND	Y20	GND
C1	PG9	J7	V_{DDEXT}	M13	GND	V19	ADDR7		
C2	PG10	J8	V_{DDEXT}	M14	V_{DDINT}	V20	ADDR6		

Figure 65 shows the top view of the CSP_BGA ball configuration. Figure 66 shows the bottom view of the CSP_BGA ball configuration.

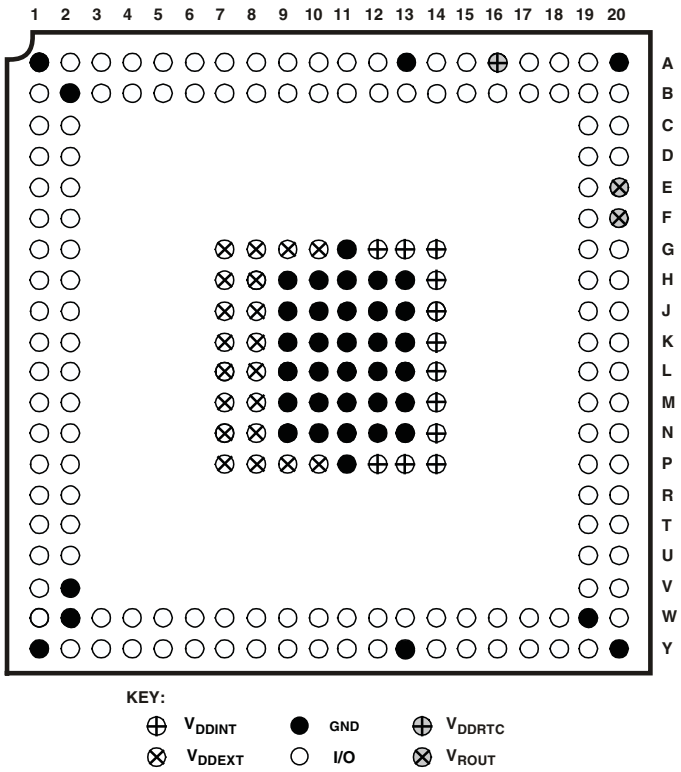


Figure 65. 208-Ball CSP_BGA Configuration (Top View)

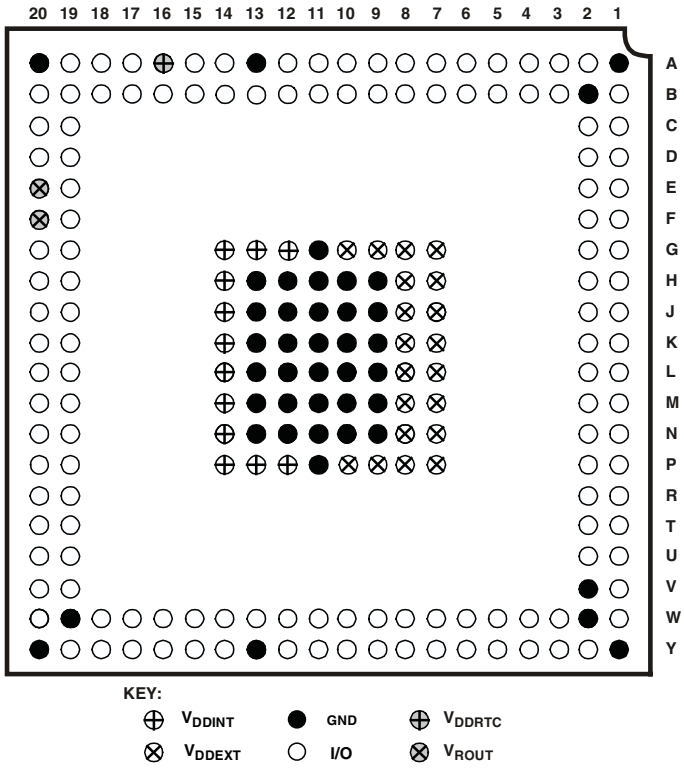


Figure 66. 208-Ball CSP_BGA Configuration (Bottom View)

AUTOMOTIVE PRODUCTS

The ADBF534W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 53 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 53. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF534WBBCZ4Axx	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADBF534WBBCZ4Bxx	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADBF534WYBCZ4Bxx	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature.