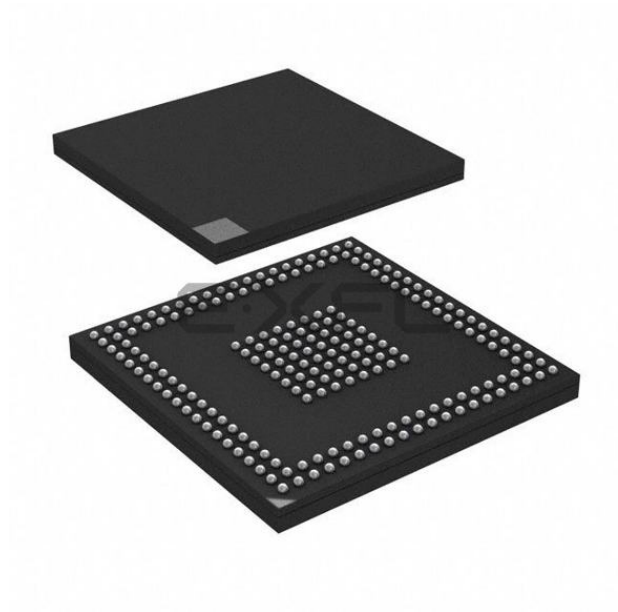

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-FBGA, CSPBGA
Supplier Device Package	208-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf537bbcz-5bv

BLACKFIN PROCESSOR CORE

As shown in Figure 2, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16-bit or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). If the second ALU is used, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates, and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

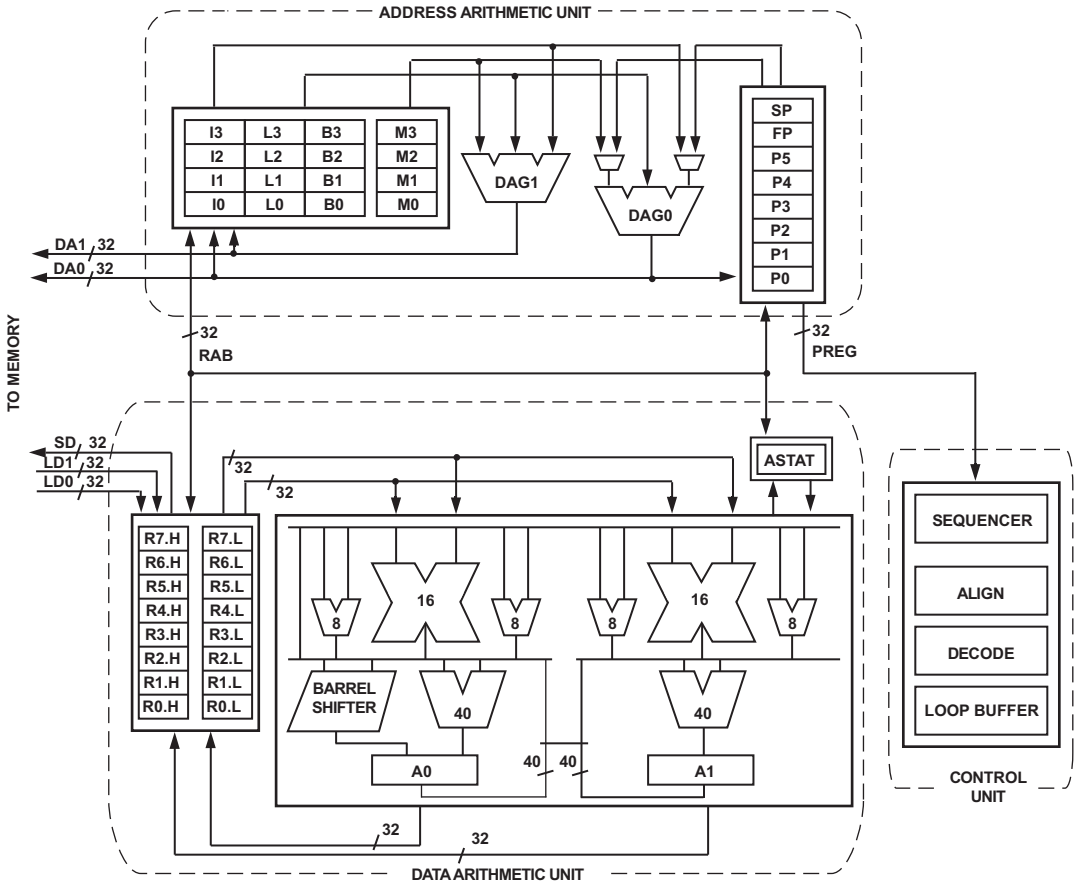

Figure 2. Blackfin Processor Core

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the Blackfin processor. Table 2 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

Table 2. Core Event Controller (CEC)

Priority (0 Is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General-Purpose Interrupt 7	IVG7
8	General-Purpose Interrupt 8	IVG8
9	General-Purpose Interrupt 9	IVG9
10	General-Purpose Interrupt 10	IVG10
11	General-Purpose Interrupt 11	IVG11
12	General-Purpose Interrupt 12	IVG12
13	General-Purpose Interrupt 13	IVG13
14	General-Purpose Interrupt 14	IVG14
15	General-Purpose Interrupt 15	IVG15

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the processor provides a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (IAR). Table 3 describes the inputs into the SIC and the default mappings into the CEC.

Table 3. System Interrupt Controller (SIC)

Peripheral Interrupt Event	Default Mapping	Peripheral Interrupt ID
PLL Wakeup	IVG7	0
DMA Error (Generic)	IVG7	1
DMAR0 Block Interrupt	IVG7	1
DMAR1 Block Interrupt	IVG7	1
DMAR0 Overflow Error	IVG7	1
DMAR1 Overflow Error	IVG7	1
CAN Error	IVG7	2
Ethernet Error (ADSP-BF536 and ADSP-BF537 only)	IVG7	2
SPORT 0 Error	IVG7	2
SPORT 1 Error	IVG7	2
PPI Error	IVG7	2
SPI Error	IVG7	2
UART0 Error	IVG7	2
UART1 Error	IVG7	2
Real-Time Clock	IVG8	3
DMA Channel 0 (PPI)	IVG8	4
DMA Channel 3 (SPORT 0 Rx)	IVG9	5
DMA Channel 4 (SPORT 0 Tx)	IVG9	6
DMA Channel 5 (SPORT 1 Rx)	IVG9	7
DMA Channel 6 (SPORT 1 Tx)	IVG9	8
TWI	IVG10	9
DMA Channel 7 (SPI)	IVG10	10
DMA Channel 8 (UART0 Rx)	IVG10	11
DMA Channel 9 (UART0 Tx)	IVG10	12
DMA Channel 10 (UART1 Rx)	IVG10	13
DMA Channel 11 (UART1 Tx)	IVG10	14
CAN Rx	IVG11	15
CAN Tx	IVG11	16
DMA Channel 1 (Ethernet Rx, ADSP-BF536 and ADSP-BF537 only)	IVG11	17
Port H Interrupt A	IVG11	17
DMA Channel 2 (Ethernet Tx, ADSP-BF536 and ADSP-BF537 only)	IVG11	18
Port H Interrupt B	IVG11	18
Timer 0	IVG12	19
Timer 1	IVG12	20
Timer 2	IVG12	21
Timer 3	IVG12	22
Timer 4	IVG12	23
Timer 5	IVG12	24
Timer 6	IVG12	25
Timer 7	IVG12	26
Port F, G Interrupt A	IVG12	27
Port G Interrupt B	IVG12	28

SERIAL PORTS (SPORTs)

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors incorporate two dual-channel synchronous serial ports (SPORT0 and SPORT1) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length – Each SPORT supports serial data words from 3 bits to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware – Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead – Each SPORT can automatically receive and transmit multiple buffers of memory data. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multichannel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors have an SPI-compatible port that enables the processor to communicate with multiple SPI-compatible devices.

The SPI interface uses three pins for transferring data: two data pins (Master Output-Slave Input, MOSI, and Master Input-Slave Output, MISO) and a clock pin (serial clock, SCK). An SPI chip select input pin ($\overline{\text{SPISS}}$) lets other SPI devices select the processor, and seven SPI chip select output pins ($\overline{\text{SPISEL7–1}}$) let the processor select other SPI devices. The SPI select pins are reconfigured programmable flag pins. Using these pins, the SPI port provides a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as:

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port simultaneously transmits and receives by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide two full-duplex universal asynchronous receiver and transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}/16) bits per second.
- Supporting data formats from 7 bits to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as:

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16 \times UARTx\_Divisor}$$

where the 16-bit *UARTx_Divisor* comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant 8 bits).

Output Mode

Output mode is used for transmitting video or other data with up to three output frame syncs. Typically, a single frame sync is appropriate for data converter applications, whereas two or three frame syncs could be used for sending video with hardware signaling.

ITU-R 656 Mode Descriptions

The ITU-R 656 modes of the PPI are intended to suit a wide variety of video capture, processing, and transmission applications. Three distinct submodes are supported:

1. Active video only mode
2. Vertical blanking only mode
3. Entire field mode

Active Video Mode

Active video only mode is used when only the active video portion of a field is of interest and not any of the blanking intervals. The PPI does not read in any data between the end of active video (EAV) and start of active video (SAV) preamble symbols, or any data present during the vertical blanking intervals. In this mode, the control byte sequences are not stored to memory; they are filtered by the PPI. After synchronizing to the start of Field 1, the PPI ignores incoming samples until it sees an SAV code. The user specifies the number of active video lines per frame (in PPI_COUNT register).

Vertical Blanking Interval Mode

In this mode, the PPI only transfers vertical blanking interval (VBI) data.

Entire Field Mode

In this mode, the entire incoming bit stream is read in through the PPI. This includes active video, control preamble sequences, and ancillary data that may be embedded in horizontal and vertical blanking intervals. Data transfer starts immediately after synchronization to Field 1. Data is transferred to or from the synchronous channels through eight DMA engines that work autonomously from the processor core.

DYNAMIC POWER MANAGEMENT

The ADSP-BF534/ADSP-BF536/ADSP-BF537 processors provide five operating modes, each with a different performance and power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode. Also, see Table 16, Table 15 and Table 17.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing capability for maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Dynamic Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. In this mode, the CLKIN to CCLK multiplier ratio can be changed, although the changes are not realized until the full-on mode is entered. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the PLL through the PLL control register (PLL_CTL). If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity wakes up the processor. When in the sleep mode, asserting wake-up causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

System DMA access to L1 memory is not supported in sleep mode.

Table 4. Power Settings

Mode	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Internal Power (V_{DDINT})
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	—	Disabled	Enabled	On
Deep Sleep	Disabled	—	Disabled	Disabled	On
Hibernate	Disabled	—	Disabled	Disabled	Off

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but cannot access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. When in deep sleep mode, an RTC asynchronous interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full-on mode.

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Port H: GPIO/10/100 Ethernet MAC (On ADSP-BF534, these pins are GPIO only)			
PH0 – GPIO/*ETxD0*	I/O	GPIO/*Ethernet MII or RMII Transmit D0*	E
PH1 – GPIO/*ETxD1*	I/O	GPIO/*Ethernet MII or RMII Transmit D1*	E
PH2 – GPIO/*ETxD2*	I/O	GPIO/*Ethernet MII Transmit D2*	E
PH3 – GPIO/*ETxD3*	I/O	GPIO/*Ethernet MII Transmit D3*	E
PH4 – GPIO/*ETxEN*	I/O	GPIO/*Ethernet MII or RMII Transmit Enable*	E
PH5 – GPIO/*MII TxCLK/RMII REF_CLK*	I/O	GPIO/*Ethernet MII Transmit Clock/RMII Reference Clock*	E
PH6 – GPIO/*MII* $\overline{PHYINT}$/*RMII* $\overline{MDINT}$	I/O	GPIO/*Ethernet MII PHY Interrupt/RMII Management Data Interrupt* (This pin should be pulled high when used as a hibernate wake-up.)	E
PH7 – GPIO/*COL*	I/O	GPIO/*Ethernet Collision*	E
PH8 – GPIO/*ERxD0*	I/O	GPIO/*Ethernet MII or RMII Receive D0*	E
PH9 – GPIO/*ERxD1*	I/O	GPIO/*Ethernet MII or RMII Receive D1*	E
PH10 – GPIO/*ERxD2*	I/O	GPIO/*Ethernet MII Receive D2*	E
PH11 – GPIO/*ERxD3*	I/O	GPIO/*Ethernet MII Receive D3*	E
PH12 – GPIO/*ERxDV/TACLK5*	I/O	GPIO/*Ethernet MII Receive Data Valid/Alternate Timer5 Input Clock*	E
PH13 – GPIO/*ERxCLK/TACLK6*	I/O	GPIO/*Ethernet MII Receive Clock/Alternate Timer6 Input Clock*	E
PH14 – GPIO/*ERxER/TACLK7*	I/O	GPIO/*Ethernet MII or RMII Receive Error/Alternate Timer7 Input Clock*	E
PH15 – GPIO/*MII CRS/RMII CRS_DV*	I/O	GPIO/*Ethernet MII Carrier Sense/Ethernet RMII Carrier Sense and Receive Data Valid*	E
Port J: SPORT0/TWI/SPI Select/CAN			
PJ0 – MDC	O	Ethernet Management Channel Clock (On ADSP-BF534 processors, do not connect this pin.)	E
PJ1 – MDIO	I/O	Ethernet Management Channel Serial Data (On ADSP-BF534 processors, tie this pin to ground.)	E
PJ2 – SCL	I/O	TWI Serial Clock (This pin is an open-drain output and requires a pull-up resistor.)	F
PJ3 – SDA	I/O	TWI Serial Data (This pin is an open-drain output and requires a pull-up resistor.)	F
PJ4 – DR0SEC/*CANRX/TACI0*	I	SPORT0 Receive Data Secondary/*CAN Receive/Timer0 Alternate Input Capture*	
PJ5 – DT0SEC/*CANTX/SPI SSEL7*	O	SPORT0 Transmit Data Secondary/*CAN Transmit/SPI Slave Select Enable 7*	C
PJ6 – RSCLK0/*TACLK2*	I/O	SPORT0 Receive Serial Clock/*Alternate Timer2 Clock Input*	D
PJ7 – RFS0/*TACLK3*	I/O	SPORT0 Receive Frame Sync/*Alternate Timer3 Clock Input*	C
PJ8 – DR0PRI/*TACLK4*	I	SPORT0 Receive Data Primary/*Alternate Timer4 Clock Input*	
PJ9 – TSCLK0/*TACLK1*	I/O	SPORT0 Transmit Serial Clock/*Alternate Timer1 Clock Input*	D
PJ10 – TFS0/*SPI SSEL3*	I/O	SPORT0 Transmit Frame Sync/*SPI Slave Select Enable 3*	C
PJ11 – DT0PRI/*SPI SSEL2*	O	SPORT0 Transmit Data Primary/*SPI Slave Select Enable 2*	C
Real-Time Clock			
RTXI	I	RTC Crystal Input (This pin should be pulled low when not used.)	
RTXO	O	RTC Crystal Output (Does not three-state in hibernate.)	
JTAG Port			
TCK	I	JTAG Clock	
TDO	O	JTAG Serial Data Out	C
TDI	I	JTAG Serial Data In	
TMS	I	JTAG Mode Select	
$\overline{TRST}$	I	JTAG Reset (This pin should be pulled low if the JTAG port is not used.)	
$\overline{EMU}$	O	Emulation Output	C

Table 9. Pin Descriptions (Continued)

Pin Name	Type	Function	Driver Type[1]
Clock			
CLKIN	I	Clock/Crystal Input	
XTAL	O	Crystal Output (If CLKBUF is enabled, does not three-state during hibernate.)	
CLKBUF	O	Buffered XTAL Output (If enabled, does not three-state during hibernate.)	E
Mode Controls			
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Nonmaskable Interrupt (This pin should be pulled high when not used.)	
BMODE2–0	I	Boot Mode Strap 2-0 (These pins must be pulled to the state required for the desired boot mode.)	
Voltage Regulator			
VROUT1–0	O	External FET Drive (These pins should be left unconnected when not used and are driven high during hibernate.)	
Supplies			
V_{DDEXT}	P	I/O Power Supply	
V_{DDINT}	P	Internal Power Supply	
V_{DDRTC}	P	Real-Time Clock Power Supply (This pin should be connected to V_{DDEXT} when not used and should remain powered at all times.)	
GND	G	External Ground	

[1] See Output Drive Currents on Page 50 for more information about each driver types.

SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 300 MHz, 400 MHz, and 500 MHz speed grade models[2]	0.8	1.2	1.32	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 533 MHz speed grade models[2]	0.8	1.25	1.375	V
V_{DDINT}	Internal Supply Voltage[1]	Nonautomotive 600 MHz speed grade models[2]	0.8	1.3	1.43	V
V_{DDINT}	Internal Supply Voltage[1]	Automotive grade models and +105°C nonautomotive grade models[2]	0.95	1.2	1.32	V
V_{DDEXT}	External Supply Voltage	Nonautomotive grade models[2]	2.25	2.5 or 3.3	3.6	V
V_{DDEXT}	External Supply Voltage	Automotive grade models and +105°C nonautomotive grade models[2]	2.7	3.0 or 3.3	3.6	V
V_{DDRTC}	Real-Time Clock Power Supply Voltage		2.25		3.6	V
V_{IH}	High Level Input Voltage[3, 4]	V_{DDEXT} = Maximum	2.0			V
$V_{IHCLKIN}$	High Level Input Voltage[5]	V_{DDEXT} = Maximum	2.2			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[6]		$0.7 \times V_{DDEXT}$			V
V_{IH5V}	5.0 V Tolerant Pins, High Level Input Voltage[7]	V_{DDEXT} = Maximum	2.0			V
V_{IL}	Low Level Input Voltage[3, 8]	V_{DDEXT} = Minimum			+0.6	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[6]				$0.3 \times V_{DDEXT}$	V
V_{IL5V}	5.0 V Tolerant Pins, Low Level Input Voltage[7]	V_{DDEXT} = Minimum			+0.8	V
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +105°C	–40		+120	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	208-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+95	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
T_J	Junction Temperature	182-Ball Chip Scale Package Ball Grid Array (CSP_BGA) @ $T_{AMBIENT}$ = 0°C to +70°C	0		+100	°C

[1] The regulator can generate V_{DDINT} at levels of 0.85 V to 1.2 V with –5% to +10% tolerance, 1.25 V with –4% to +10% tolerance, and 1.3 V with –0% to +10% tolerance. The required V_{DDINT} is a function of speed grade and operating frequency. See Table 10, Table 11, and Table 12 for details.

[2] See Ordering Guide on Page 67.

[3] Bidirectional pins (DATA15–0, PF15–0, PG15–0, PH15–0, TFS0, TSCLK0, RSCLK0, RFS0, MDIO) and input pins ($\overline{BR}$, ARDY, DR0PRI, DR0SEC, RTXI, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE2–0) of the ADSP-BF534/ADSP-BF536/ADSP-BF537 are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[4] Parameter value applies to all input and bidirectional pins except CLKIN, SDA, and SCL.

[5] Parameter value applies to CLKIN pin only.

[6] Applies to pins PJ2/SCL and PJ3/SDA which are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[7] Applies to pin PJ4/DR0SEC/CANRX/TACI0 which is 5.0 V tolerant (always accepts up to 5.5 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage.

[8] Parameter value applies to all input and bidirectional pins except SDA and SCL.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	300 MHz/400 MHz[1] Min	Typ	Max	500 MHz/533 MHz/600 MHz[2] Min	Typ	Max	Unit
V_{OH}[3]	High Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –0.5 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OH} = –8 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OH} = –6 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
V_{OH}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OH} = –2.0 mA	V_{DDEXT} – 0.5			V_{DDEXT} – 0.5			V
I_{OH}[6]	High Level Output Current	V_{OH} = V_{DDEXT} – 0.5 V Min			–64			–64	mA
I_{OH}[7]		V_{OH} = V_{DDEXT} – 0.5 V Min			–144			–144	mA
V_{OL}[3]	Low Level Output Voltage	V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OL}[4]		V_{DDEXT} = 3.3 V ± 10%, I_{OL} = 8 mA			0.5			0.5	V
		V_{DDEXT} = 2.5 V/3.0 V ± 10%, I_{OL} = 6 mA			0.5			0.5	V
V_{OL}[5]		V_{DDEXT} = 2.5 V/3.0 V/ 3.3 V ± 10%, I_{OL} = 2.0 mA			0.5			0.5	V
I_{OL}[6]	Low Level Output Current	V_{OL} = 0.5 V Max			64			64	mA
I_{OL}[7]		V_{OL} = 0.5 V Max			144			144	mA
I_{IH}	High Level Input Current[8]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{IH5V}	High Level Input Current[9]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{IL}	Low Level Input Current[2]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA
I_{IHP}	High Level Input Current JTAG[10]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			50			50	µA
I_{OZH}	Three-State Leakage Current[11]	V_{DDEXT} = 3.6 V, V_{IN} = 3.6 V			10			10	µA
I_{OZH5V}	Three-State Leakage Current[12]	V_{DDEXT} = 3.6 V, V_{IN} = 5.5 V			10			10	µA
I_{OZL}	Three-State Leakage Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10			10	µA

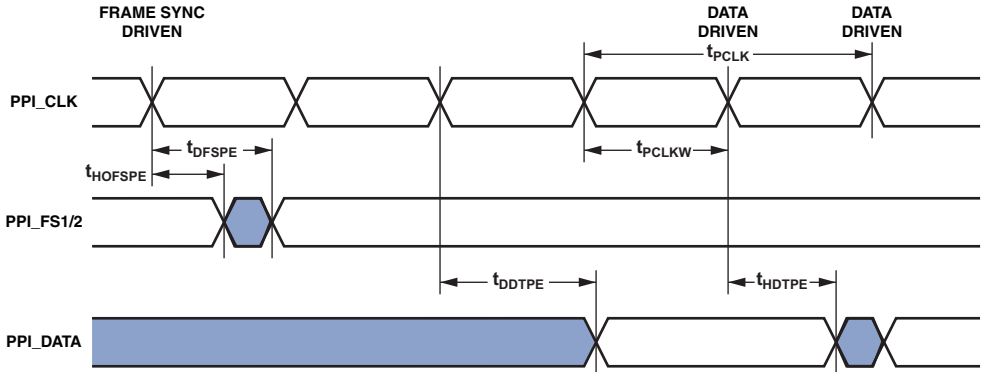

Figure 18. PPI GP Tx Mode with Internal Frame Sync Timing

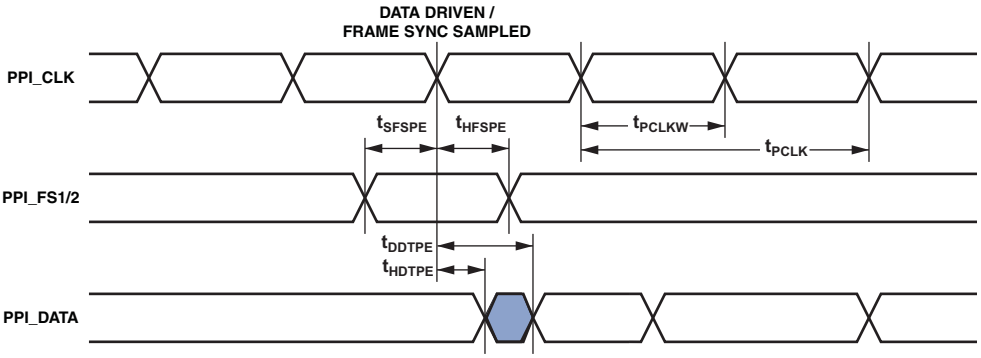

Figure 19. PPI GP Tx Mode with External Frame Sync Timing

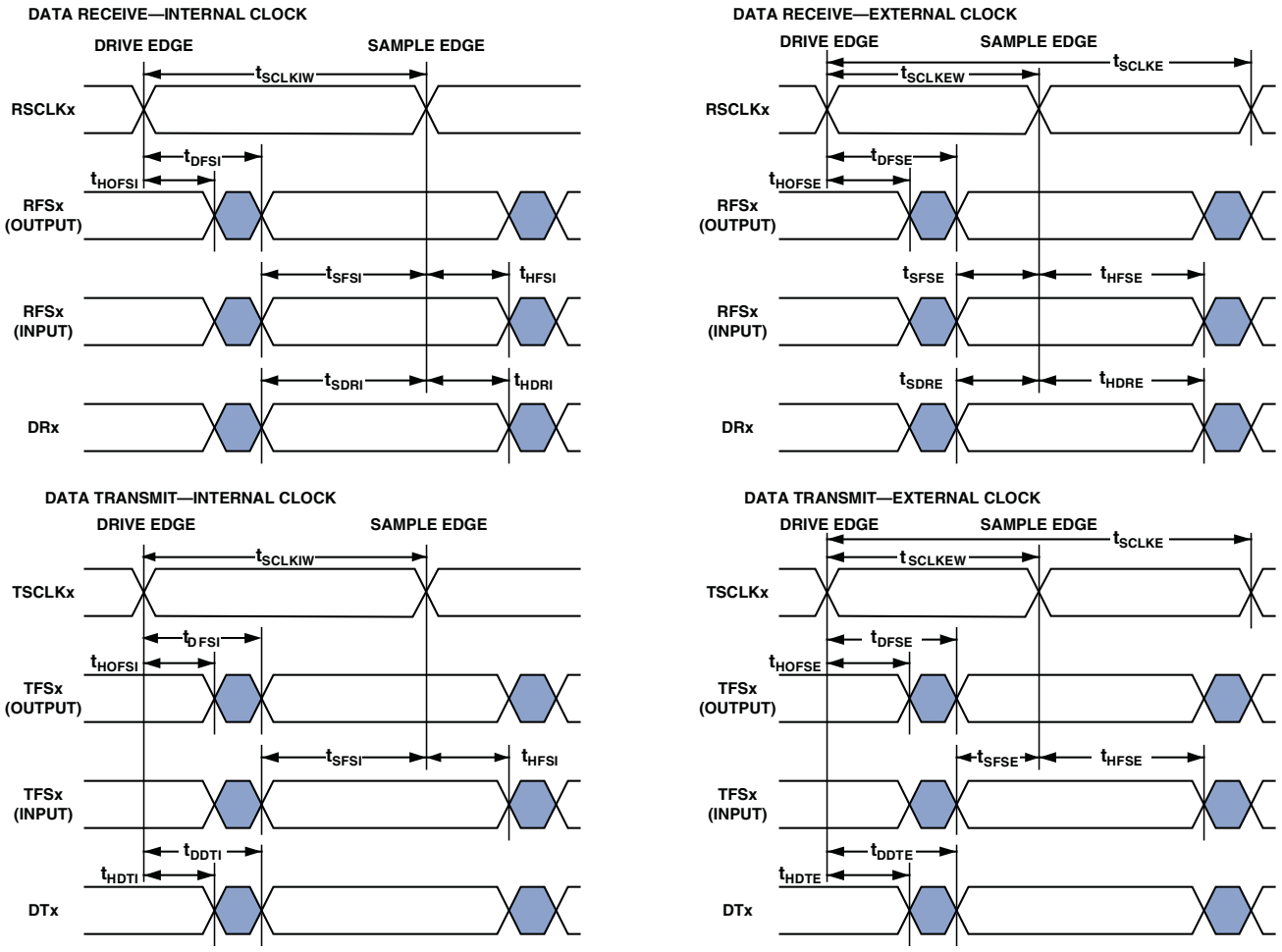

Figure 20. Serial Ports

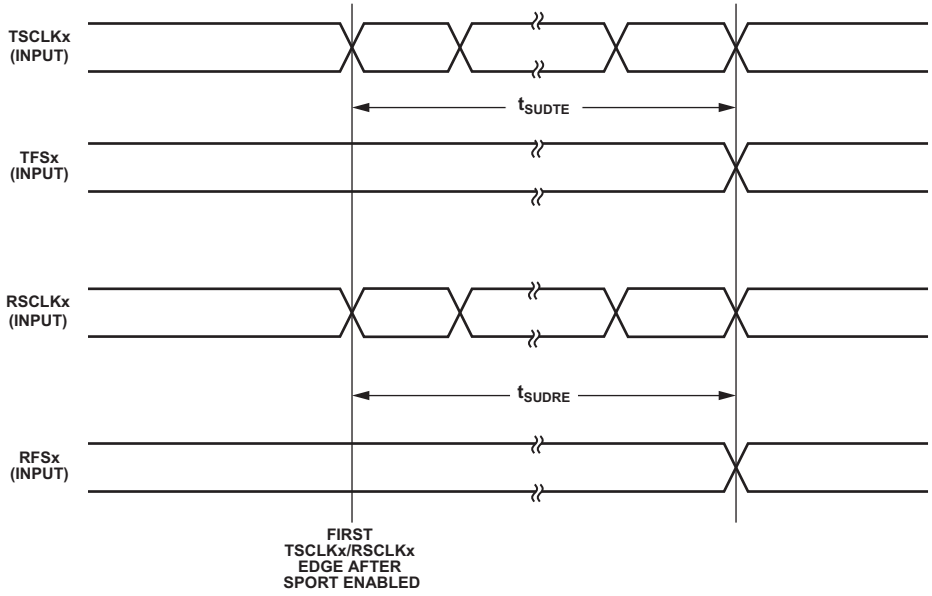

Figure 21. Serial Port Start Up with External Clock and Frame Sync

10/100 Ethernet MAC Controller Timing

Table 40 through Table 45 and Figure 30 through Figure 35 describe the 10/100 Ethernet MAC controller operations. This feature is only available on the ADSP-BF536 and ADSP-BF537 processors.

Table 40. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

Parameter[1]		Min	Max	Unit
f_{ERXCLK}	ERxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1% f_{SCLK} + 1%	MHz
$t_{ERXCLKW}$	ERxCLK Width (t_{ERxCLK} = ERxCLK Period)	t_{ERxCLK} × 35%	t_{ERxCLK} × 65%	ns
$t_{ERXCLKIS}$	Rx Input Valid to ERxCLK Rising Edge (Data In Setup)	7.5		ns
$t_{ERXCLKIH}$	ERxCLK Rising Edge to Rx Input Invalid (Data In Hold)	7.5		ns

[1] MII inputs synchronous to ERxCLK are ERxD3–0, ERxDV, and ERxER.

Table 41. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

Parameter[1]		Min	Max	Unit
f_{ETXCLK}	ETxCLK Frequency (f_{SCLK} = SCLK Frequency)	None	25 + 1% f_{SCLK} + 1%	MHz
$t_{ETXCLKW}$	ETxCLK Width (t_{ETXCLK} = ETxCLK Period)	t_{ETxCLK} × 35%	t_{ETxCLK} × 65%	ns
$t_{ETXCLKOV}$	ETxCLK Rising Edge to Tx Output Valid (Data Out Valid)		20	ns
$t_{ETXCLKOH}$	ETxCLK Rising Edge to Tx Output Invalid (Data Out Hold)	0		ns

[1] MII outputs synchronous to ETxCLK are ETxD3–0.

Table 42. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

Parameter[1]		Min	Max	Unit
f_{REFCLK}	REF_CLK Frequency (f_{SCLK} = SCLK Frequency)	None	50 + 1% 2 × f_{SCLK} + 1%	MHz
$t_{REFCLKW}$	REF_CLK Width (t_{REFCLK} = REFCLK Period)	t_{REFCLK} × 35%	t_{REFCLK} × 65%	ns
$t_{REFCLKIS}$	Rx Input Valid to RMII REF_CLK Rising Edge (Data In Setup)	4		ns
$t_{REFCLKIH}$	RMII REF_CLK Rising Edge to Rx Input Invalid (Data In Hold)	2		ns

[1] RMII inputs synchronous to RMII REF_CLK are ERxD1–0, RMII CRS_DV, and ERxER.

Table 43. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

Parameter[1]		Min	Max	Unit
$t_{REFCLKOV}$	RMII REF_CLK Rising Edge to Tx Output Valid (Data Out Valid)		7.5	ns
$t_{REFCLKOH}$	RMII REF_CLK Rising Edge to Tx Output Invalid (Data Out Hold)	2		ns

[1] RMII outputs synchronous to RMII REF_CLK are ETxD1–0.

Table 44. 10/100 Ethernet MAC Controller Timing: MII/RMII Asynchronous Signal

Parameter[1, 2]		Min	Max	Unit
t_{ECOLH}	COL Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECOLL}	COL Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns
		$t_{ERxCLK} \times 1.5$		ns
t_{ECRSH}	CRS Pulse Width High	$t_{ETxCLK} \times 1.5$		ns
t_{ECRSL}	CRS Pulse Width Low	$t_{ETxCLK} \times 1.5$		ns

[1] MII/RMII asynchronous signals are COL, CRS. These signals are applicable in both MII and RMII modes. The asynchronous COL input is synchronized separately to both the ETxCLK and the ERxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of the slower of the two clocks.
[2] The asynchronous CRS input is synchronized to the ETxCLK, and must have a minimum pulse width high or low at least 1.5 times the period of ETxCLK.

Table 45. 10/100 Ethernet MAC Controller Timing: MII Station Management

Parameter[1]		Min	Max	Unit
t_{MDIOS}	MDIO Input Valid to MDC Rising Edge (Setup)	10		ns
t_{MDCIH}	MDC Rising Edge to MDIO Input Invalid (Hold)	10		ns
t_{MDCOV}	MDC Falling Edge to MDIO Output Valid	25		ns
t_{MDCOH}	MDC Falling Edge to MDIO Output Invalid (Hold)	–1		ns

[1] MDC/MDIO is a 2-wire serial bidirectional port for controlling one or more external PHYs. MDC is an output clock whose minimum period is programmable as a multiple of the system clock SCLK. MDIO is a bidirectional data line.

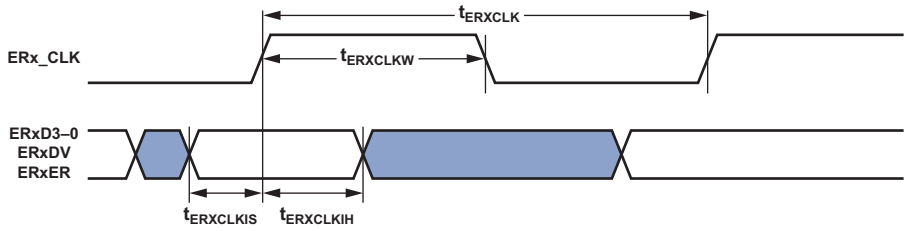

Figure 30. 10/100 Ethernet MAC Controller Timing: MII Receive Signal

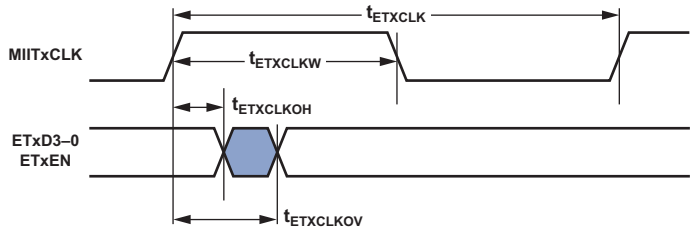

Figure 31. 10/100 Ethernet MAC Controller Timing: MII Transmit Signal

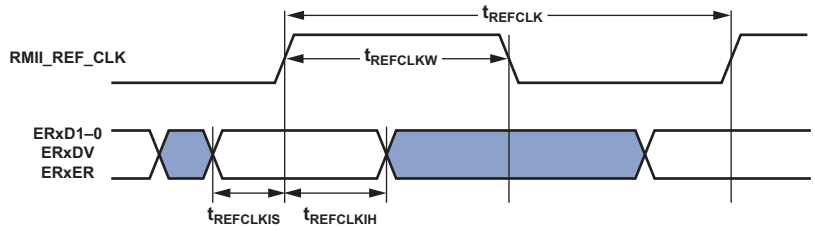

Figure 32. 10/100 Ethernet MAC Controller Timing: RMII Receive Signal

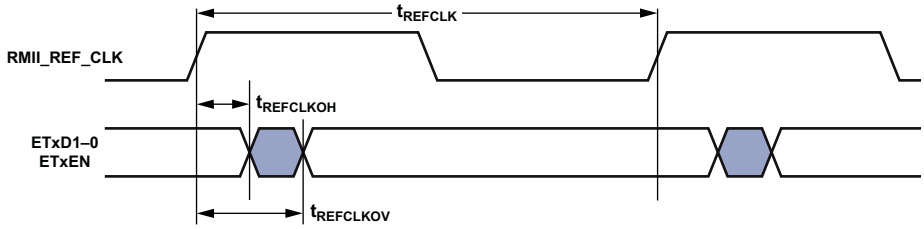

Figure 33. 10/100 Ethernet MAC Controller Timing: RMII Transmit Signal

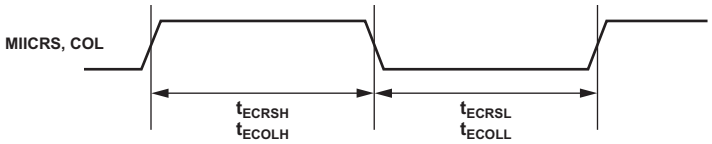

Figure 34. 10/100 Ethernet MAC Controller Timing: Asynchronous Signal

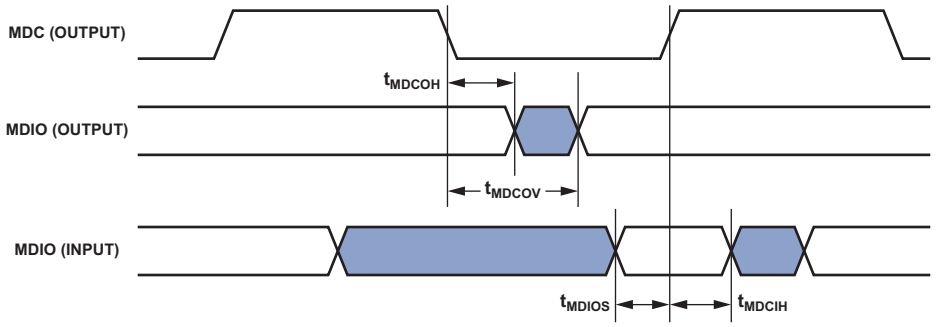

Figure 35. 10/100 Ethernet MAC Controller Timing: MII Station Management

OUTPUT DRIVE CURRENTS

Figure 36 through Figure 47 show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage. See Table 9 on Page 19 for information about which driver type corresponds to a particular pin.

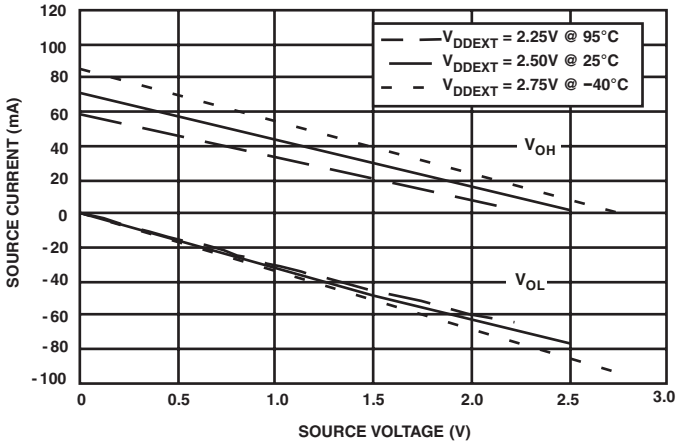

Figure 36. Drive Current A (Low V_{DDEXT})

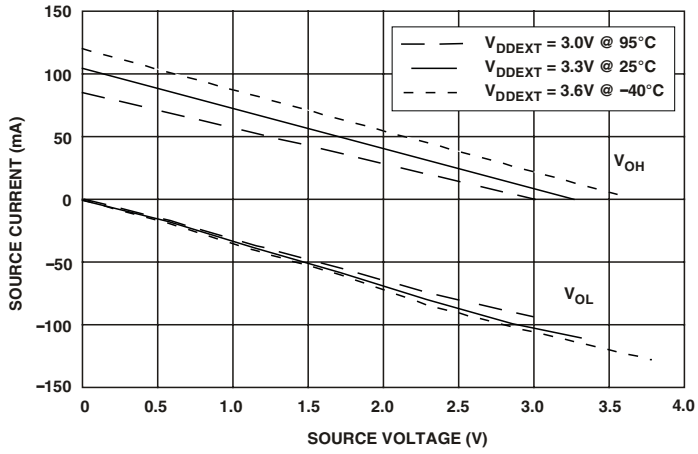

Figure 37. Drive Current A (High V_{DDEXT})

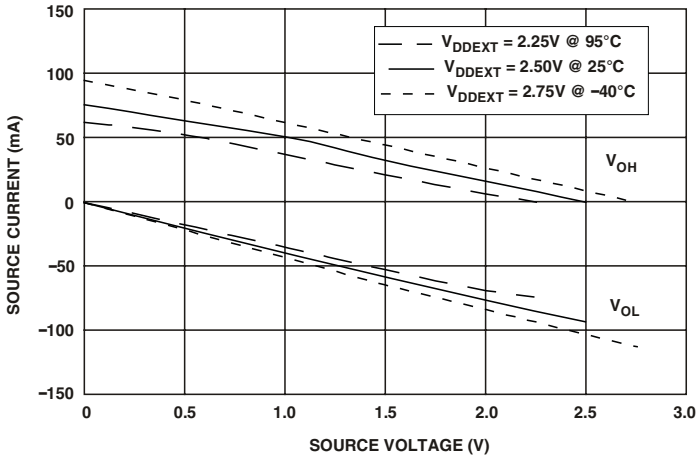

Figure 38. Drive Current B (Low V_{DDEXT})

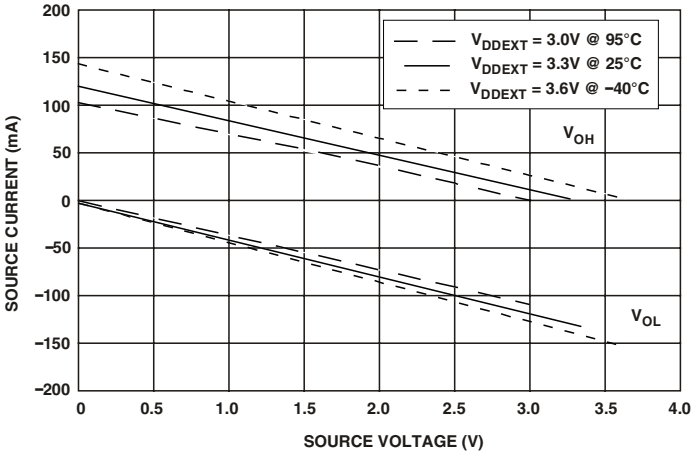

Figure 39. Drive Current B (High V_{DDEXT})

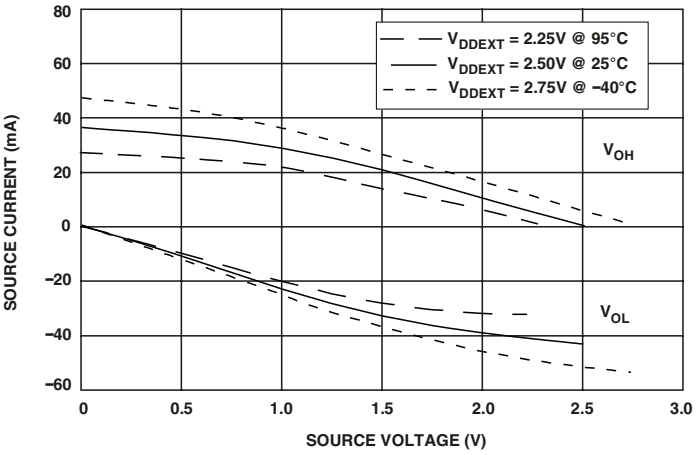

Figure 40. Drive Current C (Low V_{DDEXT})

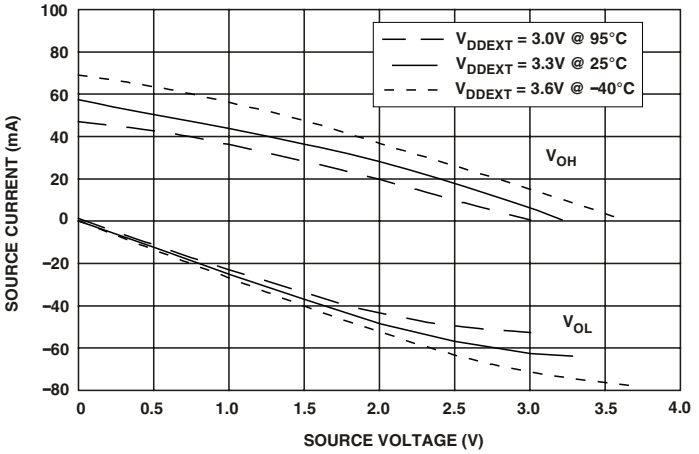

Figure 41. Drive Current C (High V_{DDEXT})

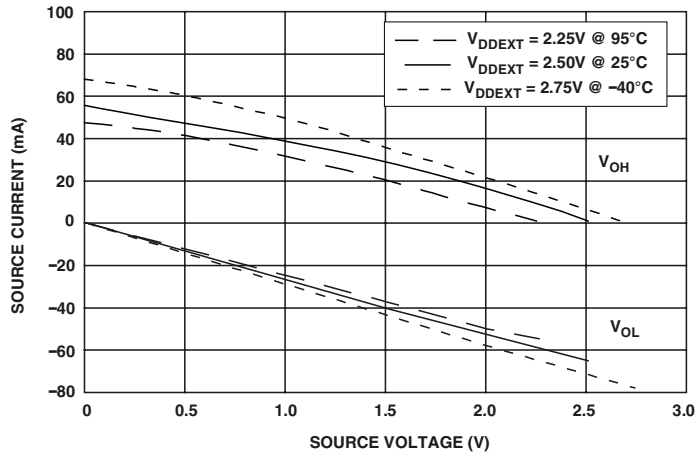

Figure 42. Drive Current D (Low V_{DDEXT})

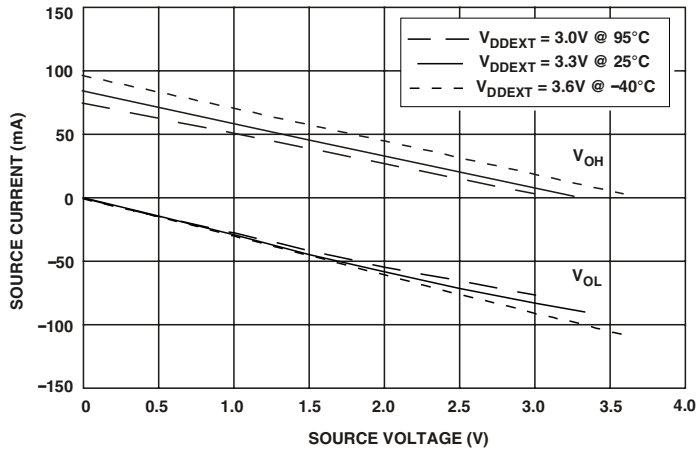

Figure 43. Drive Current D (High V_{DDEXT})

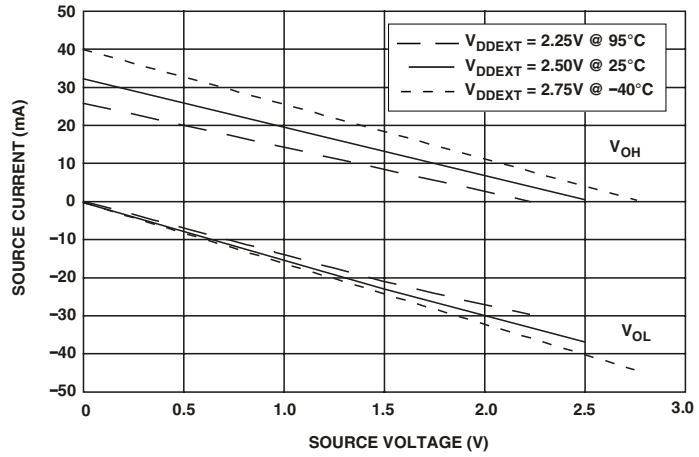

Figure 44. Drive Current E (Low V_{DDEXT})

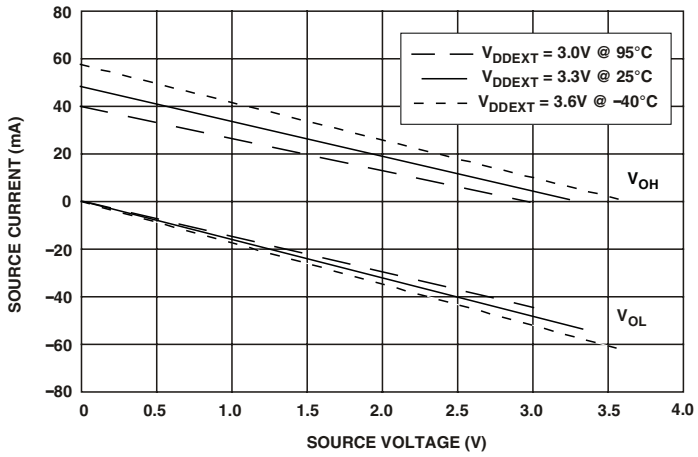

Figure 45. Drive Current E (High V_{DDEXT})

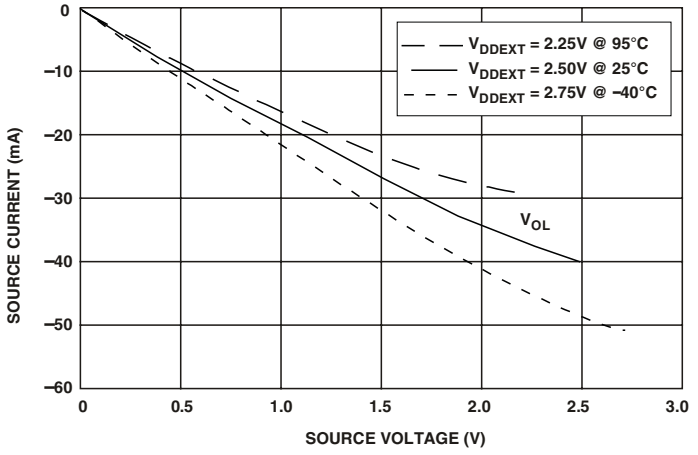

Figure 46. Drive Current F (Low V_{DDEXT})

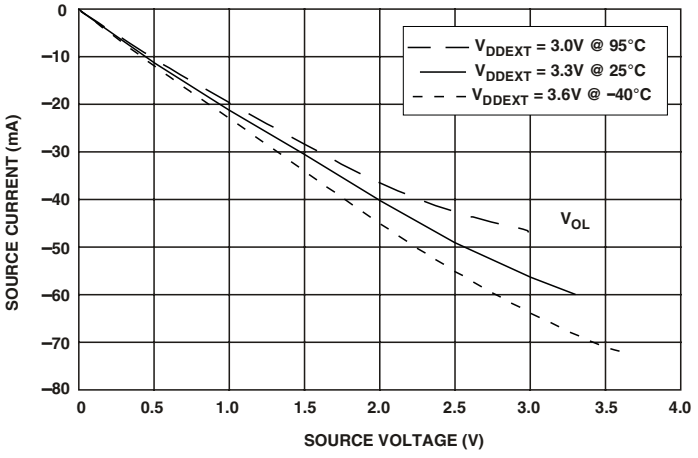

Figure 47. Drive Current F (High V_{DDEXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 48 shows the measurement point for ac measurements (other than output enable/disable). The measurement point is $V_{MEAS} = V_{DDEXT}/2$.

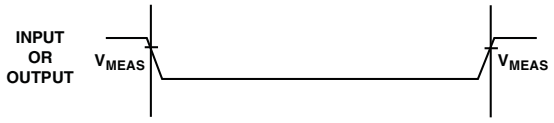

Figure 48. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the Output Enable/Disable diagram (Figure 49). The time $t_{ENA\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage reaches 2.0 V (output high) or 1.0 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.0 V or 2.0 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 49. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output-high or output-low voltage. The time t_{DECAY} is calculated with the test loads C_L and I_L, and with ΔV equal to 0.5 V.

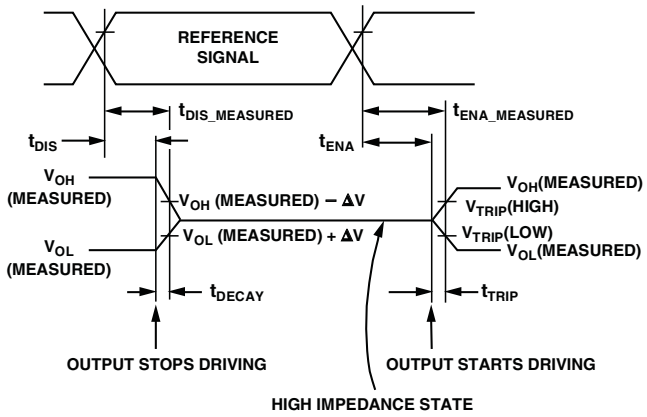

Figure 49. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the processor's output voltage and the input threshold for the device requiring the hold time. A typical ΔV is 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time is t_{DECAY} plus the minimum disable time (for example, t_{DSDAT} for an SDRAM write cycle).

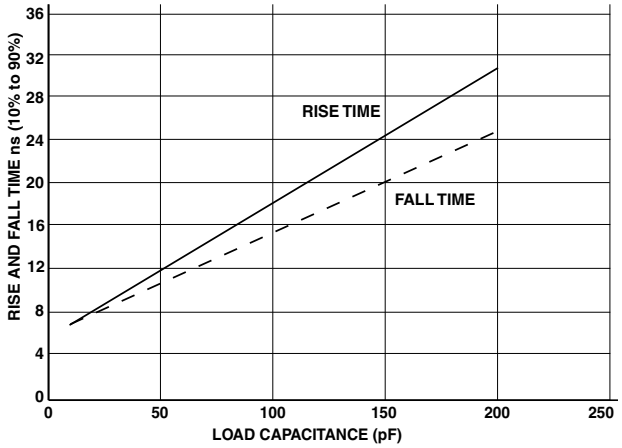

Figure 59. Typical Output Delay or Hold for Driver E at V_{DDEXT} Min

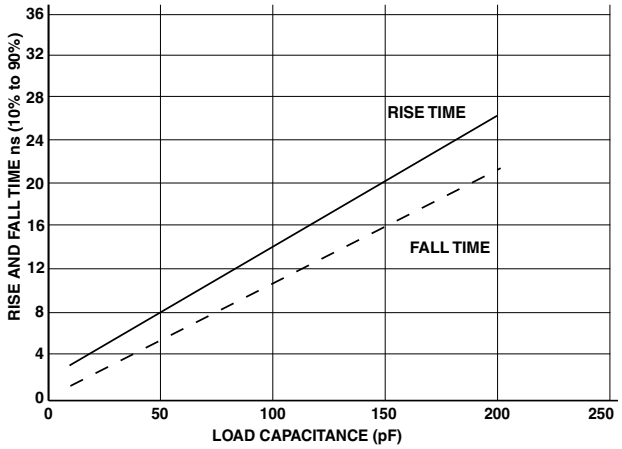

Figure 60. Typical Output Delay or Hold for Driver E at V_{DDEXT} Max

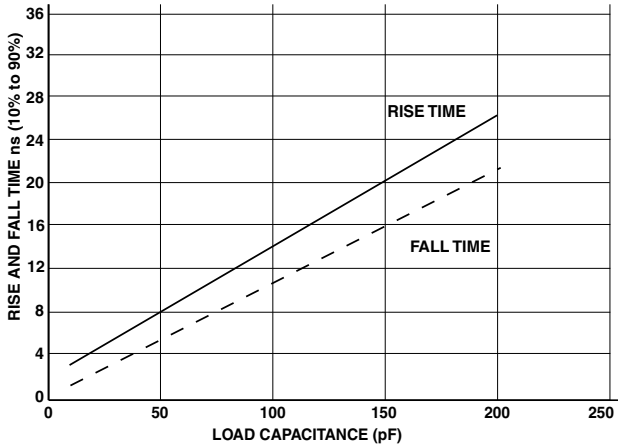

Figure 61. Typical Output Delay or Hold for Driver F at V_{DDEXT} Min

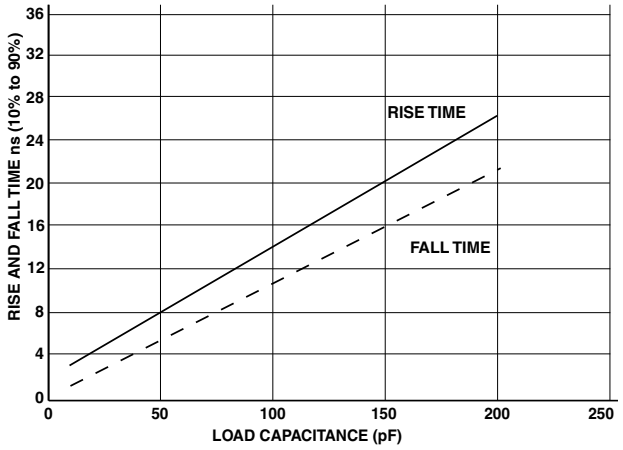

Figure 62. Typical Output Delay or Hold for Driver F at V_{DDEXT} Max

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 46

P_D = Power dissipation (see the power dissipation discussion and the tables on Page 27 for the method to calculate P_D).

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required. Values of θ_{JB} are provided for package comparison and printed circuit board design considerations.

In Table 46 through Table 48, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board and thermal via design comply with JEDEC standards JESD51-9 (BGA). The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

Industrial applications using the 208-ball BGA package require thermal vias, to an embedded ground plane, in the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Table 46. Thermal Characteristics (182-Ball BGA)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	32.80	°C/W
θ_{JMA}	1 Linear m/s Airflow	29.30	°C/W
θ_{JMA}	2 Linear m/s Airflow	28.00	°C/W
θ_{JB}		20.10	°C/W
θ_{JC}		7.92	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.19	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.35	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.45	°C/W

Table 47. Thermal Characteristics (208-Ball BGA without Thermal Vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	23.30	°C/W
θ_{JMA}	1 Linear m/s Airflow	20.20	°C/W
θ_{JMA}	2 Linear m/s Airflow	19.20	°C/W
θ_{JB}		13.05	°C/W
θ_{JC}		6.92	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.18	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.27	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.32	°C/W

Table 48. Thermal Characteristics (208-Ball BGA with Thermal Vias in PCB)

Parameter	Condition	Typical	Unit
θ_{JA}	0 Linear m/s Airflow	22.60	°C/W
θ_{JMA}	1 Linear m/s Airflow	19.40	°C/W
θ_{JMA}	2 Linear m/s Airflow	18.40	°C/W
θ_{JB}		13.20	°C/W
θ_{JC}		6.85	°C/W
Ψ_{JT}	0 Linear m/s Airflow	0.16	°C/W
Ψ_{JT}	1 Linear m/s Airflow	0.27	°C/W
Ψ_{JT}	2 Linear m/s Airflow	0.32	°C/W

Figure 63 shows the top view of the CSP_BGA ball configuration. Figure 64 shows the bottom view of the CSP_BGA ball configuration.

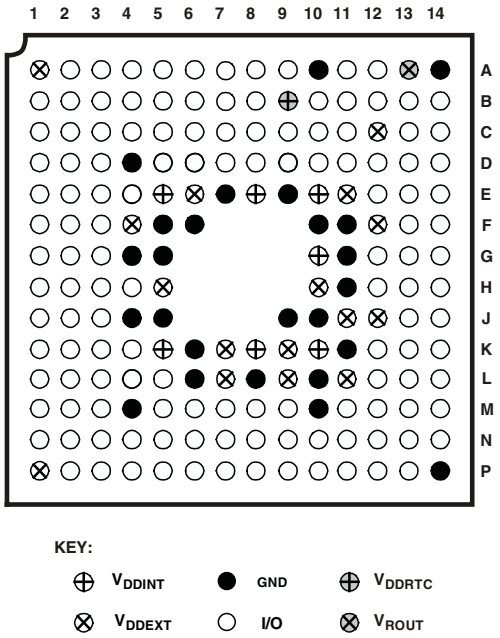

Figure 63. 182-Ball CSP_BGA Configuration (Top View)

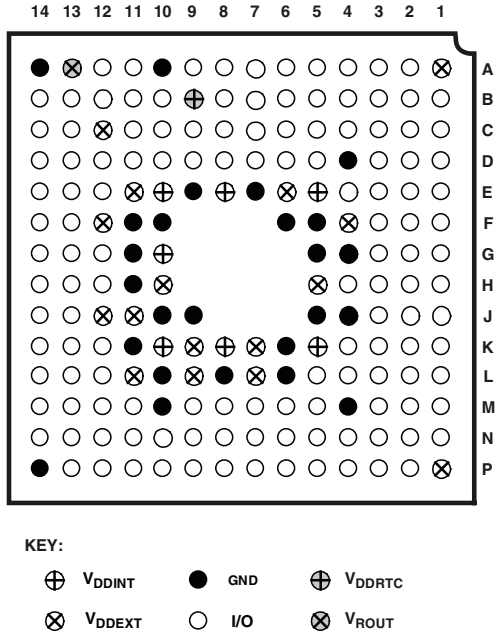

Figure 64. 182-Ball CSP_BGA Configuration (Bottom View)

AUTOMOTIVE PRODUCTS

The ADBF534W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 53 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 53. Automotive Products

Product Family[1,2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF534WBBCZ4Axx	–40°C to +85°C	400 MHz	182-Ball CSP_BGA	BC-182
ADBF534WBBCZ4Bxx	–40°C to +85°C	400 MHz	208-Ball CSP_BGA	BC-208-2
ADBF534WYBCZ4Bxx	–40°C to +105°C	400 MHz	208-Ball CSP_BGA	BC-208-2

[1] Z = RoHS compliant part.
[2] xx denotes silicon revision.
[3] Referenced temperature is ambient temperature.