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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	12MHz
Connectivity	UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86e2112vsc00tr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



CUSTOMER P ROCUREMENT S PECIFICA TION

Z86E21 CMOS Z8[®] OTP MICROCONTROLLER

GENERAL DESCRIPTION

The Z86E21 microcontroller (MCU) introduces the next level of sophistication to single-chip architecture. The Z86E21 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general purpose RAM.

The Z86E21 is a pin compatible, One-Time-Programmable (OTP) version of the Z86C21. The Z86E21 contains 8 Kbytes of EPROM memory in place of the 8 Kbyte of ROM on the Z86C21.

The MCU is housed in a 40-pin DIP, 44-pin Leaded Chip-Carrier, or a 44-pin Quad Flat Pack, and is manufactured in CMOS technology. The ROMless pin option is available on the 44-pin versions only. The MCU can address both external memory and preprogrammed ROM which enables this Z8 microcomputer to be used in high volume applications or where code flexibility is required.

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E21 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The device applications demand powerful I/O capabilities. The Z86E21 fulfills this with 32-pin dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory and 236 General-Purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the Z86E21 offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter (UART) (see Functional Block Description).

In ROM Protect Mode, the instructions LDC, LDCI, LDE and LDEI are disabled when reading address locations %0000 to %1FFF.

Notes:

All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{cc}	V _{DD}
Ground	GND	V _{SS}

PRODUCT RECOMMENDATIONS

Zilog recommends the following programming equipment for use with this One-Time-Programmable product:

Device	Zilog Support Tool	Recommended Hardware	Revision Level Software
Z86E21	Z86C1200ZEM ICEBOX™ Emulator* (*Does not support 4K/8K option.)	В	1.5
Z86E21	Data I/O 3900 Programmer* (*Does not support option bits.)		1.1
Z86E21	Data I/O Unisite Programmer* (*Does not support option bits.)		3.7

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time-Programmable products. If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

GENERAL DESCRIPTION (Continued)



Functional Block Diagram

PIN DESCRIPTION

Standard Mode





40-Lead	DIP	Pin	Identif	ication
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Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction
1 2	V _{cc} XTAL2	Power Supply Crystal, Oscillator Clock	Input Output	11 12	GND P32	Ground, GND Port 3 pin 2	Input Input
- 3 4 5	XTAL1 P37 P30	Crystal, Oscillator Clock Port 3 pin 7 Port 3 pin 0	Input Output Input	13-20 21-28 29	P00-P07 P10-P17 P34	Port 0 pin 0,1,2,3,4,5,6,7 Port 1 pin 0,1,2,3,4,5,6,7 Port 3 pin 4	In/Output In/Output Output
6 7 8 9	/RESET R//W /DS /AS	Reset Read/Write Data Strobe Address Strobe	Input Output Output Output	30 31-38 39 40	P33 P20-P27 P31 P36	Port 3 pin 3 Port 2 pin 0,1,2,3,4,5,6,7 Port 3 pin 1 Port 3 pin 6	Input In/Output Input Output
10	P35	Port 3 pin 5	Output				

PIN DESCRIPTION (Continued) Standard Mode



44-Lead PLCC Pin Assignments

44-Lead	PLCC	Pin Id	entifica	ation
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Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction	
1	V _{cc}	Power Supply	Input	14-16	P00-P02	Port 0 pin 0,1,2	In/Output	
2	XTAL2	Crystal, Oscillator Clock	Output	17	R//RL	ROM/ROMless control	Input	
3	XTAL1	Crystal, Oscillator Clock	Input	18-22	P03-P07	Port 0 pin 3,4,5,6,7	In/Output	
4	P37	Port 3 pin 7	Output	23-27	P10-P14	Port 1 pin 0,1,2,3,4	In/Output	
5	P30	Port 3 pin 0	Input	28	N/C	Not Connected	Input	
6	N/C	Not Connected	Input	29-31	P15-P17	Port 1 pin 5,6,7	In/Output	
7	/RESET	Reset	Input	32	P34	Port 3 pin 4	Output	
8	R//W	Read/Write	Output	33	P33	Port 3 pin 3	Input	
9	/DS	Data Strobe	Output	34-38	P20-P24	Port 2 pin 0,1,2,3,4	In/Output	
10	/AS	Address Strobe	Output	39	N/C	Not Connected	Input	
11	P35	Port 3 pin 5	Output	40-42	P25-P27	Port 2 pin 5,6,7	In/Output	
12	GND	Ground, GND	Input	43	P31	Port 3 pin 1	Input	
13	P32	Port 3 pin 2	Input	44	P36	Port 3 pin 6	Output	



44-Lead QFP Pin Assignments

Pin #	Symbol	Function	Direction	Pin #	Symbol	Function	Direction	
1-5	P03-P07	Port 0 pin 3,4,5,6,7	In/Output	31	XTAL1	Crystal, Oscillator Clock	Input	
6	GND	Ground, GND	Input	32	P37	Port 3 pin 7	Output	
7-14	P10-P17	Port 1 pin 0,1,2,3,4,5,6,7	In/Output	33	P30	Port 3 pin 0	Input	
15	P34	Port 3 pin 4	Output	34	/RESET	Reset	Input	
16	P33	Port 3 pin 3	Input	35	R//W	Read/Write	Output	
17-21	P20-P24	Port 2 pin 0,1,2,3,4	In/Output	36	/DS	Data Strobe	Output	
22	GND	Ground, GND	Input	37	/AS	Address Strobe	Output	
23-25	P25-P27	Port 2 pin 5,6,7	In/Output	38	P35	Port 3 pin 5	Output	
26	P31	Port 3 pin 1	Input	39	GND	Ground, GND	Input	
27	P36	Port 3 pin 6	Output	40	P32	Port 3 pin 2	Input	
28	GND	Ground, GND	Input	41-43	P00-P02	Port 0 pin 0,1,2	In/Output	
29	V	Power Supply	Input	44	R//RL	ROM/ROMless control	Input	
30	XŤĂL2	Crystal, Oscillator Clock	Output					

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max l	Jnits
V _{CC} T _{STG} T _A	Supply Voltage* Storage Temp Oper Ambient Temp	-0.3 -65	+7.0 +150 †	V C C

Notes:

* Voltages on all pins with respect to GND.

13.0 V Maximum on P30-P33.

+ See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram). Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.



Test Load Diagram

DC CHARACTERISTICS

		T _A = to +	= 0° C T _A = -40°C +70°C to +105°C		-40°C 05°C	Typical		
Sym	. Parameter	Min	Max	Min	Max	@ 25°C	Units	Conditions
	Max Input Voltage		7		7		V	I _{IN} 250 μA
	Max Input Voltage		13		13		V	P30-P33 Only
V _{CH}	Clock Input High Voltage	3.8	V _{cc}	3.8	V _{cc}		V	Driven by External Clock Generator
V _{CL}	Clock Input Low Voltage	-0.03	0.8	-0.03	0.8		V	Driven by External Clock Generator
V	Input High Voltage	2.0	V _{cc}	2.0	V _{cc}		V	
V	Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
V_	Output High Voltage	2.4		2.4			V	$I_{0H} = -2.0 \text{ mA}$
V _{OL}	Output Low Voltage		0.4		0.4		V	$I_{0L}^{01} = +2.0 \text{ mA}$
V _{RH}	Reset Input High Voltage	3.8	V _{cc}	3.8	V _{cc}		V	
V _{RI}	Reset Input Low Voltage	-0.03	0.8	-0.03	0.8		V	
I,	Input Leakage	-10	10	-10	10		μA	0V V _{IN} +5.25V
I _{OL}	Output Leakage	-10	10	-10	10		μA	0V V _{IN} +5.25V
I	Reset Input Current		-50		-50		μA	$V_{cc} = +5.25V, V_{BI} = 0V$
I _{cc}	Supply Current		50		50	25	mA	@ 12 MHz
00			60		60	35	mA	@ 16 MHz
I _{CC1}	Standby Current		15		15	5	mA	HALT Mode $V_{IN} = 0V, V_{CC} @ 12 MHz$
			20		20	10	mA	HALT Mode $V_{IN} = OV$, $V_{CC} @ 16$ MHz
1 ₀₀₂	Standby Current		20		20	5	μA	STOP Mode $V_{IN} = 0V$, $V_{CC} @ 12$ MHz
002			20		20	5	μA	STOP Mode $V_{IN} = 0V$, $V_{CC} @ 16$ MHz

Notes:

I_{cc2} requires loading TMR (%F1H) with any value prior to STOP execution. Use this sequence:

LD TMR,#00 NOP

AC CHARACTERISTICS External I/O or Memory Read or Write Timing Diagram



External I/O or Memory Read/Write Timing

AC CHARACTERISTICS External I/O or Memory Read and Write Timing Table

			$T_A = 0^{\circ}C$ to $70^{\circ}C$			$T_{A} = -40^{\circ}C \text{ to } 105^{\circ}C$						
No	Symbol	Parameter	Max	Min	Max	Min	Max	Min	Max	Min	Units	Notes
1	TdA(AS)	Address Valid to /AS Rise Delay	35		20		35		25		ns	[2,3]
2	TdAS(A)	/AS Rise to Address Float Delay	45		30		45		35		ns	[2,3]
3	TdAS(DR)	/AS Rise to Read Data Req'd Valid		220		180		250		180	ns	[1,2,3]
4	TwAS	/AS Low Width	55		35		55		40		ns	[2,3]
5	TdAZ(DS)	Address Float to /DS Fall	0		0		0		0		ns	
6	TwDSR	/DS (Read) Low Width	185		135		185		135		ns	[1,2,3]
7	TwDSW	/DS (Write) Low Width	110		80		110		80		ns	[1,2,3]
8	TdDSR(DR)	/DS Fall to Read Data Req'd Valid		130		75		130		75	ns	[1,2,3]
9	ThDR(DS)	Read Data to /DS Rise Hold Time	0		0		0		0		ns	[2,3]
10	TdDS(A)	/DS Rise to Address Active Delay	45		35		65		50		ns	[2,3]
11	TdDS(AS)	/DS Rise to /AS Fall Delay	55		30		45		35		ns	[2,3]
12	TdR/W(AS)	R//W Valid to /AS Rise Delay	30		20		33		25		ns	[2,3]
13	TdDS(R/W)	/DS Rise to R//W Not Valid	35		30		50		35		ns	[2,3]
14	TdDW(DSW)	Write Data Valid to /DS Fall (Write) Delay	35		25		35		25		ns	[2,3]
15	TdDS(DW)	/DS Rise to Write Data Not Valid Delay	35		30		55		35		ns	[2,3]
16	TdA(DR)	Address Valid to Read Data Req'd Valid		255		200		310		230	ns	[1,2,3]
17	TdAS(DS)	/AS Rise to /DS Fall Delay	55		40		65		45		ns	[2,3]
18	TdDI(DS)	Data Input Setup to /DS Rise	75		60		75		60		ns	[1,2,3]
19	TdDM(AS)	/DM Valid to /AS Fall Delay	50		30		50		30		ns	[2,3]

Notes:

[1] When using extended memory timing add 2 TpC.

[2] Timing numbers given are for minimum TpC.

[3] See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40TpC + 0.32
2	TdAS(A)	0.59TpC - 3.25
3	TdAS(DR)	2.38TpC + 6.14
4	TwAS	0.66TpC - 1.65
6	TwDSR	2.33TpC - 10.56
7	TwDSW	1.27TpC + 1.67
8	TdDSR(DR)	1.97TpC - 42.5
10	TdDS(A)	0.8TpC
11	TdDS(AS)	0.59TpC - 3.14
12	TdR/W(AS)	0.4TpC
13	TdDS(R/W)	0.8TpC - 15
14	TdDW(DSW)	0.4TpC
15	TdDS(DW)	0.88TpC - 19
16	TdA(DR)	4TpC - 20
17	TdAS(DS)	0.91TpC - 10.7
18	TsDI(DS)	0.8TpC - 10
19	TdDM(AS)	0.9TpC - 26.3

AC CHARACTERISTICS Additional Timing Diagram



Additional Timing

AC CHARACTERISTICS Additional Timing Table

No	Symbol	Parameter		T _A 12 Max	= 0°C MHz Min	to 70° 16 M Max	°C ⁻ Hz 12 Min Ma	Γ _A = -40° 2 MHz ax Min	°C to 1 16 M Max	05°C Hz Min	Units	Notes
1	ТрС	Input Clock Period	83	1000	62.5	1000) 83	1000	62.5	1000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		15		10		15		10	ns	[1]
3	TwC	Input Clock Width	37		21		37		21		ns	[1]
4	TwTinL	Timer Input Low Width	75		50		75		50		ns	[2]
5	TwTinH	Timer Input High Width	3TpC		3TpC)	3TpC		3TpC			[2]
6	TpTin	Timer Input Period	8TpC		8TpC	<u>,</u>	8TpC		8TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		50		70		50		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	3TpC		3TpC)	3TpC		3TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3TpC		3TpC)	3TpC		3TpC			[2,3]

Notes:

[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.

[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

[3] Interrupt references request via Port 3.

[4] Interrupt request via Port 3 (P31-P33).

[5] Interrupt request via Port 30.

AC CHARACTERISTICS Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

			$T_A = 0^{\circ}C$ to $70^{\circ}C$			$T_A = -40^{\circ}C$ to $105^{\circ}C$					
No	Symbol	Parameter	12 M Max	/IHz Min	16 I Max	MHZ Min	12 M Max	/IHz Min	16 N Max	IHz Min	Data Direction
1 2 3	TsDI(DAV) ThDI(DAV) TwDAV	Data In Setup Time Data In Hold Time Data Available Width	0 145 110		0 145 110		0 145 110		0 145 110		IN IN IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	110	115	110	115	110	115	110	115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	0	115	0	115	0	115	0	115	IN
7 8	TcLDAV0(RDY) TcLDAV0(RDY)	Data Out to DAV Fall Delay DAV Fall to RDY Fall Delay	0	ТрС	0	ТрС	0	ТрС	0	ТрС	OUT OUT
9 10 11	TdRDY0(DAV) TwRDY TdRDY0d(DAV)	RDY Fall to DAV Rise Delay RDY Width RDY Rise to DAV Fall Delay	110	115 115	110	115 115	110	115 115	110	115 115	OUT OUT OUT

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Zilog, Inc. 210 East Hacienda Ave. Campbell, CA 95008-6600 Telephone (408) 370-8000 Telex 910-338-7621 FAX 408 370-8056 Internet: http://www.zilog.com