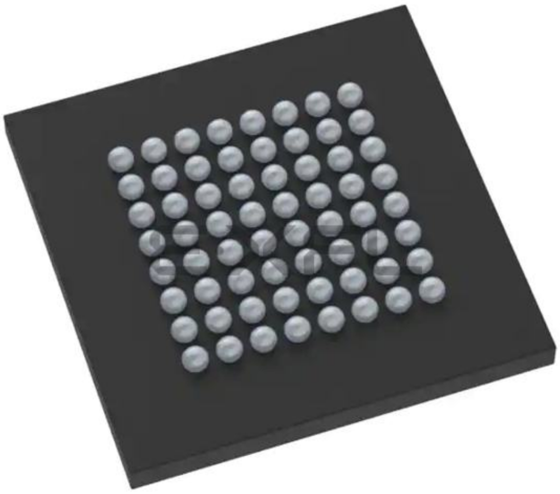

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 51 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-UFBGA, WLCSP |
| Supplier Device Package | 64-WLCSP (4.54x4.91) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rcy6tr |

# Contents

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## 3.7 Memories

The STM32L151xC/C-A and STM32L152xC/C-A devices have the following features:

- 32 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 256 Kbytes of embedded Flash program memory
  - 8 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

## 3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, general-purpose timers, DAC and ADC.

stored by ST in the system memory area, accessible in read-only mode. See *Table 60: Temperature sensor calibration values*.

### 3.10.2 Internal voltage reference ($V_{REFINT}$)

The internal voltage reference ($V_{REFINT}$) provides a stable (bandgap) voltage output for the ADC and Comparators. $V_{REFINT}$ is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the $V_{DD}$ value (when no external voltage, VREF+, is available for ADC). The precise voltage of $V_{REFINT}$ is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 15: Embedded internal reference voltage calibration values*.

## 3.11 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage $V_{REF+}$

Eight DAC trigger inputs are used in the STM32L151xC/C-A and STM32L152xC/C-A devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

## 3.12 Operational amplifier

The STM32L151xC/C-A and STM32L152xC/C-A devices embed two operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 12. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 13. General operating conditions**

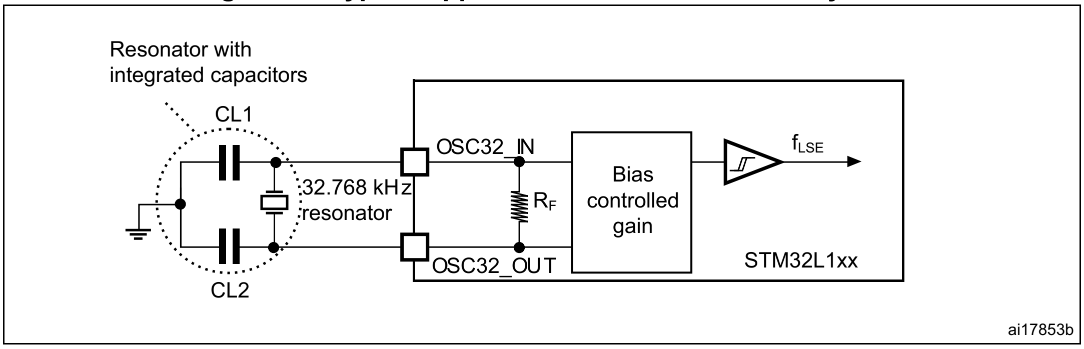
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$[1] | Analog operating voltage (ADC and DAC not used) | Must be the same voltage as $V_{DD}$[2] | 1.65 | 3.6 | V |
| | Analog operating voltage (ADC or DAC used) | | 1.8 | 3.6 | |
| $V_{IN}$ | I/O input voltage | FT pins; 2.0 V ≤$V_{DD}$ | -0.3 | 5.5[3] | V |
| | | FT pins; $V_{DD}$ < 2.0 V | -0.3 | 5.25[3] | |
| | | BOOT0 pin | 0 | 5.5 | |
| | | Any other pin | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7[4] | LQFP144 package | - | 500 | mW |
| | | LQFP100 package | - | 465 | |
| | | LQFP64 package | - | 435 | |
| | | UFBGA132 | - | 333 | |
| | | WLCSP64 package | - | 435 | |
| TA | Ambient temperature for 6 suffix version | Maximum power dissipation[5] | –40 | 85 | °C |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | –40 | 105 | |

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note:* *For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 17). $C_{L1}$ and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$.*
*Load capacitance $C_L$ has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where $C_{stray}$ is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.*

**Caution:** To avoid exceeding the maximum value of $C_{L1}$ and $C_{L2}$ (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
**Example:** if the user chooses a resonator with a load capacitance of $C_L$ = 6 pF and $C_{stray}$ = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

**Figure 17. Typical application with a 32.768 kHz crystal**



### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 40. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation, LCD levels).

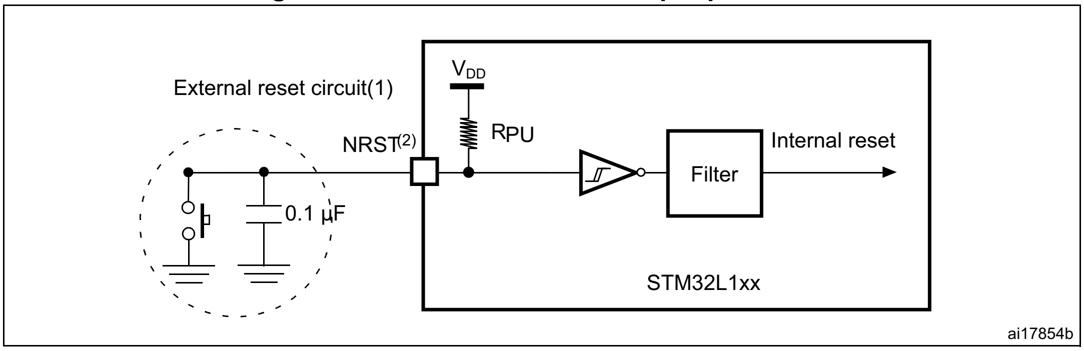
The test results are given in the *Table 41*.

**Table 41. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on all 5 V tolerant (FT) pins | -5 (1) | NA | mA |
| | Injected current on BOOT0 | -0 | NA | |
| | Injected current on any other pin | -5 (1) | +5 | |

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

**Figure 19. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 45*. Otherwise the reset will not be taken into account by the device.

## 6.3.15 TIM timer characteristics

The parameters given in the *Table 46* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output ction characteristics (output compare, input capture, external clock, PWM output).

**Table 46. TIMx[(1)] characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 31.25 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 32 MHz | 0 | 16 | MHz |
| $Res_{TIM}$ | Timer resolution | - | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected (timer's prescaler disabled) | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | 0.0312 | 2048 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 32 MHz | - | 134.2 | s |

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

### SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 13*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 49. SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max(2) | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 16 | MHz |
| | | Slave mode | - | 16 | |
| | | Slave transmitter | - | 12(3) | |
| $t_{r(SCK)}$(2)<br>$t_{f(SCK)}$(2) | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 6 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | $4t_{HCLK}$ | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{HCLK}$ | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode | $t_{SCK}/2-5$ | $t_{SCK}/2+3$ | |
| $t_{su(MI)}$(2) | Data input setup time | Master mode | 5 | - | |
| $t_{su(SI)}$(2) | | Slave mode | 6 | - | |
| $t_{h(MI)}$(2) | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$(2) | | Slave mode | 5 | - | |
| $t_{a(SO)}$(4) | Data output access time | Slave mode | 0 | $3t_{HCLK}$ | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode | - | 33 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode | - | 6.5 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode | 17 | - | |
| $t_{h(MO)}$(2) | | Master mode | 0.5 | - | |

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

**Figure 21. SPI timing diagram - slave mode and CPHA = 0**

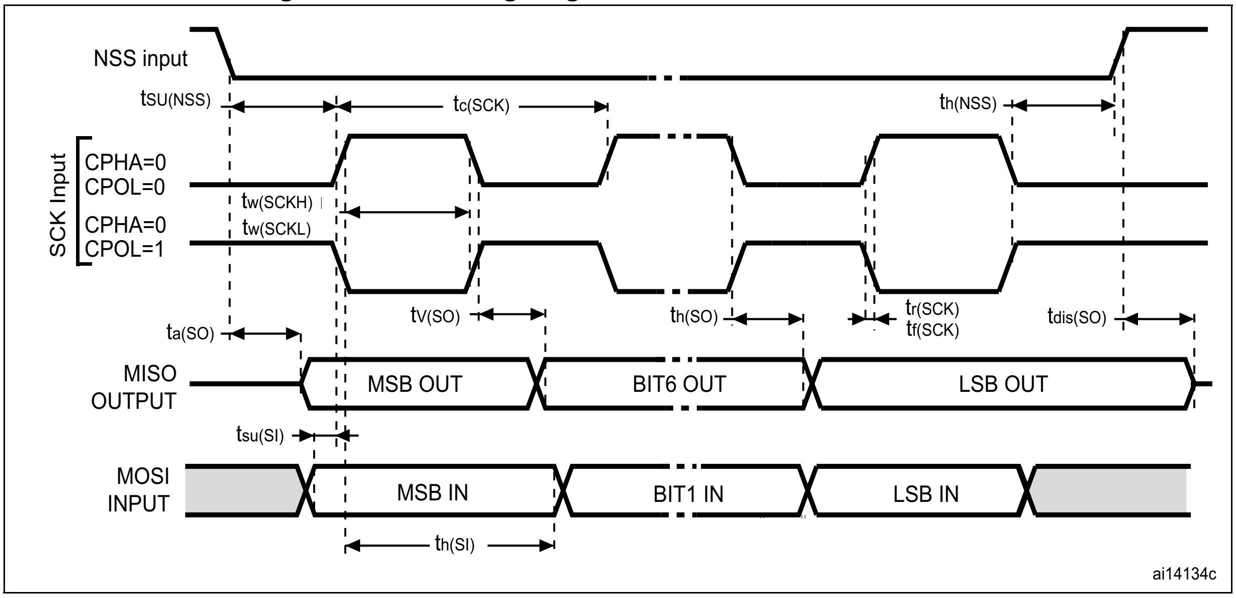
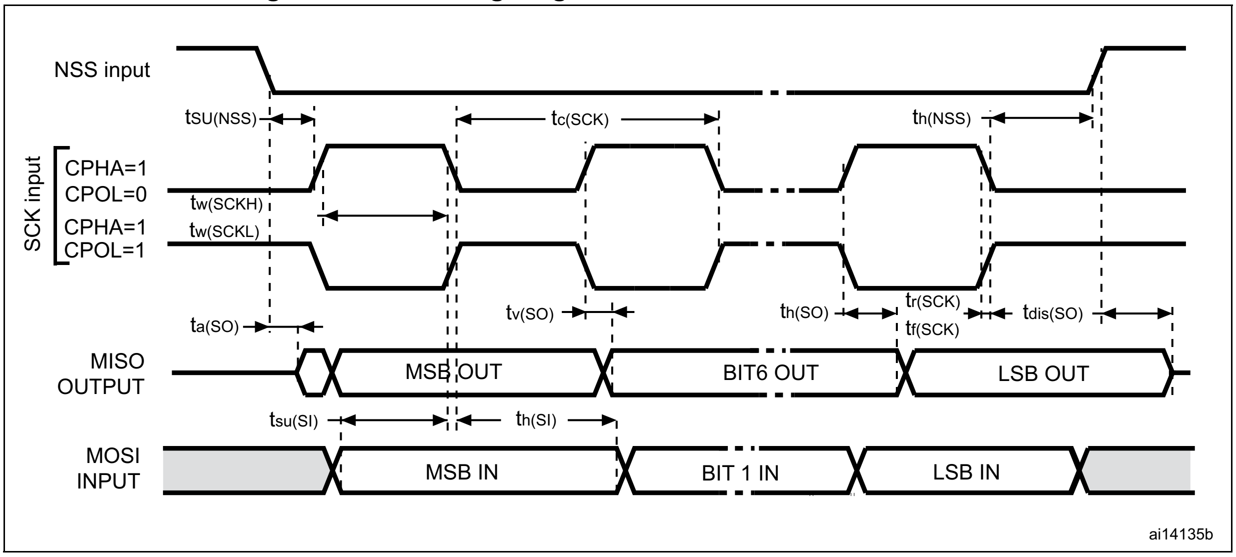



**Figure 22. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 55. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_S$(5) | Sampling time | Direct channels 2.4 V ≤ $V_{DDA}$ ≤ 3.6 V | 0.25 | - | - | µs |
| | | Multiplexed channels 2.4 V ≤ $V_{DDA}$ ≤ 3.6 V | 0.56 | - | - | |
| | | Direct channels 1.8 V ≤ $V_{DDA}$ ≤ 2.4 V | 0.56 | - | - | |
| | | Multiplexed channels 1.8 V ≤ $V_{DDA}$ ≤ 2.4 V | 1 | - | - | |
| | | - | 4 | - | 384 | $1/f_{ADC}$ |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 16 MHz | 1 | - | 24.75 | µs |
| | | - | 4 to 384 (sampling phase) +12 (successive approximation) | | | $1/f_{ADC}$ |
| $C_{ADC}$ | Internal sample and hold capacitor | Direct channels | - | 16 | - | pF |
| | | Multiplexed channels | - | | - | |
| $f_{TRIG}$ | External trigger frequency Regular sequencer | 12-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv | $1/f_{ADC}$ |
| $f_{TRIG}$ | External trigger frequency Injected sequencer | 12-bit conversions | - | - | Tconv+2 | $1/f_{ADC}$ |
| | | 6/8/10-bit conversions | - | - | Tconv+1 | $1/f_{ADC}$ |
| $R_{AIN}$(6) | Signal source impedance | | - | - | 50 | kΩ |
| $t_{lat}$ | Injection trigger conversion latency | $f_{ADC}$ = 16 MHz | 219 | - | 281 | ns |
| | | - | 3.5 | - | 4.5 | $1/f_{ADC}$ |
| $t_{latr}$ | Regular trigger conversion latency | $f_{ADC}$ = 16 MHz | 156 | - | 219 | ns |
| | | - | 2.5 | - | 3.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-up time | - | - | - | 3.5 | µs |

1. The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through VREF is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. $V_{SSA}$ or $V_{REF-}$ must be tied to ground.
5. Minimum sampling time is reached for an external input impedance limited to a value as defined in *Table 57: Maximum source impedance RAIN max*.
6. External impedance has another high value limitation when using short sampling time as defined in *Table 57: Maximum source impedance RAIN max*.

**Figure 29. Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion**

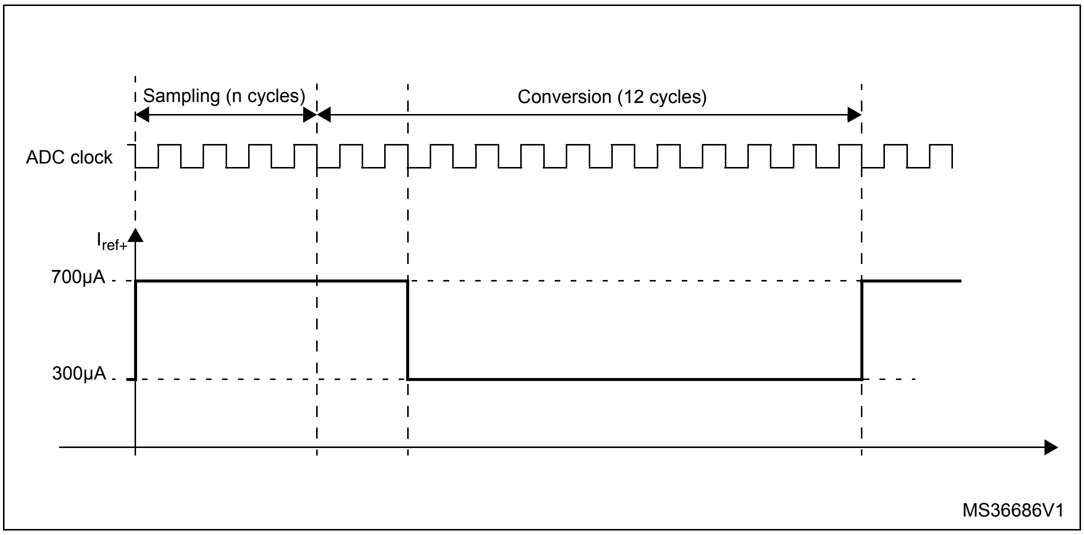



**Table 57. Maximum source impedance $R_{AIN}$ max[(1)]**

| Ts (µs) | $R_{AIN}$ max (kΩ) | | | | Ts (cycles) $f_{ADC}$=16 MHz[(2)] |
|---|---|---|---|---|---|
| | Multiplexed channels | | Direct channels | | |
| | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | |
| 0.25 | Not allowed | Not allowed | 0.7 | Not allowed | 4 |
| 0.5625 | 0.8 | Not allowed | 2.0 | 1.0 | 9 |
| 1 | 2.0 | 0.8 | 4.0 | 3.0 | 16 |
| 1.5 | 3.0 | 1.8 | 6.0 | 4.5 | 24 |
| 3 | 6.8 | 4.0 | 15.0 | 10.0 | 48 |
| 6 | 15.0 | 10.0 | 30.0 | 20.0 | 96 |
| 12 | 32.0 | 25.0 | 50.0 | 40.0 | 192 |
| 24 | 50.0 | 50.0 | 50.0 | 50.0 | 384 |

1. Guaranteed by design.
2. Number of samples calculated for $f_{ADC}$ = 16 MHz. For $f_{ADC}$ = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (µs),

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 11*. The applicable procedure depends on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

**Table 58. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| dOffset/dT[1] | Offset error temperature coefficient (code 0x800) | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer OFF | -20 | -10 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer ON | 0 | 20 | 50 | |
| Gain[1] | Gain error[7] | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ<br>DAC output buffer ON | - | +0.1 / -0.2% | +0.2 / -0.5% | % |
| | | No $R_L$, $C_L \leq 50$ pF<br>DAC output buffer OFF | - | +0 / -0.2% | +0 / -0.4% | |
| dGain/dT[1] | Gain error temperature coefficient | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer OFF | -10 | -2 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer ON | -40 | -8 | 0 | |
| TUE[1] | Total unadjusted error | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ<br>DAC output buffer ON | - | 12 | 30 | LSB |
| | | No $R_L$, $C_L \leq 50$ pF<br>DAC output buffer OFF | - | 8 | 12 | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 7 | 12 | µs |
| Update rate | Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | - | 1 | Msps |
| $t_{WAKEUP}$ | Wakeup time from off state (setting the ENx bit in the DAC Control register)[8] | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 9 | 15 | µs |
| PSRR+ | $V_{DDA}$ supply rejection ratio (static DC measurement) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | -60 | -35 | dB |

1. Data based on characterization results.
2. Connected between DAC_OUT and $V_{SSA}$.
3. Difference between two consecutive codes - 1 LSB.

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

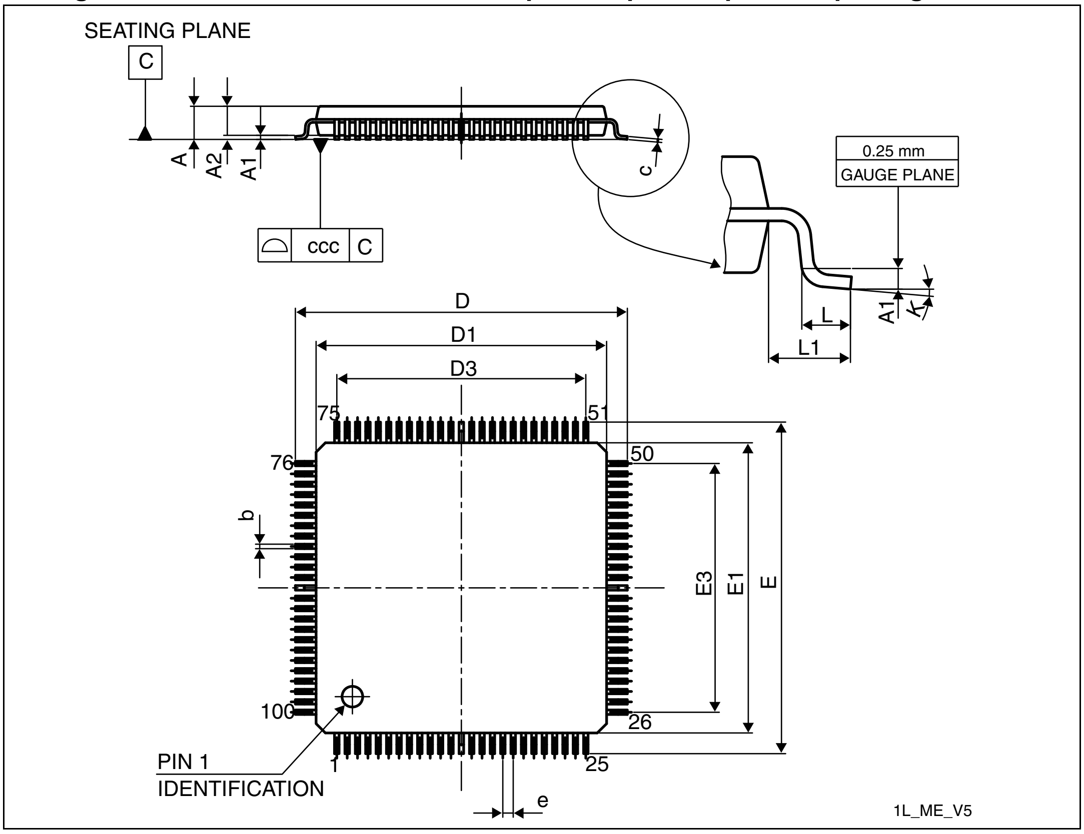
**Table 63. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | - | 3.6 | V |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay(2) in slow mode | $1.65\ V \le V_{DDA} \le 2.7\ V$ | - | 1.8 | 3.5 | |
| | | $2.7\ V \le V_{DDA} \le 3.6\ V$ | - | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay(2) in fast mode | $1.65\ V \le V_{DDA} \le 2.7\ V$ | - | 0.8 | 2 | |
| | | $2.7\ V \le V_{DDA} \le 3.6\ V$ | - | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | | - | ±4 | ±20 | mV |
| dThreshold/dt | Threshold voltage temperature coefficient | $V_{DDA} = 3.3V$<br>$T_A = 0$ to $50\ °C$<br>V- = $V_{REFINT}$,<br>3/4 $V_{REFINT}$,<br>1/2 $V_{REFINT}$,<br>1/4 $V_{REFINT}$. | - | 15 | 100 | ppm/°C |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | - | 0.5 | 2 | |

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

## 7.2 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

**Figure 34. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data**

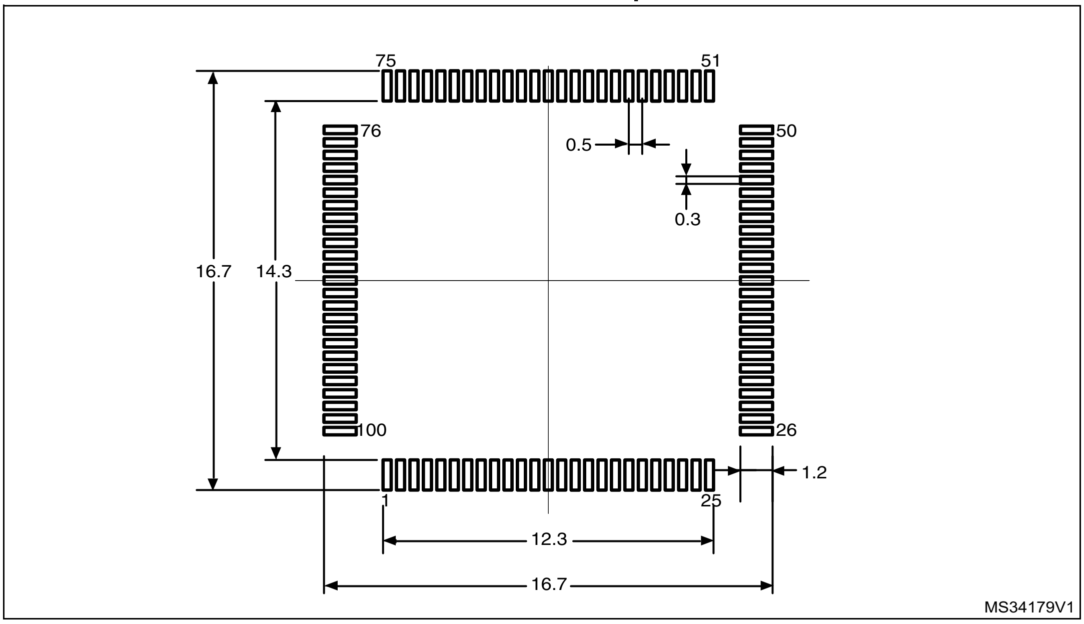
| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.000 | - | - | 0.4724 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |

**Table 66. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 35. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint**




1. Dimensions are in millimeters.

# 9 Revision History

**Table 73. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 01-Apr-2014 | 1 | Initial release. |
| 07-Apr-2014 | 2 | Updated *Table 3: Functionalities depending on the operating power supply range*.<br>Updated *Table 17: Current consumption in Run mode, code with data processing running from Flash*.<br>Modified $I_{DD(LP\ Sleep)}$ (TIM9 and USART1 enabled, Flash ON, VDD from 1.65 V to 3.6 V) in *Table 21: Current consumption in Low-power sleep mode*.<br>Updated $V_{IH(NRST)}$ minimum value in *Table 45: NRST pin characteristics*.<br>Added *Table 41: UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint*.. |
| 12-June-2014 | 3 | Updated title removing memory I/F.<br>Removed ambiguity of “ambient temperature” in the electrical characteristics description.<br>updated *Figure 1* with graphic improvements. |
| 13-Sept-2014 | 4 | Updated *Section 3.17: Communication interfaces* putting I2S characteristics inside.<br>Updated DMIPS features in cover page and *Section 2: Description*.<br>Updated max temperature at 105°C instead of 85°C in the whole datasheet.<br>Updated Flash switched ON & OFF conditions in *Table 19: Current consumption in Sleep mode*.<br>Updated *Table 24: Peripheral current consumption* with new measured current values.<br>Updated *Table 57: Maximum source impedance RAIN max* adding note 2. |