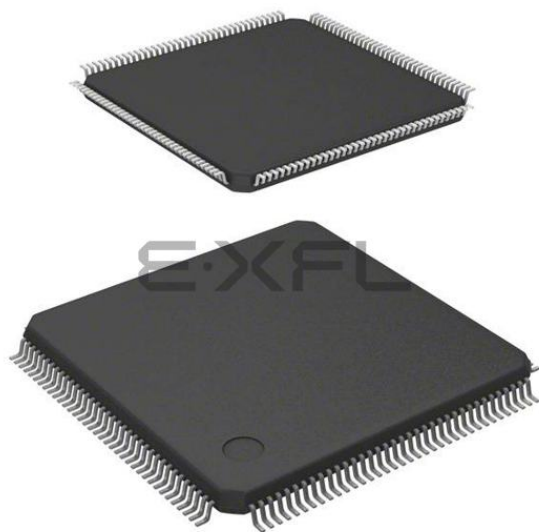




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I ² S, POR, PWM, WDT
Number of I/O	115
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151zct6

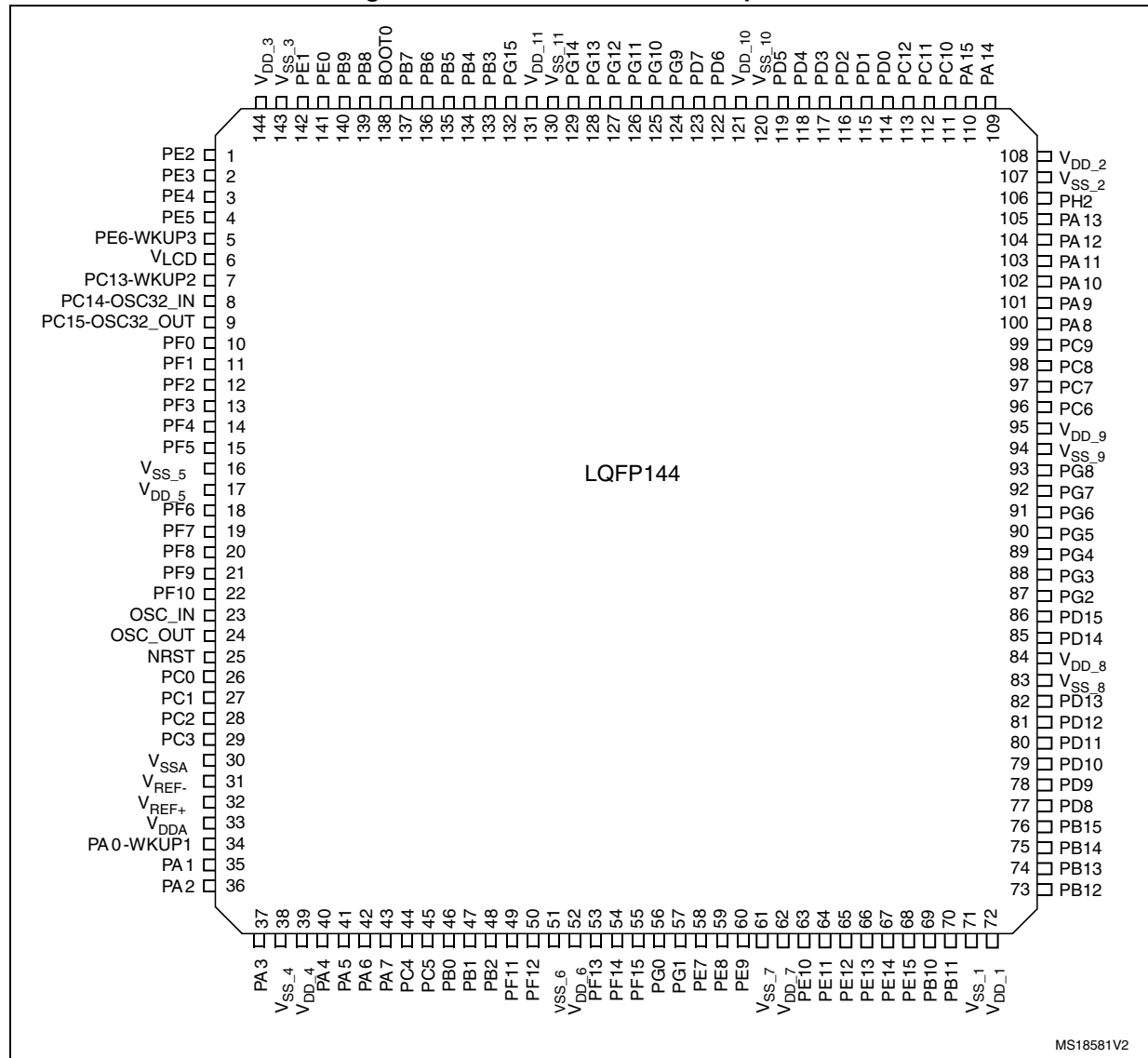
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4 Pin descriptions

Figure 3. STM32L15xZC LQFP144 pinout



MS18581V2

1. This figure shows the package top view.

Table 8. STM32L151xC/C-A and STM32L152xC/C-A pin definitions (continued)

Pins					Pin name	Pin Type ⁽¹⁾	I / O structure	Main function ⁽²⁾ (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
7	C1	7	2	C8	PC13-WKUP2	I/O	FT	PC13	-	WKUP2/ RTC_TAMP1/ RTC_TS/ RTC_OUT
8	D1	8	3	B8	PC14- OSC32_IN ⁽⁴⁾	I/O	TC	PC14	-	OSC32_IN
9	E1	9	4	B7	PC15- OSC32_OUT	I/O	TC	PC15	-	OSC32_OUT
10	D6	-	-	-	PF0	I/O	FT	PF0	-	-
11	D5	-	-	-	PF1	I/O	FT	PF1	-	-
12	D4	-	-	-	PF2	I/O	FT	PF2	-	-
13	E4	-	-	-	PF3	I/O	FT	PF3	-	-
14	F3	-	-	-	PF4	I/O	FT	PF4	-	-
15	F4	-	-	-	PF5	I/O	FT	PF5	-	-
16	F2	10	-	-	V _{SS_5}	S	-	V _{SS_5}	-	-
17	G2	11	-	-	V _{DD_5}	S	-	V _{DD_5}	-	-
18	G3	-	-	-	PF6	I/O	FT	PF6	TIM5_CH1/TIM5_ETR	ADC_IN27
19	G4	-	-	-	PF7	I/O	FT	PF7	TIM5_CH2	ADC_IN28/ COMP1_INP
20	H4	-	-	-	PF8	I/O	FT	PF8	TIM5_CH3	ADC_IN29/ COMP1_INP
21	J6	-	-	-	PF9	I/O	FT	PF9	TIM5_CH4	ADC_IN30/ COMP1_INP
22	-	-	-	-	PF10	I/O	FT	PF10	-	ADC_IN31/ COMP1_INP
23	F1	12	5	D8	PH0- OSC_IN ⁽⁵⁾	I/O	TC	PH0	-	OSC_IN
24	G1	13	6	D7	PH1- OSC_OUT ⁽⁵⁾	I/O	TC	PH1	-	OSC_OUT
25	H2	14	7	C7	NRST	I/O	RST	NRST	-	-
26	H1	15	8	E8	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP

Table 8. STM32L151xC/C-A and STM32L152xC/C-A pin definitions (continued)

Pins					Pin name	Pin Type ⁽¹⁾	I / O structure	Main function ⁽²⁾ (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
53	K7	-	-	-	PF13	I/O	FT	PF13	-	ADC_IN3b
54	J8	-	-	-	PF14	I/O	FT	PF14	-	ADC_IN6b
55	J9	-	-	-	PF15	I/O	FT	PF15	-	ADC_IN7b
56	H9	-	-	-	PG0	I/O	FT	PG0	-	ADC_IN8b
57	G9	-	-	-	PG1	I/O	FT	PG1	-	ADC_IN9b
58	M7	38	-	-	PE7	I/O	TC	PE7	-	ADC_IN22/ COMP1_INP
59	L7	39	-	-	PE8	I/O	TC	PE8	-	ADC_IN23/ COMP1_INP
60	M8	40	-	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR	ADC_IN24/ COMP1_INP
61	-	-	-	-	V _{SS_7}	S	-	V _{SS_7}	-	-
62	-	-	-	-	V _{DD_7}	S	-	V _{DD_7}	-	-
63	L8	41	-	-	PE10	I/O	TC	PE10	TIM2_CH2	ADC_IN25/ COMP1_INP
64	M9	42	-	-	PE11	I/O	FT	PE11	TIM2_CH3	-
65	L9	43	-	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS	-
66	M10	44	-	-	PE13	I/O	FT	PE13	SPI1_SCK	-
67	M11	45	-	-	PE14	I/O	FT	PE14	SPI1_MISO	-
68	M12	46	-	-	PE15	I/O	FT	PE15	SPI1_MOSI	-
69	L10	47	29	G3	PB10	I/O	FT	PB10	TIM2_CH3/I2C2_SCL/ USART3_TX/ LCD_SEG10	-
70	L11	48	30	F3	PB11	I/O	FT	PB11	TIM2_CH4/ I2C2_SDA/ USART3_RX/ LCD_SEG11	-
71	F12	49	31	H2	V _{SS_1}	S	-	V _{SS_1}	-	-
72	G12	50	32	H1	V _{DD_1}	S	-	V _{DD_1}	-	-
73	L12	51	33	G2	PB12	I/O	FT	PB12	TIM10_CH1/I2C2_SMBA/ SPI2_NSS/ I2S2_WS/ USART3_CK/ LCD_SEG12	ADC_IN18/ COMP1_INP



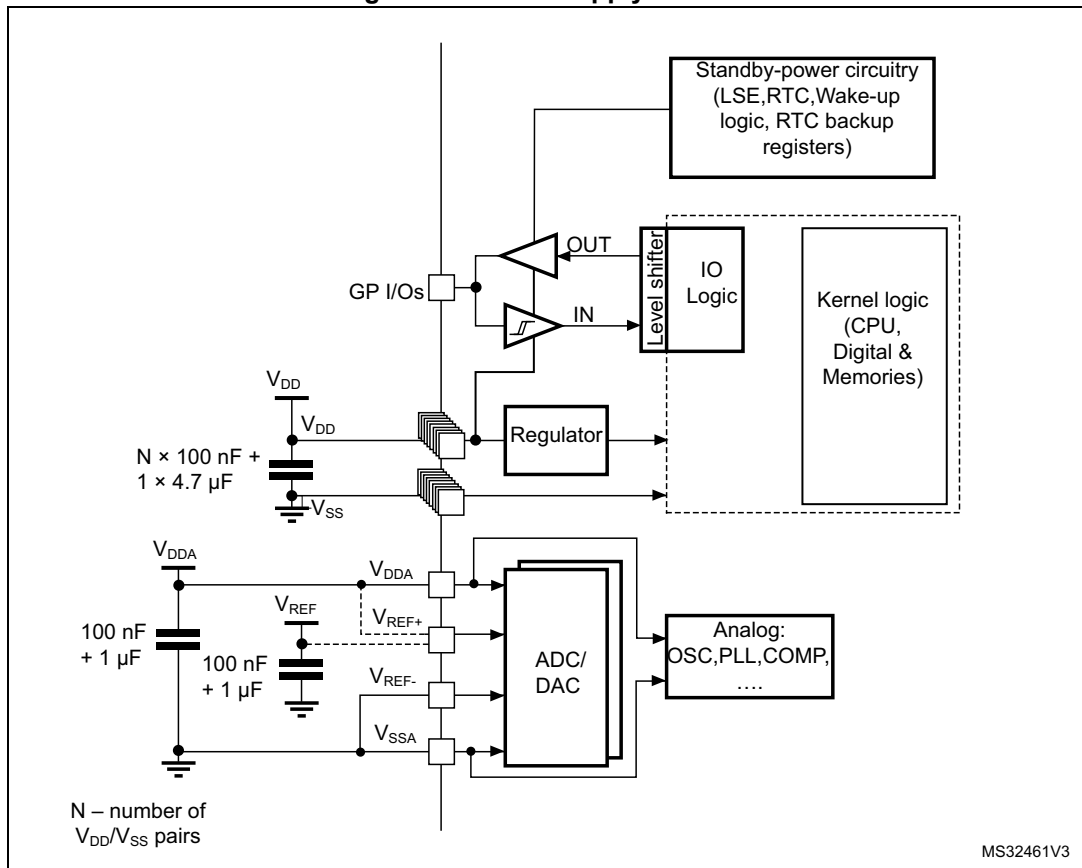
Alternate functions

Table 9. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	AFIO12	..	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	-		LCD	-		CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-	-		-	-		-	-
PA0-WKUP1	-	TIM2_CH1_ETR	TIM5_CH1	-	-	-	-	USART2_CTS	-		-	-		TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	-		SEG0	-		TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-		SEG1	-		TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-		SEG2	-		TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-		-	-		TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-		-	-		TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-		SEG3	-		TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-		SEG4	-		TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-		COM0	-		TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX	-		COM1	-		TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX	-		COM2	-		TIMx_IC3	EVENT OUT
PA11	-	-	-	-	-	SPI1_MISO		USART1_CTS	-		-	-		TIMx_IC4	EVENT OUT

6.1.6 Power supply scheme

Figure 11. Power supply scheme



Low-speed external user clock generated from an external source

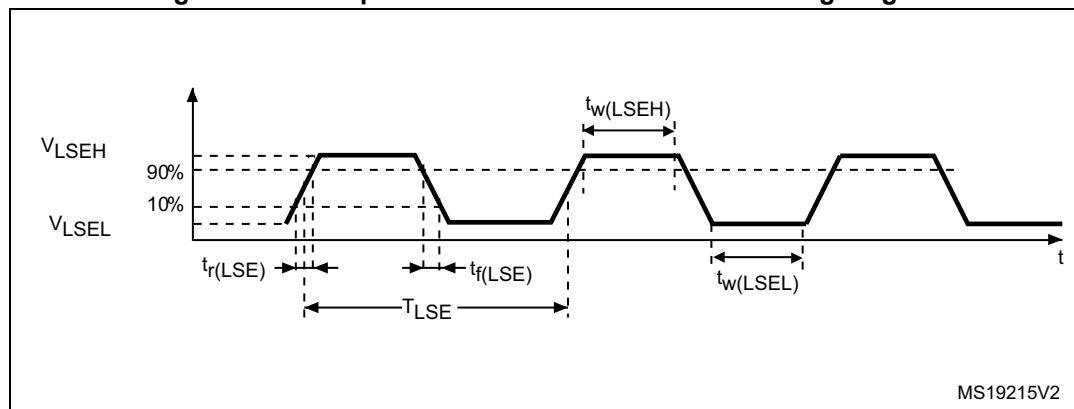
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under the conditions summarized in [Table 13](#).

Table 27. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF

1. Guaranteed by design.

Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 28](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

6.3.8 PLL characteristics

The parameters given in [Table 33](#) are derived from tests performed under the conditions summarized in [Table 13](#).

Table 33. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f _{PLL_IN}	PLL input clock ⁽²⁾	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f _{PLL_OUT}	PLL output clock	2	-	32	MHz
t _{LOCK}	PLL lock time PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	μs
Jitter	Cycle-to-cycle jitter	-	-	±600	ps
I _{DDA} (PLL)	Current consumption on V _{DDA}	-	220	450	μA
I _{DD} (PLL)	Current consumption on V _{DD}	-	120	150	

1. Guaranteed by characterization results.

2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 18](#) and [Table 44](#), respectively.

Unless otherwise specified, the parameters given in [Table 44](#) are derived from tests performed under the conditions summarized in [Table 13](#).

Table 44. I/O AC characteristics⁽¹⁾

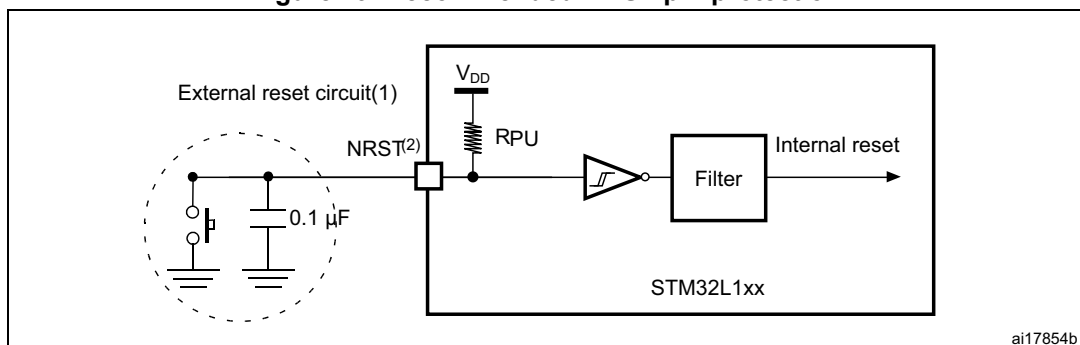
OSPEEDRx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	400	kHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	400	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	625	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	625	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	2	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	1	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	125	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	250	
10	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	10	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	2	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	25	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	125	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	8	
	$t_{f(\text{IO})\text{out}}$ $t_{r(\text{IO})\text{out}}$	Output rise and fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	-	5	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 1.65 \text{ V to } 2.7 \text{ V}$	-	30	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32L151xx, STM32L152xx and STM32L162xx reference manual for a description of GPIO Port configuration register.

2. Guaranteed by design.

3. The maximum frequency is defined in [Figure 18](#).

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 45](#). Otherwise the reset will not be taken into account by the device.

6.3.15 TIM timer characteristics

The parameters given in the [Table 46](#) are guaranteed by design.

Refer to [Section 6.3.13: I/O port characteristics](#) for details on the input/output cition characteristics (output compare, input capture, external clock, PWM output).

Table 46. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 32 \text{ MHz}$	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	0.0312	2048	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 32 \text{ MHz}$	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM3 and TIM4 timers.

6.3.16 Communications interfaces

I²C interface characteristics

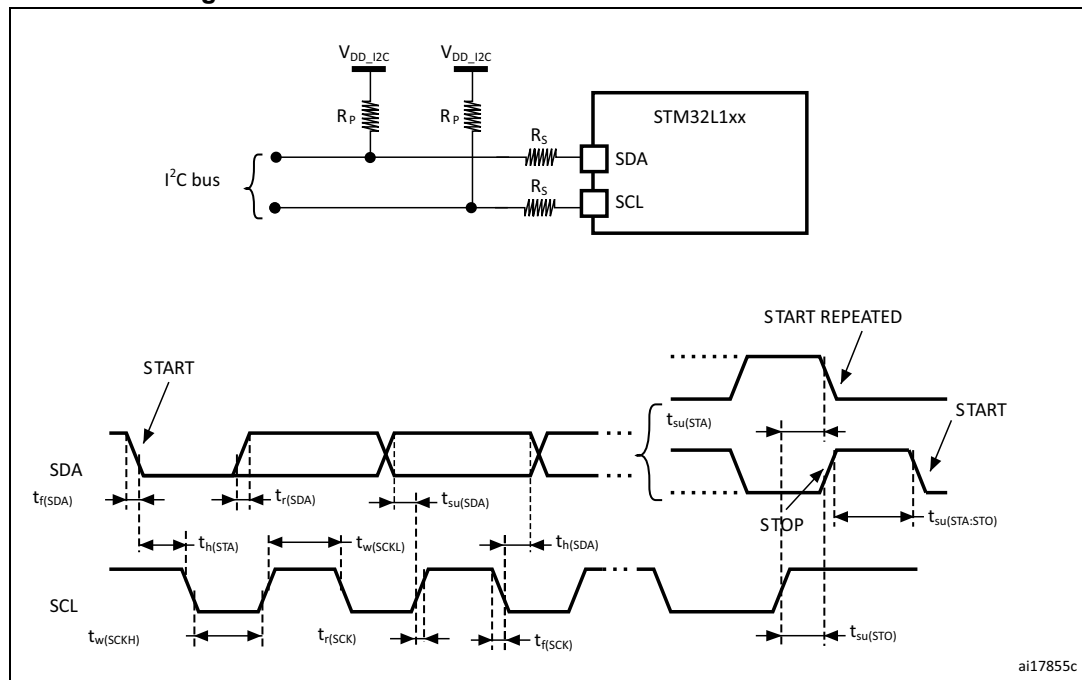
The device I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: SDA and SCL are not “true” open-drain I/O pins. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in [Table 47](#). Refer also to [Section 6.3.13: I/O port characteristics](#) for more details on the input/output cation characteristics (SDA and SCL).

Table 47. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	μs
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	
t _{su} (SDA)	SDA setup time	250	-	100	-	ns
t _h (SDA)	SDA data hold time	-	3450 ⁽³⁾	-	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1000	-	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	300	-	300	
t _h (STA)	Start condition hold time	4.0	-	0.6	-	μs
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su} (STO)	Stop condition setup time	4.0	-	0.6	-	μs
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF
t _{SP}	Pulse width of spikes that are suppressed by the analog filter	0	50 ⁽⁴⁾	0	50 ⁽⁴⁾	ns

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP(max)}.

Figure 20. I²C bus AC waveforms and measurement circuit

1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 48. SCL frequency ($f_{PCLK1} = 32 \text{ MHz}$, $V_{DD} = V_{DD_I2C} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

f_{SCL} (kHz)	I2C_CCR value
	$R_P = 4.7 \text{ k}\Omega$
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of $\pm 5\%$. For other speed ranges, the tolerance on the achieved speed is $\pm 2\%$. These variations depend on the accuracy of the external components used to design the application.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in [Table 13](#).

Refer to [Section 6.3.12: I/O current injection characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max ⁽²⁾	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12 ⁽³⁾	
$t_{r(SCK)}^{(2)}$ $t_{f(SCK)}^{(2)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}^{(2)}$ $t_{w(SCKL)}^{(2)}$	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}^{(2)}$	Data input setup time	Master mode	5	-	
$t_{su(SI)}^{(2)}$		Slave mode	6	-	
$t_{h(MI)}^{(2)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}^{(2)}$		Slave mode	5	-	
$t_{a(SO)}^{(4)}$	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}^{(2)}$	Data output valid time	Slave mode	-	33	
$t_{v(MO)}^{(2)}$	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}^{(2)}$	Data output hold time	Slave mode	17	-	
$t_{h(MO)}^{(2)}$		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.

2. Guaranteed by characterization results.

3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.

4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

6.3.18 DAC electrical specifications

Data guaranteed by design, unless otherwise specified.

Table 58. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V _{REF+}	Reference supply voltage	V _{REF+} must always be below V _{DDA}	1.8	-	3.6	
V _{REF-}	Lower reference voltage	-	V _{SSA}			
I _{DDVREF+} ⁽¹⁾	Current consumption on V _{REF+} supply V _{REF+} = 3.3 V	No load, middle code (0x800)	-	130	220	μA
		No load, worst code (0x000)	-	220	350	
I _{DDA} ⁽¹⁾	Current consumption on V _{DDA} supply V _{DDA} = 3.3 V	No load, middle code (0x800)	-	210	320	
		No load, worst code (0xF1C)	-	320	520	
R _L ⁽²⁾	Resistive load	DAC output buffer ON	5	-	-	kΩ
C _L ⁽²⁾	Capacitive load		-	-	50	pF
R _O	Output impedance	DAC output buffer OFF	12	16	20	kΩ
V _{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	V _{DDA} − 0.2	V
		DAC output buffer OFF	0.5	-	V _{REF+} − 1LSB	mV
DNL ⁽¹⁾	Differential non linearity ⁽³⁾	C _L ≤ 50 pF, R _L ≥ 5 kΩ DAC output buffer ON	-	1.5	3	LSB
		No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	1.5	3	
INL ⁽¹⁾	Integral non linearity ⁽⁴⁾	C _L ≤ 50 pF, R _L ≥ 5 kΩ DAC output buffer ON	-	2	4	
		No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	2	4	
Offset ⁽¹⁾	Offset error at code 0x800 ⁽⁵⁾	C _L ≤ 50 pF, R _L ≥ 5 kΩ DAC output buffer ON	-	±10	±25	
		No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	±5	±8	
Offset1 ⁽¹⁾	Offset error at code 0x001 ⁽⁶⁾	No R _L , C _L ≤ 50 pF DAC output buffer OFF	-	±1.5	±5	

6.3.22 LCD controller

The device embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 64. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	μF
$I_{LCD}^{(1)}$	Supply current at $V_{DD} = 2.2 V$	-	3.3	-	μA
	Supply current at $V_{DD} = 3.0 V$	-	3.1	-	
$R_{Htot}^{(2)}$	Low drive resistive network overall value	5.28	6.6	7.92	$M\Omega$
$R_L^{(2)}$	High drive resistive network total value	192	240	288	$k\Omega$
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	$3/4 V_{LCD}$	-	V
V_{23}	Segment/Common 2/3 level voltage	-	$2/3 V_{LCD}$	-	
V_{12}	Segment/Common 1/2 level voltage	-	$1/2 V_{LCD}$	-	
V_{13}	Segment/Common 1/3 level voltage	-	$1/3 V_{LCD}$	-	
V_{14}	Segment/Common 1/4 level voltage	-	$1/4 V_{LCD}$	-	
V_0	Segment/Common lowest level voltage	0	-	-	
$\Delta V_{xx}^{(3)}$	Segment/Common level voltage error $T_A = -40$ to $105^\circ C$	-	-	± 50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Table 65. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

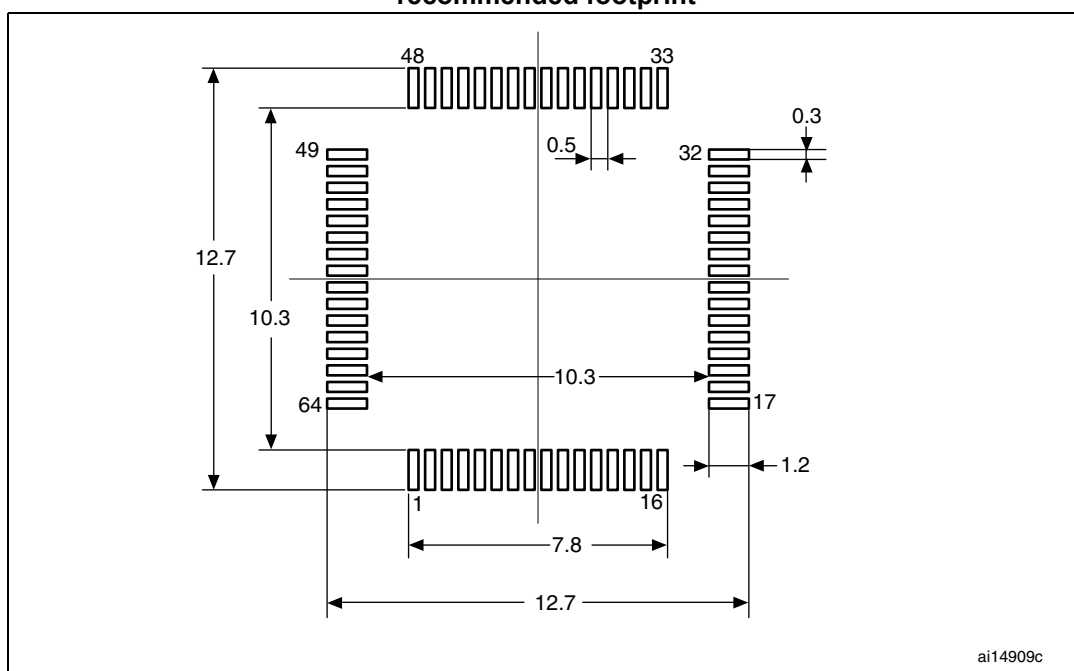
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 67. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

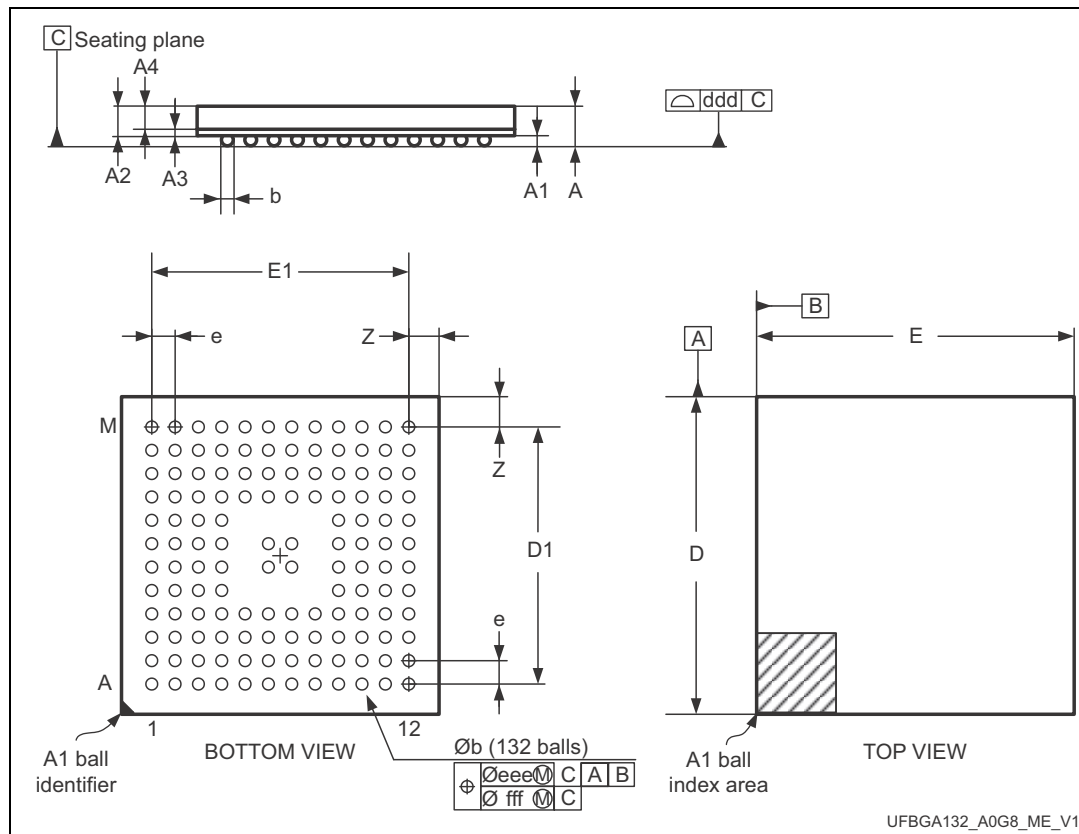
Figure 38. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint



1. Dimensions are in millimeters.

7.4 UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package information

Figure 40. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 68. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

7.6 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 71. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm / 0.5 mm pitch	40	°C/W
	Thermal resistance junction-ambient UFBGA132 - 7 x 7 mm	60	
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient WLCSP64 - 0.400 mm pitch	46	