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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	109
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152qch6

Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}=V_{DDA} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD}=V_{DDA} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

3.13 Ultra-low-power comparators and reference voltage

The STM32L151xC/C-A and STM32L152xC/C-A devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.15 Touch sensing

The STM32L151xC/C-A and STM32L152xC/C-A devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 23 capacitive sensing channels distributed over 10 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.17.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

3.17.4 Inter-integrated sound (I^2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

3.17.5 Universal serial bus (USB)

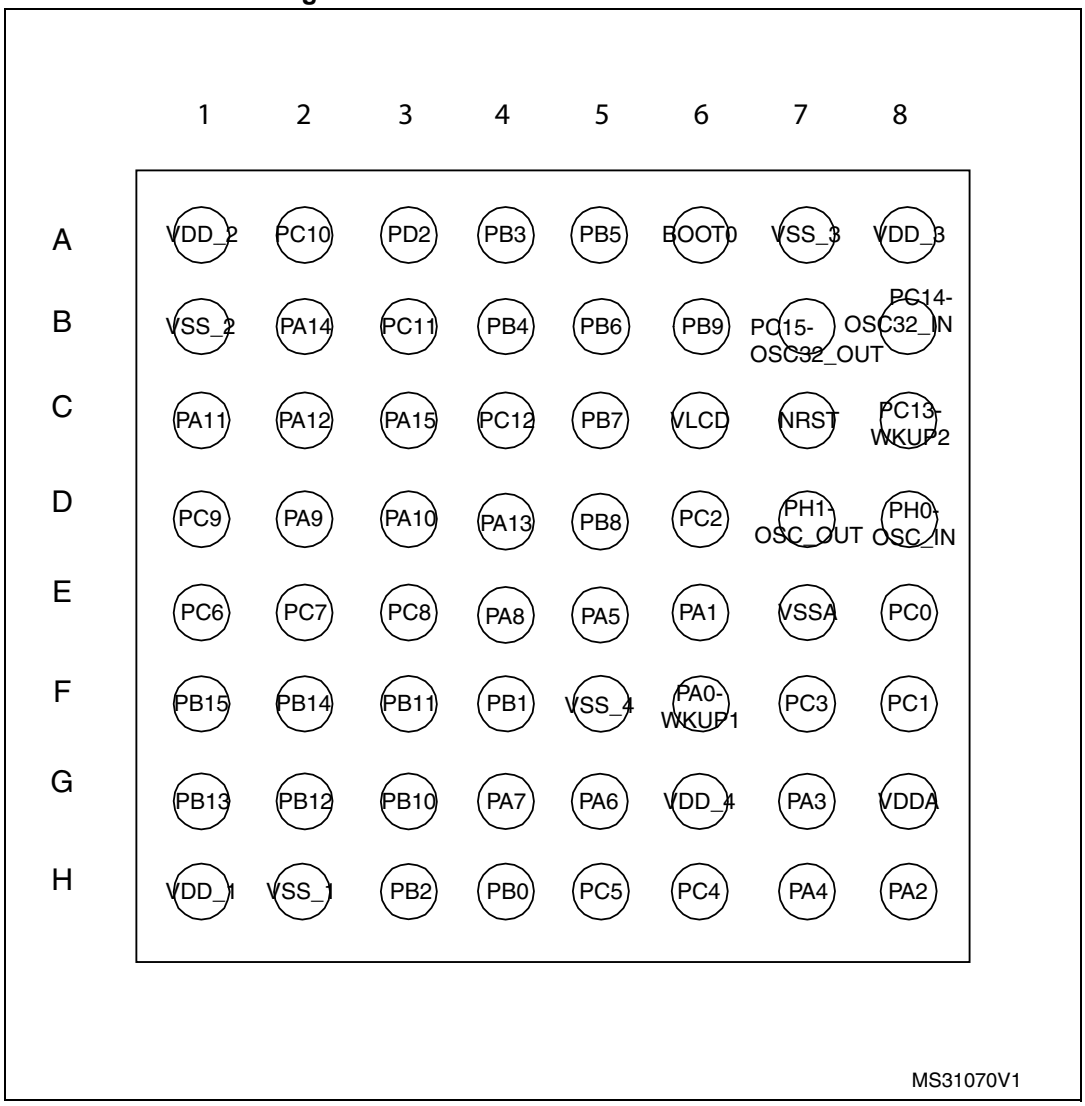
The STM32L151xC/C-A and STM32L152xC/C-A devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.18 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Figure 7. STM32L15xRC WLCSP64 ballout



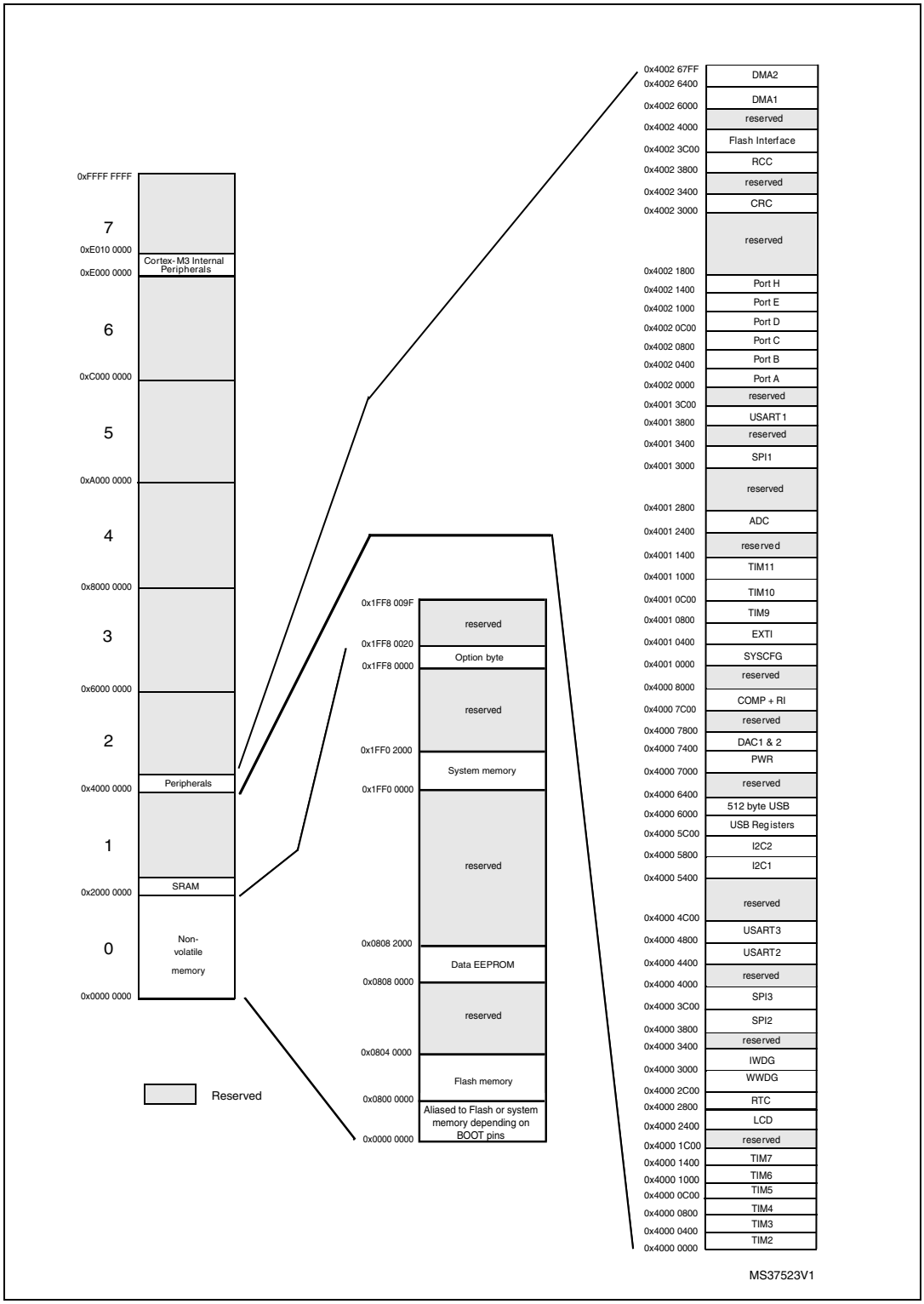
1. This figure shows the package top view.

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	AFIO12	..	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	-		LCD	-		CPRI	SYSTEM
PF6	-	-	TIM5_ETR	-	-	-	-	-	-		-	-		-	EVENT OUT
PF7	-	-	TIM5_CH2	-	-	-	-	-	-		-	-		-	EVENT OUT
PF8	-	-	TIM5_CH3	-	-	-	-	-	-		-	-		-	EVENT OUT
PF9	-	-	TIM5_CH4	-	-	-	-	-	-		-	-		-	EVENT OUT
PF10	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PF11	-	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
PF12	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PF13	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PF14	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PG0	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PG1	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PG2	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PG3	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT
PG4	-	-	-	-	-	-	-	-	-		-			-	EVENT OUT

5 Memory mapping

Figure 8. Memory map



6.1.6 Power supply scheme

Figure 11. Power supply scheme

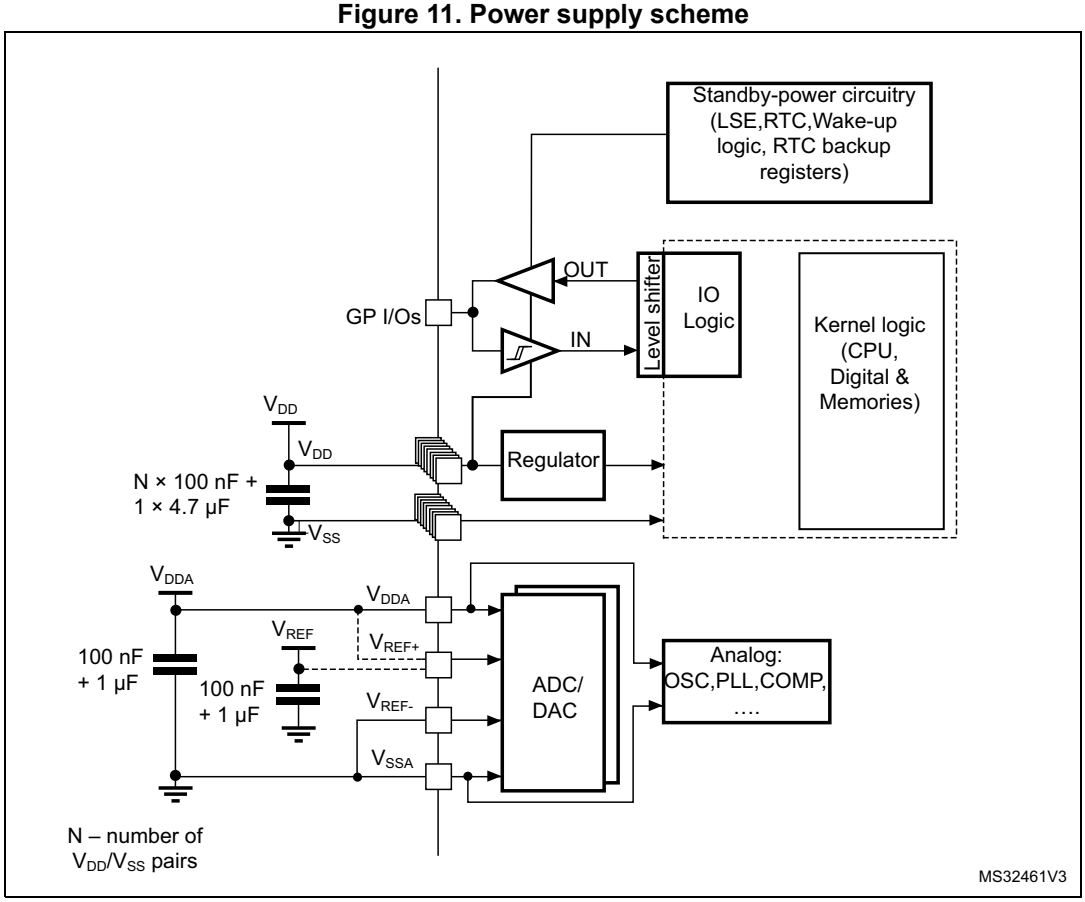


Table 13. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	110	

1. When the ADC is used, refer to *Table 55: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up .
3. To sustain a voltage higher than VDD+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 71: Thermal characteristics on page 129*).
5. In low-power dissipation state, T_A can be extended to -40°C to 105°C temperature range as long as T_J does not exceed T_J max (see *Table 71: Thermal characteristics on page 129*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the conditions summarized in *Table 13*.

Table 14. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16MHz (PLL ON)(1)	Range3, V_{CORE}=1.2 V VOS[1:0]=11	1	230	470	µA
				2	415	780	
				4	800	1200	
			Range2, V_{CORE}=1.5 V VOS[1:0]=10	4	0.935	1.5	mA
				8	1.9	3	
				16	3.75	5	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	8	2.25	3.5	
				16	4.45	5.55	
				32	9.05	10.9	
		HSI clock source (16 MHz)	Range2, V_{CORE}=1.5 V VOS[1:0]=10	16	3.75	4.8	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	32	8.95	11.7	
		MSI clock, 65 kHZ	Range3, V_{CORE}=1.2 V VOS[1:0]=11	0.065	43.5	100	µA
		MSI clock, 524 kHZ		0.524	135	215	
		MSI clock, 4.2 MHZ		4.2	835	1100	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 28. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

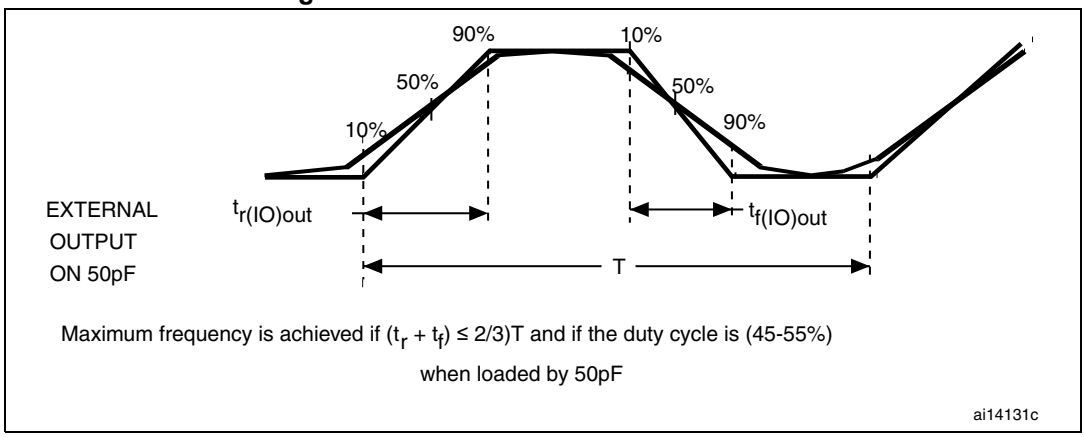
For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Multi-speed internal (MSI) RC oscillator

Table 32. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤105 °C	-	±3	-	%
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Figure 18. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 45*)

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 13*.

Table 45. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7 V_{DD}	-	-	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(3)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 13*.

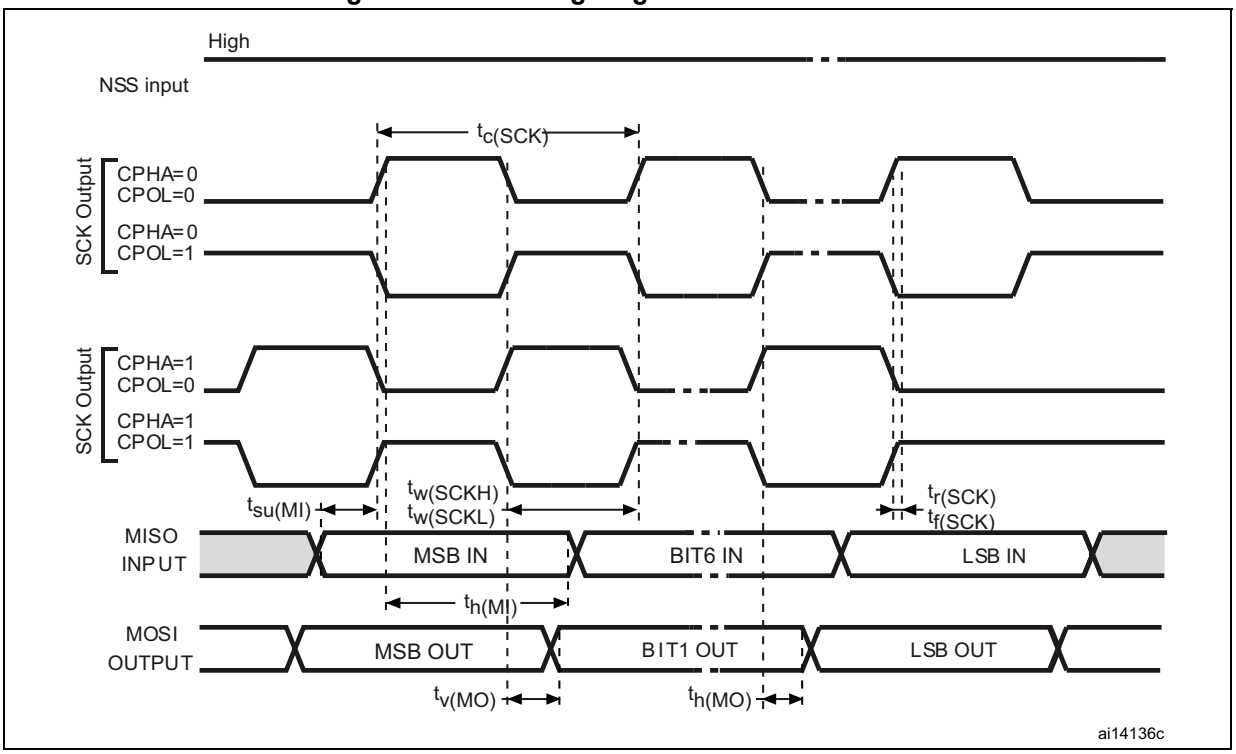
Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Figure 23. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 63. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤V_{DDA} ≤2.7 V	-	1.8	3.5	
		2.7 V ≤V_{DDA} ≤3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤V_{DDA} ≤2.7 V	-	0.8	2	
		2.7 V ≤V_{DDA} ≤3.6 V	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- =V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	100	ppm /°C
I_{COMP2}	Current consumption(3)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.22 LCD controller

The device embeds a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 64. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(3)	Segment/Common level voltage error T_A = -40 to 105 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Table 69. WLCSP64, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
b[2]	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	4.504	4.539	4.574	0.1773	0.1787	0.1801
E	4.876	4.911	4.946	0.1920	0.1933	0.1947
e	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
F	-	0.870	-	-	0.0343	-
G	-	1.056	-	-	0.0416	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 44. WLCSP64, 0.4 mm pitch wafer level chip scale package recommended footprint

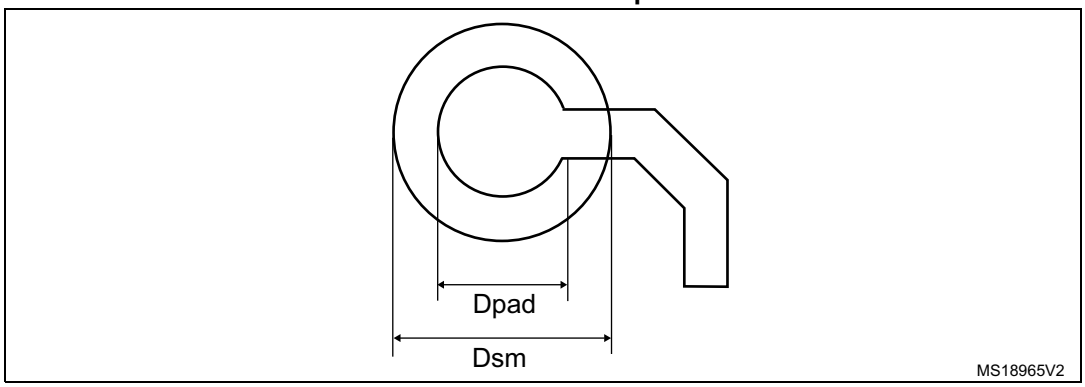


Table 70. WLCSP64, 0.4 mm pitch package recommended PCB design rules

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

9 Revision History

Table 73. Document revision history

Date	Revision	Changes
01-Apr-2014	1	Initial release.
07-Apr-2014	2	Updated *Table 3: Functionalities depending on the operating power supply range*. Updated *Table 17: Current consumption in Run mode, code with data processing running from Flash*. Modified $I_{DD(LP\ Sleep)}$ (TIM9 and USART1 enabled, Flash ON, V_{DD} from 1.65 V to 3.6 V) in *Table 21: Current consumption in Low-power sleep mode*. Updated $V_{IH(NRST)}$ minimum value in *Table 45: NRST pin characteristics*. Added *Table 41: UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint*..
12-June-2014	3	Updated title removing memory I/F. Removed ambiguity of “ambient temperature” in the electrical characteristics description. updated *Figure 1* with graphic improvements.
13-Sept-2014	4	Updated *Section 3.17: Communication interfaces* putting I2S characteristics inside. Updated DMIPS features in cover page and *Section 2: Description*. Updated max temperature at 105°C instead of 85°C in the whole datasheet. Updated Flash switched ON & OFF conditions in *Table 19: Current consumption in Sleep mode*. Updated *Table 24: Peripheral current consumption* with new measured current values. Updated *Table 57: Maximum source impedance RAIN max* adding note 2.