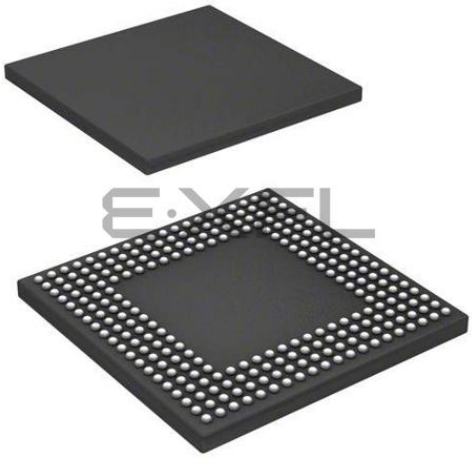

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Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
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Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	256-LFBGA (17x17)
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Name	I/O	Function
WE3(BE3)/DQMUU/ ICIOWR	O	Indicates that D31 to D24 are being written to. Connected to the byte select signal when a byte-selection SRAM is connected. Corresponds to signals D31 to D24 when SDRAM is connected. Functions as the I/O write strobe signal when the PCMCIA is used.
WE2(BE2)/DQMUL/ ICIORD	O	Indicates that D23 to D16 are being written to. Connected to the byte select signal when a byte-selection SRAM is connected. Corresponds to signals D23 to D16 when the SDRAM is used. Functions as the I/O read strobe signal when the PCMCIA is used.
WE1(BE1)/DQMLU/ WE	O	Indicates that D15 to D8 are being written to. Connected to the byte select signal when a byte-selection SRAM is connected. Corresponds to signals D15 to D8 when the SDRAM is used. Functions as the memory write strobe signal when the PCMCIA is used.
WE0(BE0)/DQMLL	O	Indicates that D7 to D0 are being written to. Connected to the byte select signal when a byte-selection SRAM is connected. Corresponds to select signals D7 to D0 when the SDRAM is used.
RAS	O	Connects to RAS pin when SDRAM is connected.
CAS	O	Connects to CAS pin when SDRAM is connected.
CKE	O	Connects to CKE pin when SDRAM is connected.
IOIS16	I	PCMCIA 16-bit I/O signal Valid only in little endian mode. Pulled low in bit endian mode.
WAIT	I	External wait input (sampled at the falling edge of CKIO)
BREQ	I	Bus request input
BACK	O	Bus acknowledge output
MD5 to MD3	I	MD5: Selects data alignment (big endian or little endian) MD4 and MD3: Specify area 0 bus width (8/16/32 bits)
REFOUT	O	Bus mastership request signal for refreshing

9.4.3 CSn Space Wait Control Register (CSnWCR)

This register specifies various wait cycles for memory accesses. The bit configuration of this register varies as shown below according to the memory type (TYPE3, TYPE2, TYPE1, or TYPE0) specified by the CSn space bus control register (CSnBCR). Specify CSnWCR before accessing the target area. Specify CSnBCR first, then specify CSnWCR.

(n = 0, 2, 3, 4, 5A, 5B, 6A, 6B)

(1) Normal Space, Byte-Selection SRAM

- CS0WCR, CS6BWCR

Bit	Bit Name	Initial Value	R/W	Description
31 to 21		All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BAS	0	R/W	Byte Access Selection for Byte-Selection SRAM Specifies the WEn (BEn) and RD/WR signal timing when the byte-selection SRAM interface is used. 0: Asserts the WEn (BEn) signal at the read/write timing and asserts the RD/WR signal during the write access cycle. 1: Asserts the WEn (BEn) signal during the read/write access cycle and asserts the RD/WR signal at the write timing.
19 to 13		All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 11	SW1 SW0	0 0	R/W R/W	Number of Delay Cycles from Address, CSn Assertion to RD, WEn (BEn) Assertion Specify the number of delay cycles from address and CSn assertion to RD and WEn (BEn) assertion. 00: 0.5 cycle 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles

- DMARS2

Bit	Bit Name	Initial Value	R/W	Description
15	C5MID5	0	R/W	Transfer request module ID5 to ID0 for DMA channel 5 (MID) See table 10.2.
14	C5MID4	0	R/W	
13	C5MID3	0	R/W	
12	C5MID2	0	R/W	
11	C5MID1	0	R/W	
10	C5MID0	0	R/W	
9	C5RID1	0	R/W	Transfer request register ID1 and ID0 for DMA channel 5 (RID) See table 10.2.
8	C5RID0	0	R/W	
7	C4MID5	0	R/W	Transfer request module ID5 to ID0 for DMA channel 4 (MID) See table 10.2.
6	C4MID4	0	R/W	
5	C4MID3	0	R/W	
4	C4MID2	0	R/W	
3	C4MID1	0	R/W	
2	C4MID0	0	R/W	
1	C4RID1	0	R/W	Transfer request register ID1 and ID0 for DMA channel 4 (RID) See table 10.2.
0	C4RID0	0	R/W	

This intermittent mode can be used for all transfer section; transfer request source, transfer source, and transfer destination. The bus modes, however, must be cycle steal mode in all channels.

Figure 10.10 shows an example of DMA transfer timing in cycle steal intermittent mode. Transfer conditions shown in the figure are:

Dual address mode

DREQ low level detection

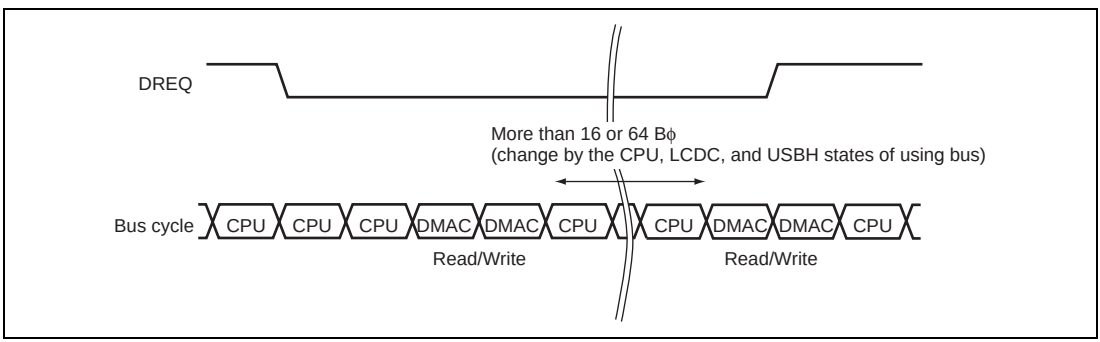


Figure 10.10 Example of DMA Transfer in Cycle Steal Intermittent Mode (Dual Address, DREQ Low Level Detection)

(b) Burst Mode

In burst mode, once the DMAC obtains the bus mastership, the transfer is performed continuously without releasing the bus mastership until the transfer end condition is satisfied. In external request mode with level detection of the DREQ pin, however, when the DREQ pin is not active, the bus mastership passes to the other bus master after the DMAC transfer request that has already been accepted ends, even if the transfer end conditions have not been satisfied.

Burst mode cannot be used for other than CMT (channels 0 to 4) when the on-chip peripheral module is the transfer request source.

Figure 10.11 shows DMA transfer timing in burst mode.

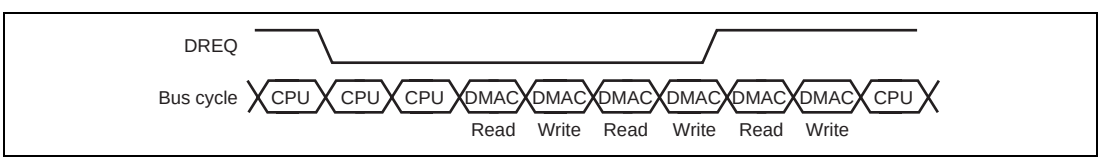


Figure 10.11 DMA Transfer Example in Burst Mode (Dual Address, DREQ Low Level Detection)

12.2 Register Descriptions for WDT

The WDT has the following two registers. Refer to section 37, List of Registers, for more details on the addresses and states of these registers in each operating mode.

- Watchdog timer counter (WTCNT)
- Watchdog timer control/status register (WTCSR)

12.2.1 Watchdog Timer Counter (WTCNT)

WTCNT is an 8-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval time mode. The WTCNT counter is not initialized by an internal reset due to the WDT overflow. The WTCNT counter is initialized to H'00 only by a power-on reset. Use a word access to write to the WTCNT counter, with H'5A in the upper byte. Use a byte access to read WTCNT.

Note: WTCNT differs from other registers in that it is more difficult to write to. See section 12.2.3, Notes on Register Access, for details.

12.2.2 Watchdog Timer Control/Status Register (WTCSR)

WTCSR is an 8-bit readable/writable register composed of bits to select the clock used for the count, bits to select the timer mode, and overflow flags. WTCSR holds its value in an internal reset due to the WDT overflow. WTCSR is initialized to H'00 only by a power-on reset.

When used to count the clock settling time for canceling a software standby, it retains its value after counter overflow. Use a word access to write to WTCSR, with H'A5 in the upper byte. Use a byte access to read WTCSR.

Note: WTCSR differs from other registers in that it is more difficult to write to. See section 12.2.3, Notes on Register Access, for details.

Bit	Bit Name	Initial Value	R/W	Description
1	TGFB	0	R/(W)*	Compare Flag B Status flag that indicates the occurrence of TGRB compare match. [Clearing conditions] When 0 is written to TGFB after reading TGFB = 1 [Setting conditions] When TCNT = TGRB
0	TGFA	0	R/(W)*	Output Compare Flag A Status flag that indicates the occurrence of TGRA compare match. [Clearing conditions] When 0 is written to TGFA after reading TGFA = 1 [Setting conditions] When TCNT = TGRA

Note: * Only 0 can be written, to clear the flag.

15.3.6 Timer Counters (TCNT)

The TCNT registers are 16-bit readable/writable counters. The TPU has four TCNT counters, one for each channel.

The TCNT counters are initialized to H'0000 by a reset.

The TCNT counters are not initialized in standby mode, sleep mode, or module standby.

15.3.7 Timer General Registers (TGR)

The TGR registers are 16-bit registers. The TPU has 16 TGR registers, four each for channels 0 and 3. TGRC and TGRD can also be designated for operation as buffer registers*. The TGR registers are initialized to H'FFFF by a reset. These registers are not initialized in standby mode, sleep mode, or module standby.

Note: * TGR buffer register combinations are TGRA—TGRC and TGRB—TGRD.

20.3.4 I²C Bus Interrupt Enable Register (ICIER)

ICIER enables or disables interrupt sources and acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When the TDRE bit in ICSR is set to 1, this bit enables or disables the transmit data empty interrupt (TXI). 0: Transmit data empty interrupt request (TXI) is disabled. 1: Transmit data empty interrupt request (TXI) is enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disabled. 1: Transmit end interrupt request (TEI) is enabled.
5	RIE	0	R/W	Receive Interrupt Enable This bit enables or disables the receive data full interrupt request (RXI) when a receive data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Receive data full interrupt request (RXI) is disabled. 1: Receive data full interrupt request (RXI) is enabled.
4	NAKIE	0	R/W	NACK Receive Interrupt Enable This bit enables or disables the NACK receive interrupt request (NAKI) when the NACKF and AL bits in ICSR are set to 1. NAKI can be canceled by clearing the NACKF, OVE, or NAKIE bit to 0. 0: NACK receive interrupt request (NAKI) is disabled. 1: NACK receive interrupt request (NAKI) is enabled.

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Transfer Rate					
CKS4	CKS3	CKS2	CKS1	CKS0	Peripheral Clock	Pϕ = 10 MHz	Pϕ = 16 MHz	Pϕ = 20 MHz	Pϕ = 25 MHz	Pϕ = 30 MHz	Pϕ = 32 MHz
1	1	1	0	1	Pϕ/800	13kHz	20kHz	25kHz	31kHz	38kHz	40kHz
1	1	1	1	0	Pϕ/896	11kHz	18kHz	22kHz	28kHz	33kHz	36kHz
1	1	1	1	1	Pϕ/1024	10kHz	16kHz	20kHz	24kHz	29kHz	31kHz

Note: In master mode, a transfer rate of 300 kHz or lower should be used.
In slave mode, a transfer rate of 400 kHz or lower should be used.

20.4 Operation

20.4.1 I²C Bus Format

Figure 20.3 shows the I²C bus formats. Figure 20.4 shows the I²C bus timing. The first frame following a start condition always consists of 8 bits.

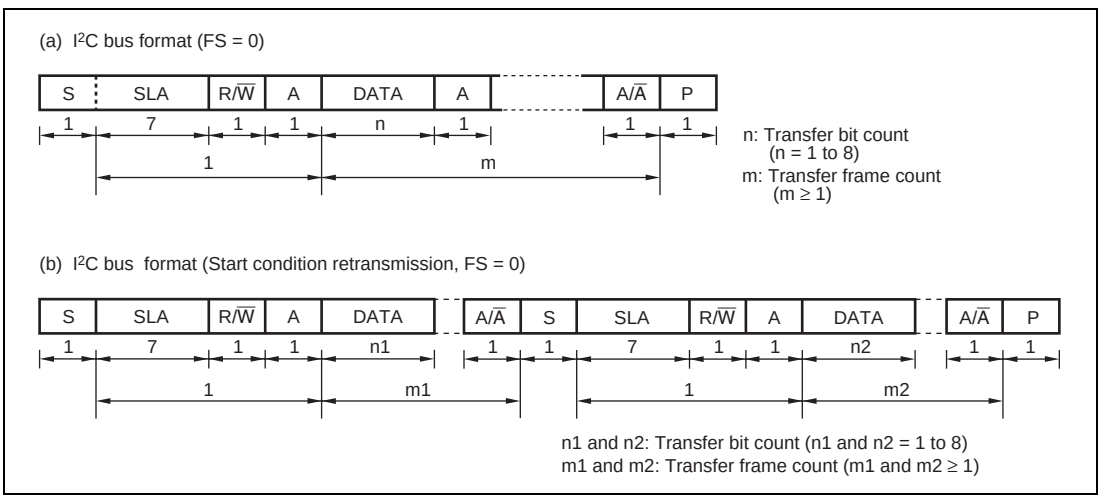


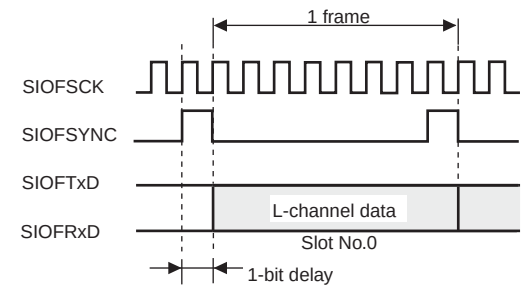
Figure 20.3 I²C Bus Formats

21.4.9 Transmit and Receive Timing

Examples of the SIOF serial transmission and reception are shown in figures 21.13 to 21.19.

(1) 8-bit Monaural Data (1)

Synchronous pulse method, falling edge sampling, slot No.0 used for transmit and receive data, an frame length = 8 bits



Specifications: TRMD[1:0]=00 or 10, TDLE=1, RDLE=1, CD0E=0, REDG=0, TDLA[3:0]=0000, RDLA[3:0]=0000, CD0A[3:0]=0000, FL[3:0]=0000 (frame length: 8 bits) TDRE=0, RDRE=0, CD1E=0, TDRA[3:0]=0000, RDRA[3:0]=0000, CD1A[3:0]=0000

Figure 21.13 Transmit and Receive Timing (8-Bit Monaural Data (1))

Bit	Bit Name	Initial Value	R/W	Description
5	MIFTYP5	0	R/W	Module Interface Type Select
4	MIFTYP4	0	R/W	Set the LCD panel type and data bus width to be output to the LCD panel. There are three LCD panel types: STN, DSTN, and TFT. There are four data bus widths for output to the LCD panel: 4, 8, 12, and 16 bits. When the required data bus width for a TFT panel is 16 bits or more, connect the LCDC and LCD panel according to the data bus size of the LCD panel. Unlike in a TFT panel, in an STN or DSTN panel, the data bus width setting does not have a 1:1 correspondence with the number of display colors and display resolution, e.g., an 8-bit data bus can be used for 16 bpp, and a 12-bit data bus can be used for 4 bpp. This is because the number of display colors in an STN or DSTN panel is determined by how data is placed on the bus, and not by the number of bits. For data specifications for an STN or DSTN panel, see the specifications of the LCD panel used. The output data bus width should be set according to the mechanical interface specifications of the LCD panel. If an STN or DSTN panel is selected, display control is performed using a 24-bit space-modulation FRC (Frame Rate Controller) consisting of the 8-bit R, G, and B included in the LCDC, regardless of the color and gradation settings. Accordingly, the color and gradation specified by DSPCOLOR is selected from 16 million colors in an STN or DSTN panel. If a palette is used, the color specified in the palette is displayed. 000000: STN monochrome 4-bit data bus module 000001: STN monochrome 8-bit data bus module 001000: STN color 4-bit data bus module 001001: STN color 8-bit data bus module 001010: STN color 12-bit data bus module 001011: STN color 16-bit data bus module 010001: DSTN monochrome 8-bit data bus module 010011: DSTN monochrome 16-bit data bus module 011001: DSTN color 8-bit data bus module 011010: DSTN color 12-bit data bus module 011011: DSTN color 16-bit data bus module 101011: TFT color 16-bit data bus module Settings other than above: Setting prohibited
3	MIFTYP3	1	R/W	
2	MIFTYP2	0	R/W	
1	MIFTYP1	0	R/W	
0	MIFTYP0	1	R/W	

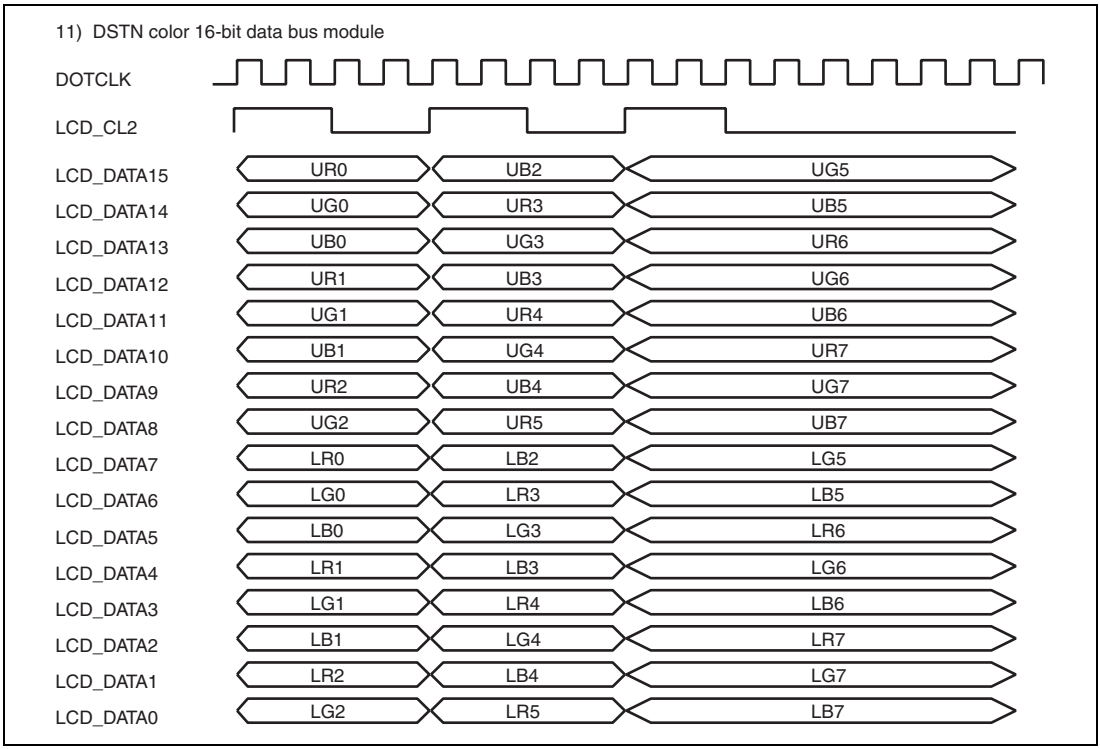


Figure 26.20 Clock and LCD Data Signal Example (DSTN Color 16-Bit Data Bus Module)

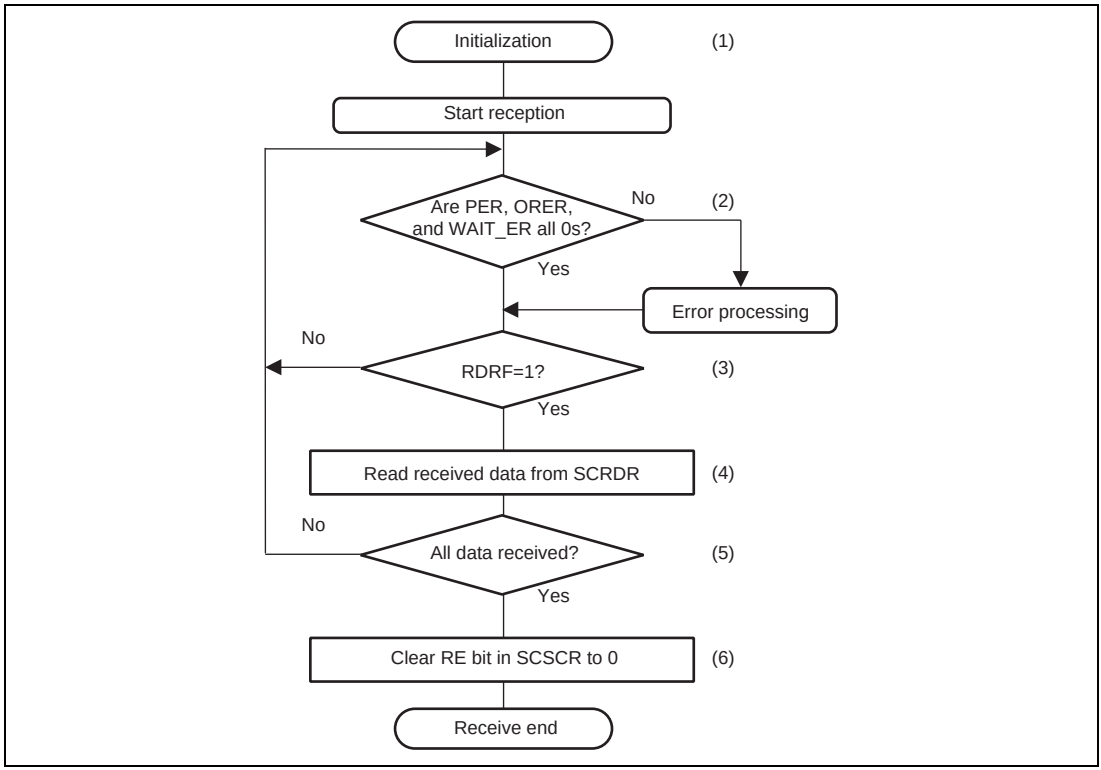


Figure 30.6 Example of Receive Processing

(4) Switching Modes

When switching from receive mode to transmit mode, after confirming that reception has been completed, start initialization, and then clear the RE bit to 0 and set the TE bit to 1. Completion of reception can be confirmed through the RDRF flag.

When switching from transmit mode to receive mode, after confirming that transmission has been completed, start initialization, and then clear the TE bit to 0 and set the RE bit to 1. Completion of transmission can be confirmed through the TDRE and TEND flags.

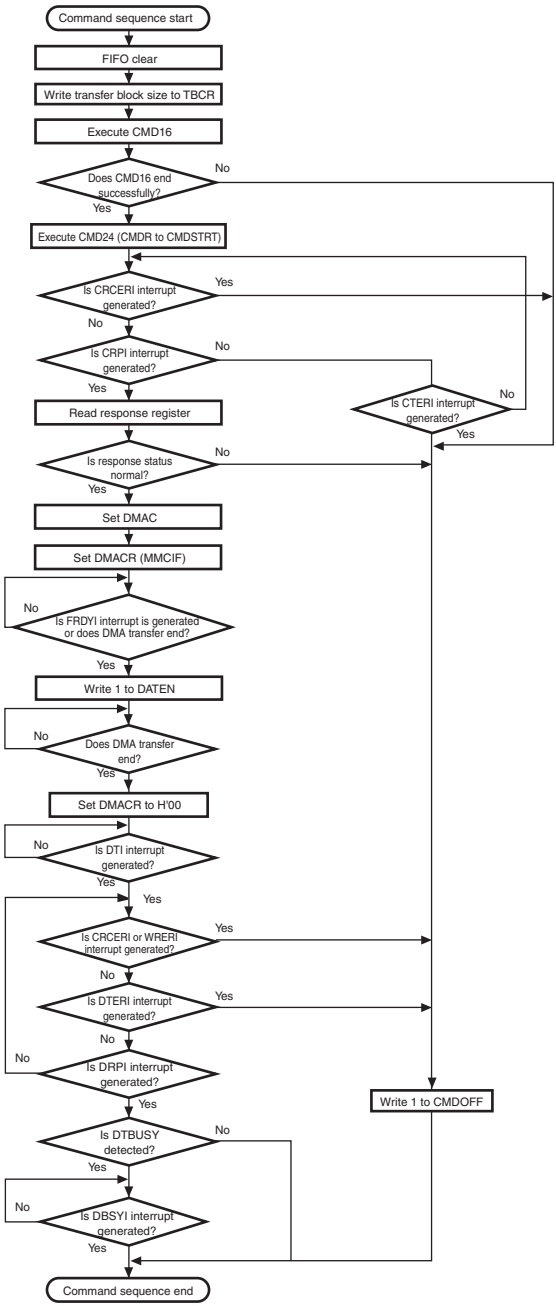


Figure 31.28 Operational Flowchart for Write Sequence (Single Block Transfer)

Section 34 Pin Function Controller (PFC)

The pin function controller (PFC) consists of registers to select the functions and I/O directions of multiplex pins. Pin functions and I/O directions can be individually selected for every pin regardless of the LSI operating mode. Table 34.1 lists the multiplex pins of this LSI.

Note: The signals related to the SDHI should be selected only on the models that include it.

Table 34.1 Multiplexed Pins

Port	Port Function (Related Module)	Other Function (Related Module)
A	PTA7 input/output (port)	D23 input/output (BSC)
	PTA6 input/output (port)	D22 input/output (BSC)
	PTA5 input/output (port)	D21 input/output (BSC)
	PTA4 input/output (port)	D20 input/output (BSC)
	PTA3 input/output (port)	D19 input/output (BSC)
	PTA2 input/output (port)	D18 input/output (BSC)
	PTA1 input/output (port)	D17 input/output (BSC)
	PTA0 input/output (port)	D16 input/output (BSC)
B	PTB7 input/output (port)	D31 input/output (BSC)
	PTB6 input/output (port)	D30 input/output (BSC)
	PTB5 input/output (port)	D29 input/output (BSC)
	PTB4 input/output (port)	D28 input/output (BSC)
	PTB3 input/output (port)	D27 input/output (BSC)
	PTB2 input/output (port)	D26 input/output (BSC)
	PTB1 input/output (port)	D25 input/output (BSC)
	PTB0 input/output (port)	D24 input/output (BSC)
C	PTC7 input/output (port)	LCD_DATA7 output (LCDC)
	PTC6 input/output (port)	LCD_DATA6 output (LCDC)
	PTC5 input/output (port)	LCD_DATA5 output (LCDC)
	PTC4 input/output (port)	LCD_DATA4 output (LCDC)
	PTC3 input/output (port)	LCD_DATA3 output (LCDC)
	PTC2 input/output (port)	LCD_DATA2 output (LCDC)
	PTC1 input/output (port)	LCD_DATA1 output (LCDC)
	PTC0 input/output (port)	LCD_DATA0 output (LCDC)

Bit	Bit Name	Initial Value	R/W	Description
11 10	PSELC11 PSELC10	0 0	R/W R/W	SIM_RST/SCIF1_RxD/SD_WP Select as PTV1 Other Functions 00: Select SCIF1_RxD 01: Reserved 10: Select SIM_RST 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_WP when PSELB0 = 1
9 8	PSELC9 PSELC8	0 0	R/W R/W	SIM_D/SCIF1_TxD/SD_CD Select as PTV2 Other Functions 00: Select SCIF1_TxD 01: Reserved 10: Select SIM_D 11: Select according to PSELB0 setting Reserved when PSELB0 = 0 Select SD_CD when PSELB0 = 1
7 to 0		All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

PFCR State

PFnMD1	PFnMD0	Pin State	Read	Write
0	0	Other function	PFDR value	Value is written to PFDR, but does not affect pin state.
	1	Reserved		
1	0	Input (Pull-up MOS on)	Pin state	Value is written to PFDR, but does not affect pin state.
	1	Input (Pull-up MOS off)	Pin state	Value is written to PFDR, but does not affect pin state.

Note: n = 0

(3) EXTEST

This instruction is provided to test external circuitry when this LSI is mounted on a printed circuit board. When this instruction is executed, output pins are used to output test data (previously set by the SAMPLE/PRELOAD instruction) from the boundary scan register to the printed circuit board, and input pins are used to latch test results into the boundary scan register from the printed circuit board. If testing is carried out by using the EXTEST instruction N times, the Nth test data is scanned-in when test data (N-1) is scanned out.

Data loaded into the output pin boundary scan register in the Capture-DR state is not used for external circuit testing (it is replaced by a shift operation).

The upper four bits of the instruction code are B'0000.

(4) IDCODE

A command can be set in SDIR by the H-UDI pins to place the H-UDI pins in the IDCODE mode stipulated by JTAG. When the H-UDI is initialized ($\overline{\text{TRST}}$ is asserted or TAP is in the Test-Logic-Reset state), the IDCODE mode is entered.

(5) CLAMP, HIGHZ

A command can be set in SDIR by the H-UDI pins to place the H-UDI pins in the CLAMP or HIGHZ mode stipulated by JTAG.

36.5.2 Points for Attention

1. Boundary scan mode does not cover the following signals:

   Clock-related signals (EXTAL, XTAL, EXTAL_USB, XTAL_USB, EXTAL_RTC, XTAL_RTC, CKIO)

   System- and E10A-related signals ($\overline{\text{RESETP}}$, $\overline{\text{RESETM}}$, CA, $\overline{\text{ASEMD0}}$)

   H-UDI-related signals (TCK, TDI, TDO, TMS, $\overline{\text{TRST}}$)

   IIC-related signals (IIC_SCL/PTE6, IIC_SDA/PTE5)

   Analog-related signals (AN0/PTF1, AN1/PTF2, AN2/PTF3, AN3/PTF4, DA0/PTF5, DA1/PTF6, USB1_P, USB1_M, USB2_P, USB2_M)
2. When the EXTEST, CLAMP, and HIGHZ commands are set, fix the $\overline{\text{RESETP}}$ pin low.
3. Fix the CA pin high, during boundary scan.
4. When a boundary scan test for other than BYPASS and IDCODE is carried out, fix the $\overline{\text{ASEMD0}}$ pin high.