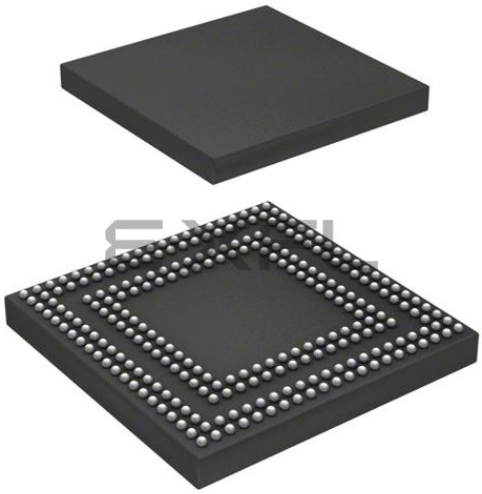
Renesas Electronics America Inc - R8A77210C133BAV Datasheet



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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	SH-3 DSP
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-20°C ~ 75°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	256-LFBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77210c133bav

Bit	Bit Name	Initial Value	R/W	Description
28	BL	1	R/W	Block Specifies whether an exception, interrupt, or user break is enabled or not. 0: Enables an exception, interrupt, or user break. 1: Disables an exception, interrupt, or user break. The BL bit is set to 1 in reset or exception handling state.
27 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	M	—	R/W	M Bit
8	Q	—	R/W	Q Bit These bits are used by the DIV0S, DIV0U, and DIV1 instructions. These bits can be changed even in user mode by using the DIV0S, DIV0U, and DIV1 instructions. These bits are undefined at reset. These bits do not change in an exception handling state.
7 to 4	I3 to I0	All 1	R/W	Interrupt Mask Indicates the interrupt mask level. These bits do not change even if an interrupt occurs. At reset, these bits are initialized to B'1111. These bits are not affected in an exception handling state.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	S	—	R/W	Saturation Mode Specifies the saturation mode for multiply instructions or multiply and accumulate instructions. This bit can be specified by the SETS and CLRS instructions in user mode. At reset, this bit is undefined. This bit is not affected in an exception handling state.

Table 2.8 Logic Operation Instructions

Instruction		Instruction Code	Operation	Privileged Mode	Cycles	T Bit
AND	Rm,Rn	0010nnnnmmmm1001	Rn & Rm → Rn	–	1	–
AND	#imm,R0	11001001iiiiiiii	R0 & imm → R0	–	1	–
AND.B	#imm,@(R0, GBR)	11001101iiiiiiii	(R0+GBR) & imm → (R0+GBR)	–	3	–
NOT	Rm,Rn	0110nnnnmmmm0111	~Rm → Rn	–	1	–
OR	Rm,Rn	0010nnnnmmmm1011	Rn | Rm → Rn	–	1	–
OR	#imm,R0	11001011iiiiiiii	R0 | imm → R0	–	1	–
OR.B	#imm,@(R0, GBR)	11001111iiiiiiii	(R0+GBR) | imm → (R0+GBR)	–	3	–
TAS.B	@Rn	0100nnnn00011011	If (Rn) is 0, 1 → T; 1 → MSB of (Rn)	–	4	Test result
TST	Rm,Rn	0010nnnnmmmm1000	Rn & Rm; if the result is 0, 1 → T	–	1	Test result
TST	#imm,R0	11001000iiiiiiii	R0 & imm; if the result is 0, 1 → T	–	1	Test result
TST.B	#imm,@(R0, GBR)	11001100iiiiiiii	(R0 + GBR) & imm; if the result is 0, 1 → T	–	3	Test result
XOR	Rm,Rn	0010nnnnmmmm1010	Rn ^ Rm → Rn	–	1	–
XOR	#imm,R0	11001010iiiiiiii	R0 ^ imm → R0	–	1	–
XOR.B	#imm,@(R0, GBR)	11001110iiiiiiii	(R0+GBR) ^ imm → (R0+GBR)	–	3	–

Notes: 1. If a TRAPA instruction is used as a repeat detection instruction, an instruction following the repeat detection instruction is regarded as a return address. In this case, a control cannot be returned to the repeat control correctly. In a TRAPA instruction, an address of an instruction following the repeat detection address is regarded as return address. Accordingly, to return to the repeat control correctly, place a return address prior to the repeat detection instruction.

2. If a SLEEP instruction is placed following a repeat detection instruction, a transition to the low-power consumption state or an exception acceptance such as interrupts can be performed correctly. In this case, however, the repeat control cannot be returned correctly. To return to the repeat control correctly, the SLEEP instruction must be placed prior to the repeat detection instruction.

(e) Branch from a repeat detection instruction

If a repeat detection instruction is a delayed slot instruction of a delayed branch instruction or a branch instruction, a repeat loop can be acknowledged when a branch does not occur in a branch instruction. If a branch occurs in a branch instruction, a repeat control is not performed and a branch destination instruction is executed.

(f) Program counter during repeat control

If RC[11:0] ≥ 2, the program counter (PC) value is not correct for instructions two instructions following a repeat detection instruction. In a repeat loop consisting of one to three instructions, the PC indicates the correct value (instruction address + 4) for an instruction (repeat start instruction) following a repeat detect ion instruction but the PC continues to indicate the same address (repeat start instruction address) from the subsequent instruction to a repeat end instruction. In a repeat loop consisting of four or more instructions, the PC indicates the correct value (instruction address + 4) for an instruction following a repeat detect ion instruction, but PC indicates the RS and (RS +2) for instructions two and three instructions following the repeat detection instruction. Here, RS indicates the value stored in the repeat start register (RS). The correct operation cannot be guaranteed for the incorrect PC values.

Accordingly, PC relative addressing instructions placed two or more instructions following the repeat detection instruction cannot be executed correctly and the correct results cannot be obtained.

(4) Initial page write exception

- Conditions

  A hit occurred to the TLB for a store access, but D = 0.
- Types

  Instruction synchronous, re-execution type
- Save address

  Instruction fetch: An instruction address to be fetched when an exception occurred

  Data access: An instruction address where an exception occurs (a delayed branch instruction address if an instruction is assigned to a delay slot)
- Exception code

  H'080
- Remarks

  The virtual address (32 bits) that caused the exception is set in TEA, and the MMU register is updated.

Table 7.5 Instruction Where a Specific Exception Occurs When a Memory Access Exception Occurs in Repeat Control (SR.RC[11:0]≥1)

Instruction Where an Exception Occurs	Number of Instructions in a Repeat Loop			
	1	2	3	4 or Greater
RptDtct	—	—	—	—
RptDtct1	Instruction/data access	Instruction/data access	Instruction/data access	Instruction/data access
RptDtct2	—	Instruction/data access	Instruction/data access	Instruction/data access
RptDtct3	—	—	Instruction/data access	Instruction/data access

Note: The following labels are used here.
RptDtct: Repeat detection instruction address
RptDtct1: Instruction address immediately after the repeat detect instruction
RptDtct2: Second instruction address from the repeat detect instruction
RptDtct3: Third instruction address from the repeat detect instruction

(5) MMU Exception in Repeat Control Period

If an MMU exception occurs in the repeat control period, a specific exception code is generated as well as a CPU address error. For a TLB miss exception, TLB invalid exception, and initial page write exception, an exception code (H'070) indicating the repeat loop period is specified in the EXPEVT. For a TLB protection exception, an exception code (H'0D0) is specified in the EXPEVT. In a TLB miss exception, vector offset is specified as H'00000100.

An instruction where an exception occurs and the SPC value to be saved are the same as those for the CPU address error.

After this exception processing, the repeat control cannot be returned correctly. To execute a repeat loop correctly, care must be taken not to generate an MMU related exception in the repeat control period.

Note: In a repeat loop consisting of one to three instructions, some restrictions apply to repeat detection instructions and all the remaining instructions. In a repeat loop consisting of four or more instructions, restrictions apply to only the three instructions that include a repeat end instruction. The restriction occurs when SR.RC[11:0] ≥ 1.

9.3.4 Area 0 Memory Type and Memory Bus Width

The memory bus width in this LSI can be set for each area. In area 0, external pins can be used to select byte (8 bits), word (16 bits), or longword (32 bits) on power-on reset. The memory bus width of the other area is set by the register. The correspondence between the memory type, external pins (MD3, MD4), and bus width is listed in the table below.

Table 9.4 Correspondence between External Pins (MD3 and MD4), Memory Type of CS0, and Memory Bus Width

MD4	MD3	Memory Type	Bus Width
0	0	Normal memory	Reserved (Setting prohibited)
	1		8 bits*
1	0		16 bits
	1		32 bits

Note: * The bus width must not be specified as eight bits if the burst ROM (clock synchronous) interface is selected.

9.3.5 Data Alignment

This LSI supports the big endian and little endian methods of data alignment. The data alignment is specified using the external pin (MD5) at power-on reset as shown in table 9.5.

Table 9.5 Correspondence between External Pin (MD5) and Endians

MD5	Endian
0	Big endian
1	Little endian

Bit	Bit Name	Initial Value	R/W	Description
15	TYPE3	0	R/W	Memory Type
14	TYPE2	0	R/W	Specify the type of memory connected to a space.
13	TYPE1	0	R/W	0000: Normal space
12	TYPE0	0	R/W	0001: Burst ROM (clock asynchronous)
				0010: Reserved (setting prohibited)
				0011: Byte-selection SRAM
				0100: SDRAM
				0101: PCMCIA
				0110: Reserved (setting prohibited)
				0111: Burst ROM (clock synchronous)
				1000: Reserved (setting prohibited)
				1001: Reserved (setting prohibited)
				1010: Reserved (setting prohibited)
				1011: Reserved (setting prohibited)
				1100: Reserved (setting prohibited)
				1101: Reserved (setting prohibited)
				1110: Reserved (setting prohibited)
				1111: Reserved (setting prohibited)
				Note: Memory type for area 0 immediately after reset is normal space. The normal space, burst ROM (clock asynchronous), or burst ROM (clock synchronous) can be selected by these bits.
				For details on memory type in each area, see tables 9.2 and 9.3.
11	—	0	R	Reserved
				This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11	TRCD1	0	R/W	Number of Cycles from ACTV Command to READ(A)/WRIT(A) Command
10	TRCD0	1	R/W	Specify the number of minimum cycles from issuing ACTV command to issuing READ(A)/WRIT(A) command. The setting for areas 2 and 3 is common. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	A3CL1	1	R/W	CAS Latency for Area 3.
7	A3CL0	0	R/W	Specify the CAS latency for area 3. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles When connecting the SDRAM to area 2 and area 3, set the CAS latency to the bits 8 and 7 in the CS2WCR register and the SDMR2 and SDMR3 registers for SDRAM mode setting. (See table 9.19.)
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	TRWL1	0	R/W	Number of Cycles from WRITA/WRIT Command to Auto-Precharge/PRE Command
3	TRWL0	0	R/W	Specifies the number of cycles from issuing WRITA/WRIT command to the start of auto-precharge or to issuing PRE command. The setting for areas 2 and 3 is common. 00: 0 cycles 01: 1 cycle 10: 2 cycles 11: 3 cycles

Table 9.16 Relationship between A2/3BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (5)-1

Setting				
A2/3 BSZ [1:0]	**A2/3 ROW [1:0]**	**A2/3 COL [1:0]**		
10 (16 bits)	**01 (12 bits)**	**01 (9 bits)**		
Output Pin of This LSI	**Row Address Output**	**Column Address Output**	**Synchronous DRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16		
A15	A24	A15		
A14	A23*2	A23*2	A13 (BA1)	Specifies bank
A13	A22*2	A22*2	A12 (BA0)	
A12	A21	A12	A11	Address
A11	A20	L/H*1	A10/AP	Specifies address/precharge
A10	A19	A10	A9	Address
A9	A18	A9	A8	
A8	A17	A8	A7	
A7	A16	A7	A6	
A6	A15	A6	A5	
A5	A14	A5	A4	
A4	A13	A4	A3	
A3	A12	A3	A2	
A2	A11	A2	A1	
A1	A10	A1	A0	
A0	A9	A0		Unused
Example of connected memory				
128-Mbit product (2 Mwords x 16 bits x 4 banks, column 9 bits product): 1				

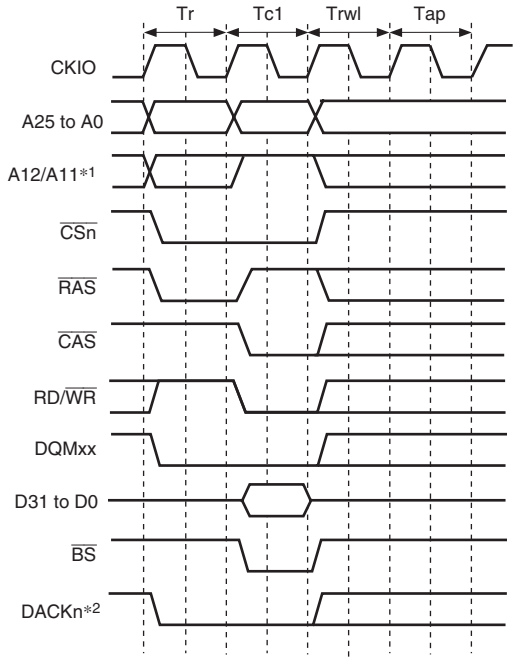
Notes: 1. L/H is a bit used in the command specification; it is fixed at low or high according to the access mode.

2. Bank address specification

(6) Single Write

A write access ends in one cycle when data is written in non-cacheable region and the data bus width is larger than or equal to access size.

Figure 9.18 shows the single write basic timing.



Notes: 1. Address pin to be connected to the A10 pin of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 9.18 Basic Timing for Single Write (Auto-Precharge)

10.2 Input/Output Pins

The external pins for the DMAC are described below. Table 10.1 lists the configuration of the pins that are connected to external bus. The DMAC has pins for 2 channels (channels 0 and 1) for external bus use.

Table 10.1 Pin Configuration

Channel	Name	Pin Name	I/O	Function
0	DMA transfer request	$\overline{\text{DREQ0}}$	Input	DMA transfer request input from external device to channel 0
	DMA transfer request reception	$\overline{\text{DACK0}}$	Output	DMA transfer request acknowledge output from channel 0 to external device
	DMA transfer end	$\overline{\text{TEND0}}$	Output	DMA transfer end of DMAC channel 0 output of
1	DMA transfer request	$\overline{\text{DREQ1}}$	Input	DMA transfer request input from external device to channel 1
	DMA transfer request reception	$\overline{\text{DACK1}}$	Output	DMA transfer request acknowledge output from channel 1 to external device
	DMA transfer end	$\overline{\text{TEND1}}$	Output	DMA transfer end of DMAC channel 1 output

Section 15 16-Bit Timer Pulse Unit (TPU)

This LSI has an on-chip 16-bit timer pulse unit (TPU) that comprises four 16-bit timer channels.

15.1 Features

- Maximum 4-pulse output
  - A total of 16 timer general registers (TGRA to TGRD × 4 ch.) are provided (four each for channels). TGRA can be set as an output compare register.
  - TGRB, TGRC, and TGRD for each channel can also be used as timer counter clearing registers. TGRC and TGRD can also be used as buffer registers.
- Selection of four counter input clocks for channels 0 and 1, and of six counter input clocks for channels 2 and 3.
- The following operations can be set for each channel:
  - Waveform output at compare match: Selection of 0, 1, or toggle output
  - Counter clear operation: Counter clearing possible by compare match
  - PWM mode: Any PWM output duty can be set
    Maximum of 4-phase PWM output possible
- Buffer operation settable for each channel
  - Automatic rewriting of output compare register possible
- Phase counting mode settable independently for each of channels 2, and 3
  - Two-phase encoder pulse up/down-count possible
- An interrupt request for each channel (TPIn (n = 0, 1, 2, 3))
  - For channels 0 and 1, compare match interrupts and overflow interrupts can be requested independently
  - For channels 2, and 3, compare match interrupts, overflow interrupts, and underflow interrupts can be requested independently

Table 15.1 lists the functions of the TPU.

(8) Synchronization-Pulse Output Mode at End of Each Slot (SYNCAT Bit = 1)

Synchronous pulse method, falling edge sampling, slot No.0 used for left-channel data, slot No.1 used for right-channel data, slot No.2 used for control channel 0 data, slot No.3 used for control channel 1 data, and frame length = 128 bits

In this mode, valid data must be set to slot No. 0.

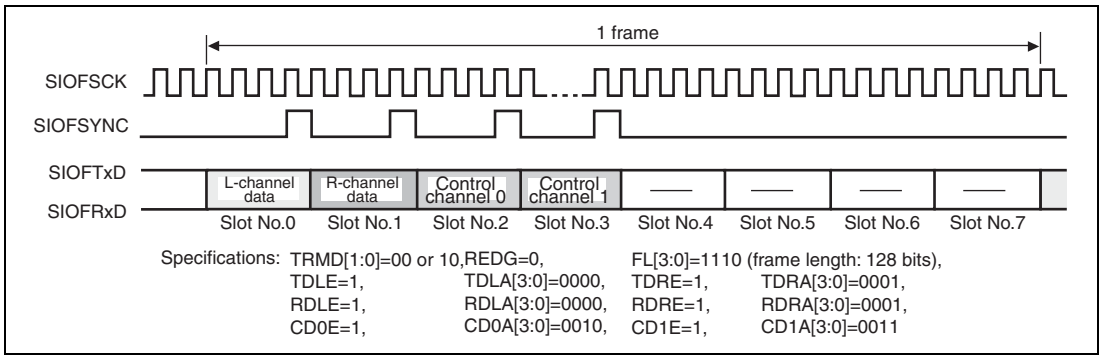
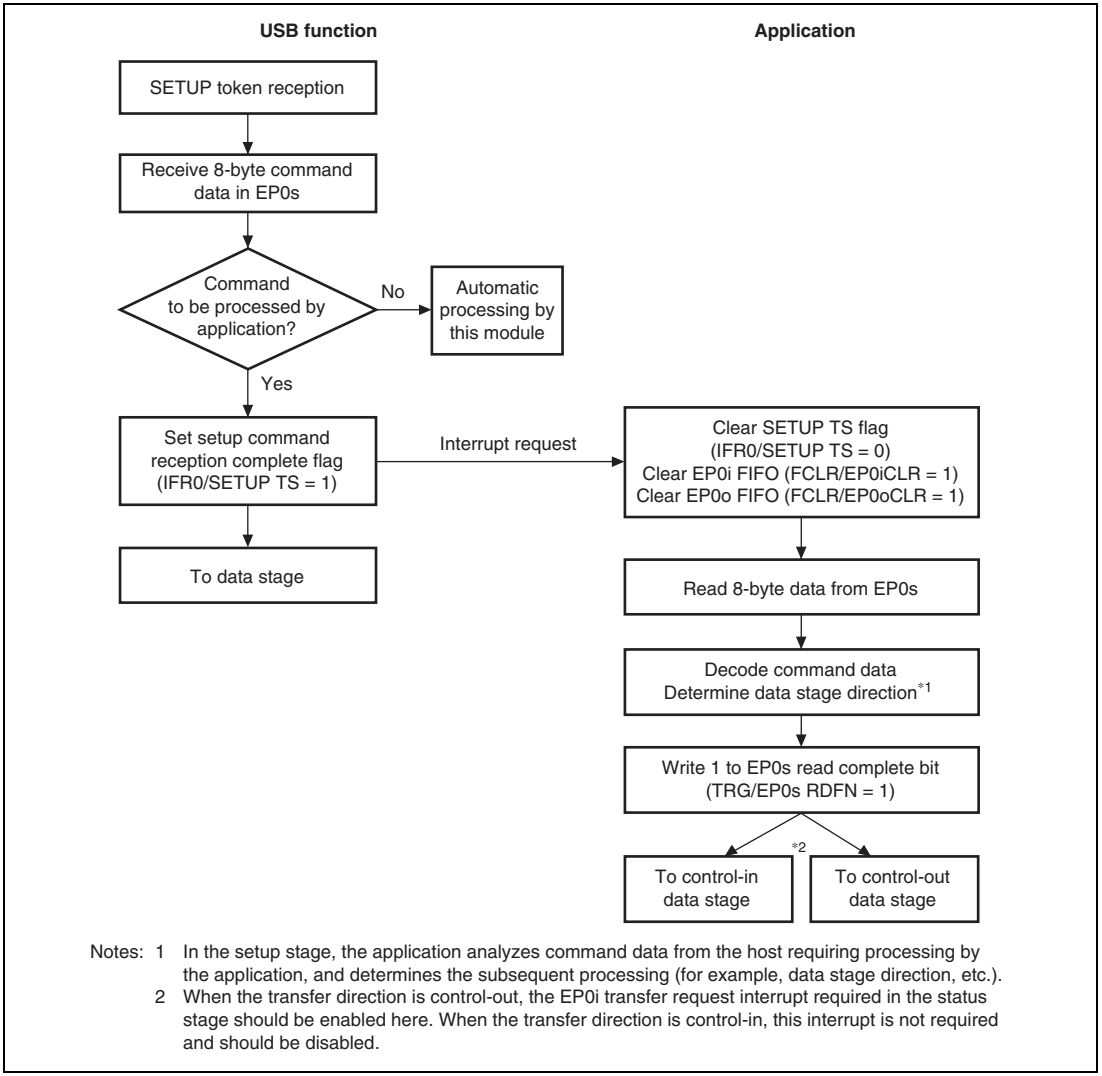


Figure 21.20 Transmit and Receive Timing (16-Bit Stereo Data)

- Setup Stage



Notes: 1 In the setup stage, the application analyzes command data from the host requiring processing by the application, and determines the subsequent processing (for example, data stage direction, etc.).
2 When the transfer direction is control-out, the EP0i transfer request interrupt required in the status stage should be enabled here. When the transfer direction is control-in, this interrupt is not required and should be disabled.

Figure 25.6 Setup Stage Operation

26.3.18 LCDC Power-Supply Sequence Period Register (LDPSPR)

LDPSPR controls the power supply circuit that provides power to the LCD module. The timing to start outputting the timing signals to the LCD_VEPWC and LCD_VCPWC pins is specified.

Bit	Bit Name	Initial Value	R/W	Description
15	ONA3	1	R/W	LCDC Power-On Sequence Period
14	ONA2	1	R/W	Set the period from LCD_VCPWC assertion to starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-on sequence of the LCD module in frame units.
13	ONA1	1	R/W	
12	ONA0	1	R/W	
				Specify to the value of (the period)-1.
				This period is the (a) period in figures 26.4 to 26.7, Power-Supply Control Sequence and States of the LCD Module.
11	ONB3	0	R/W	LCDC Power-On Sequence Period
10	ONB2	1	R/W	Set the period from starting output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) to the LCD_VEPWC assertion in the power-on sequence of the LCD module in frame units.
9	ONB1	1	R/W	
8	ONB0	0	R/W	
				Specify to the value of (the period)-1.
				This period is the (b) period in figures 26.4 to 26.7, Power-Supply Control Sequence and States of the LCD Module.
7	OFFE3	0	R/W	LCDC Power-Off Sequence Period
6	OFFE2	0	R/W	Set the period from LCD_VEPWC negation to stopping output of the display data (LCD_DATA) and timing signals (LCD_FLM, LCD_CL1, LCD_CL2, and LCD_M_DISP) in the power-off sequence of the LCD module in frame units.
5	OFFE1	0	R/W	
4	OFFE0	0	R/W	
				Specify to the value of (the period)-1.
				This period is the (e) period in figures 26.4 to 26.7, Power-Supply Control Sequence and States of the LCD Module.

Bit	Bit Name	Initial Value	R/W	Description
1	P0BW	0	R/W	PCC0 Battery Warning Indicates whether the BVD2 and BVD1 of the PC card are in the state in which "the battery must be changed although the data is guaranteed" when the PC card connected to area 6 is on the IC memory card interface. When the BVD2 and BVD1 are 0 and 1, respectively, the P0BW bit is set to 1; in other cases, the P0BW bit remains at 0. This bit is updated when the BVD2 and BVD1 are changed. Write 0 to bit 1 in order to clear this bit to 0. This bit is not changed if 1 is written. This bit always reads 0 on the I/O card interface. 0: BVD2 and BVD1 of the PC card are not in the battery warning state when the PC card is in the IC memory card interface 1: BVD2 and BVD1 of the PC card are in the battery warning state and "the battery must be changed although the data is guaranteed" when the PC card is on the IC memory card interface
0	P0BD	0	R/W	PCC0 Battery Dead Indicates whether the BVD2 and BVD1 of the PC card are in the state in which "the battery must be changed since the data is not guaranteed" when the PC card connected to area 6 is on the IC memory card interface. When the BVD2 and BVD1 are 1 and 0 or 0 and 0, the P0BD bit is set to 1; in other cases, the P0BD bit remains at 0. This bit is updated when the BVD2 and BVD1 are changed. Write 0 to bit 0 in order to clear this bit to 0. This bit is not changed if 1 is written. This bit always reads 0 on the I/O card interface. 0: BVD2 and BVD1 of the PC card are not in the state in which "the battery must be changed since the data is not guaranteed" when the PC card is on the IC memory card interface 1: BVD2 and BVD1 of the PC card are in the state in which "the battery must be changed since the data is not guaranteed" when the PC card is on the IC memory card interface

36.2 Input/Output Pins

Table 36.1 shows the pin configuration of the H-UDI.

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size
EP3 data register	EPDR3	8	H'A442 0018	USBF	8
EP4 data register	EPDR4	8	H'A442 001C		8
EP5 data register	EPDR5	8	H'A442 0020		8
EP0o receive data size register	EPSZ0o	8	H'A442 0024		8
EP1 receive data size register	EPSZ1	8	H'A442 0025		8
EP4 receive data size register	EPSZ4	8	H'A442 0026		8
Data status register	DASTS	8	H'A442 0027		8
FIFO clear register 0	FCLR0	8	H'A442 0028		8
FIFO clear register 1	FCLR1	8	H'A442 0029		8
Endpoint stall register 0	EPSTL0	8	H'A442 002A		8
Endpoint stall register 1	EPSTL1	8	H'A442 002B		8
Trigger register	TRG	8	H'A442 002C		8
DMA transfer setting register	DMA	8	H'A442 002D		8
Configuration value register	CVR	8	H'A442 002E		8
Control register 0	CTLR0	8	H'A442 002F		8
Time stamp register H	TSRH	8	H'A442 0030		8
Time stamp register L	TSRL	8	H'A442 0031		8
Endpoint information register	EPIR	8	H'A442 0032		8
Interrupt flag register 4	IFR4	8	H'A442 0034		8
Interrupt enable register 4	IER4	8	H'A442 0035		8
Interrupt select register 4	ISR4	8	H'A442 0036		8
Control register 1	CTLR1	8	H'A442 0037		8
Timer register H	TMRH	8	H'A442 0038		8
Timer register L	TMRL	8	H'A442 0039		8
Set time out register H	STOH	8	H'A442 003A		8
Set time out register L	STOL	8	H'A442 003B		8
Palette data register 00 to Palette data register FF	LDPR00 to LDPRFF	32	H'A440 0000 to H'A440 03FC	LCDC	32
LCDC input clock register	LDICKR	16	H'A440 0400		16
LCDC module type register	LDMTR	16	H'A440 0402		16

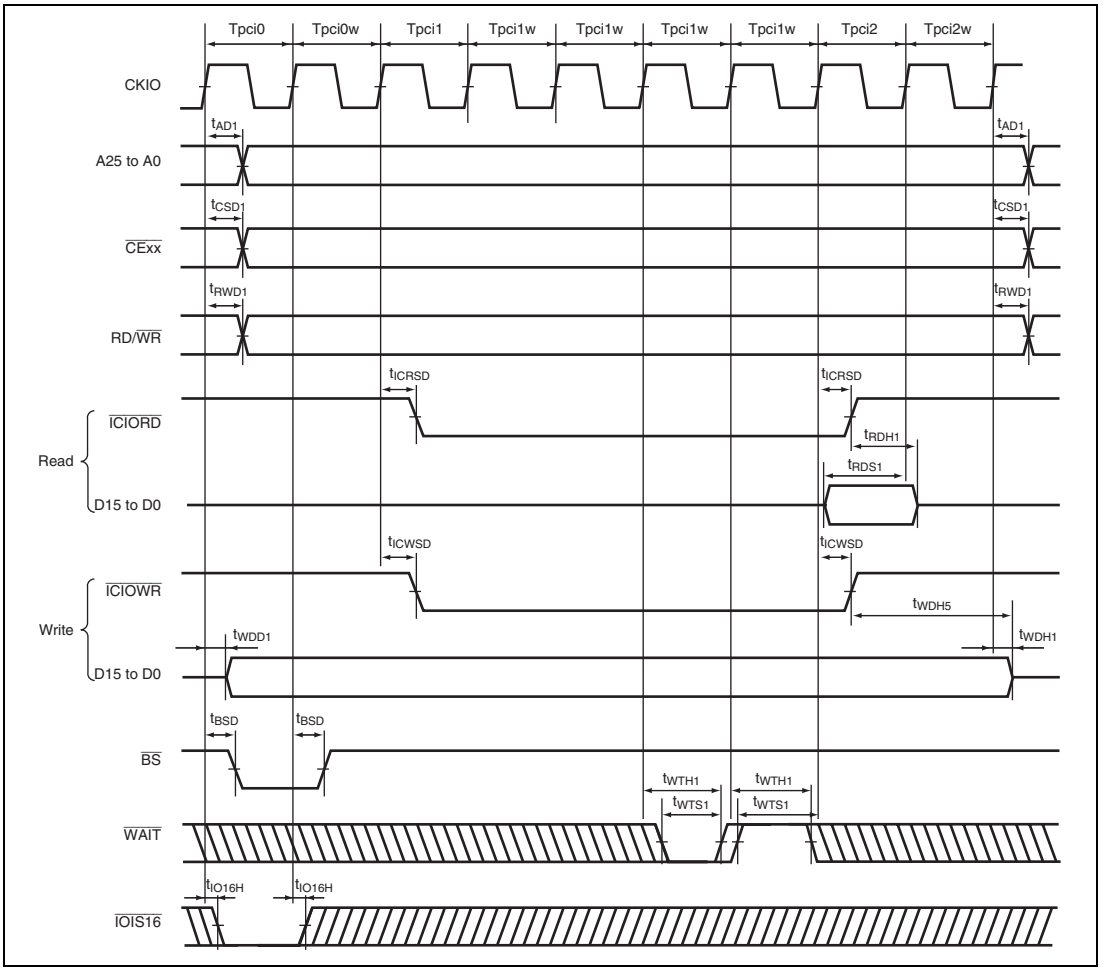


Figure 38.42 PCMCIA I/O Card Interface Bus Timing (TED[3:0] = B'0010, TEH[3:0] = B'0001, Software Wait 1, Hardware Wait 1)

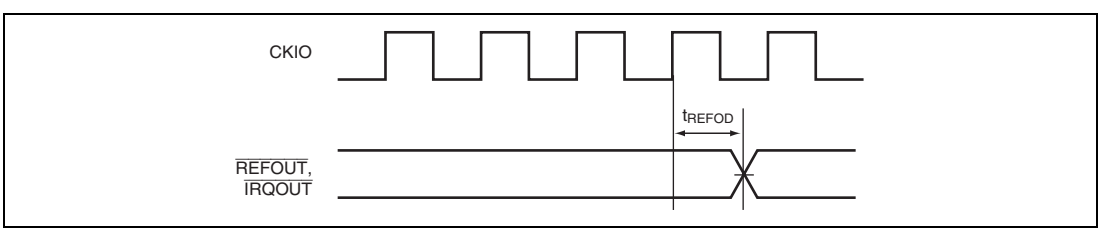


Figure 38.43 REFOUT, IRQOUT Delay Time