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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | SH-3 DSP |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 133MHz |
| Co-Processors/DSP | - |
| RAM Controllers | - |
| Graphics Acceleration | - |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 3.3V |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Security Features | - |
| Package / Case | 81-LFBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r8a77210c133bgv |

**Table 5.3 Way Replacement when a PREF Instruction Misses the Cache**

| DSP Bit | W3LOAD | W3LOCK | W2LOAD | W2LOCK | Way to be Replaced |
|---|---|---|---|---|---|
| 0 | * | * | * | * | Determined by LRU (table 5.2) |
| 1 | * | 0 | * | 0 | Determined by LRU (table 5.2) |
| 1 | * | 0 | 0 | 1 | Determined by LRU (table 5.5) |
| 1 | 0 | 1 | * | 0 | Determined by LRU (table 5.6) |
| 1 | 0 | 1 | 0 | 1 | Determined by LRU (table 5.7) |
| 1 | 0 | * | 1 | 1 | Way 2 |
| 1 | 1 | 1 | 0 | * | Way 3 |

Note: * Don't care
W3LOAD and W2LOAD should not be set to 1 at the same time.

**Table 5.4 Way Replacement when Instructions other than the PREF Instruction Miss the Cache**

| DSP Bit | W3LOAD | W3LOCK | W2LOAD | W2LOCK | Way to be Replaced |
|---|---|---|---|---|---|
| 0 | * | * | * | * | Determined by LRU (table 5.2) |
| 1 | * | 0 | * | 0 | Determined by LRU (table 5.2) |
| 1 | * | 0 | * | 1 | Determined by LRU (table 5.5) |
| 1 | * | 1 | * | 0 | Determined by LRU (table 5.6) |
| 1 | * | 1 | * | 1 | Determined by LRU (table 5.7) |

Note: * Don't care
W3LOAD and W2LOAD should not be set to 1 at the same time.

**Table 5.5 LRU and Way Replacement (when W2LOCK = 1 and W3LOCK =0)**

| LRU (Bits 5 to 0) | Way to be Replaced |
|---|---|
| 000000, 000001, 000100, 010100, 100000, 100001, 110000, 110100 | 3 |
| 000011, 000110, 000111, 001011, 001111, 010110, 011110, 011111 | 1 |
| 101001, 101011, 111000, 111001, 111011, 111100, 111110, 111111 | 0 |

**Table 7.2 Instruction Positions and Restriction Types**

| Instruction Position | SPC*[1] | Illegal Instruction*[2] | Interrupt, Break*[3] | CPU Address Error*[4] |
|---|---|---|---|---|
| [A] | | | | |
| [B] | | | Retained | |
| [C1] | | Added | Retained | Instruction/data |
| [C2] | Illegal | Added | Retained | Instruction/data |

Notes: 1. A specific address is specified in the SPC if an exception occurs while SR.RC[11:0] ≥ 2.
2. There are a greater number of instructions that can be illegal instructions while SR.RC[11:0] ≥ 1.
3. An interrupt, break or DMA address error request is retained while SR.RC[11:0] ≥1.
4. A specific exception code is specified while SR.RC[11:0] ≥1.

- Example 1: Repeat loop consisting of four or greater instructions

```
            LDRS RptStart   ; [A]
            LDRE RptDtct + 4      ; [A]
            SETRC #4        ; [A]
            instr0          ; [A]
RptStart:   instr1          ; [A] [Repeat start instruction]
            ……              ; [A]
            ……              ; [A]
RptDtct:    RptDtct         ; [B] A repeat detection
                                  instruction is an
                                  instruction three
                                  instructions before a
                                  repeat end instruction
            RptDtct1        ; [C1]
            RptDtct2        ; [C2]
RptEnd:     RptDtct3        ; [C2] [Repeat end instruction]
            instrNext       ; [A]
```

### 8.3.10 Interrupt Request Register 6 (IRR6)

IRR6 is an 8-bit register that indicates whether interrupt requests from the PINT, SIOF0, and SIOF1 are generated. This register is initialized to H'00 by a power-on reset or manual reset, but is not initialized in standby mode.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7, 6 | — | All 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 5 | SIOF1IR | 0 | R/W | SIOFI1 Interrupt Request<br>Indicates whether the SIOFI1 (SIOF1) interrupt request is generated.<br>0: SIOFI1 interrupt request is not generated<br>1: SIOFI1 interrupt request is generated |
| 4 | SIOF0IR | 0 | R/W | SIOFI0 Interrupt Request<br>Indicates whether the SIOFI0 (SIOF0) interrupt request is generated.<br>0: SIOFI0 interrupt request is not generated<br>1: SIOFI0 interrupt request is generated |
| 3, 2 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 1 | PINTBR | 0 | R/W | PINTB Interrupt Request<br>Indicates whether the PINTB (PINT) interrupt request is generated.<br>0: PINTB interrupt request is not generated<br>1: PINTB interrupt request is generated |
| 0 | PINTAR | 0 | R/W | PINTA Interrupt Request<br>Indicates whether the PINTA (PINT) interrupt request is generated.<br>0: PINTA interrupt request is not generated<br>1: PINTA interrupt request is generated |

**Table 9.13 Relationship between A2/3BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (2)-1**

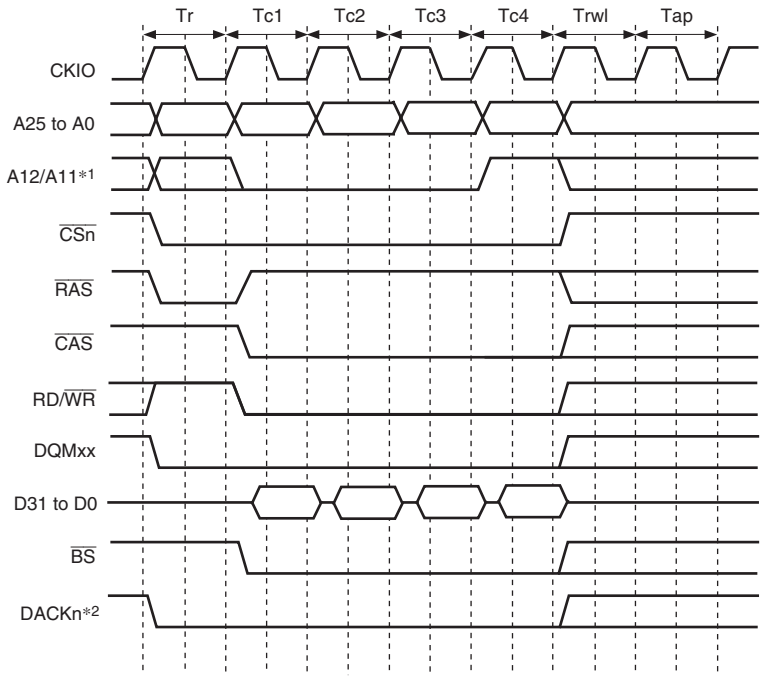
| Setting | | | | |
|---|---|---|---|---|
| **A2/3 BSZ [1:0]** | **A2/3 ROW [1:0]** | **A2/3 COL [1:0]** | | |
| **11 (32 bits)** | **01 (12 bits)** | **01 (9 bits)** | | |
| **Output Pin of This LSI** | **Row Address Output** | **Column Address Output** | **Synchronous DRAM Pin** | **Function** |
| A17 | A26 | A17 | | Unused |
| A16 | A25 | A16 | | |
| A15 | A24*2 | A24*2 | A13 (BA1) | Specifies bank |
| A14 | A23*2 | A23*2 | A12 (BA0) | |
| A13 | A22 | A13 | A11 | Address |
| A12 | A21 | L/H*1 | A10/AP | Specifies address/precharge |
| A11 | A20 | A11 | A9 | Address |
| A10 | A19 | A10 | A8 | |
| A9 | A18 | A9 | A7 | |
| A8 | A17 | A8 | A6 | |
| A7 | A16 | A7 | A5 | |
| A6 | A15 | A6 | A4 | |
| A5 | A14 | A5 | A3 | |
| A4 | A13 | A4 | A2 | |
| A3 | A12 | A3 | A1 | |
| A2 | A11 | A2 | A0 | |
| A1 | A10 | A1 | | Unused |
| A0 | A9 | A0 | | |
| Example of connected memory | | | | |
| 256-Mbit product (2 Mwords x 32 bits x 4 banks, column 9 bits product): 1<br>128-Mbit product (2 Mwords x 16 bits x 4 banks, column 9 bits product): 2 | | | | |

Notes: 1. L/H is a bit used in the command specification; it is fixed at low or high according to the access mode.
2. Bank address specification

**Table 9.15 Relationship between A2/3BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (4)-2**

| Setting | | | | |
|---|---|---|---|---|
| **A2/3 BSZ [1:0]** | **A2/3 ROW [1:0]** | **A2/3 COL [1:0]** | | |
| **10 (16 bits)** | **01 (12 bits)** | **00 (8 bits)** | | |
| **Output Pin of This LSI** | **Row Address Output** | **Column Address Output** | **Synchronous DRAM Pin** | **Function** |
| A17 | A25 | A17 | | Unused |
| A16 | A24 | A16 | | |
| A15 | A23 | A15 | | |
| A14 | A22*2 | A22*2 | A13 (BA1) | Specifies bank |
| A13 | A21*2 | A21*2 | A12 (BA0) | |
| A12 | A20 | A12 | A11 | Address |
| A11 | A19 | L/H*1 | A10/AP | Specifies address/precharge |
| A10 | A18 | A10 | A9 | Address |
| A9 | A17 | A9 | A8 | |
| A8 | A16 | A8 | A7 | |
| A7 | A15 | A7 | A6 | |
| A6 | A14 | A6 | A5 | |
| A5 | A13 | A5 | A4 | |
| A4 | A12 | A4 | A3 | |
| A3 | A11 | A3 | A2 | |
| A2 | A10 | A2 | A1 | |
| A1 | A9 | A1 | A0 | |
| A0 | A8 | A0 | | Unused |
| Example of connected memory | | | | |
| 64-Mbit product (1 Mword x 16 bits x 4 banks, column 8 bits product): 1 | | | | |

Notes: 1. L/H is a bit used in the command specification; it is fixed at low or high according to the access mode.
2. Bank address specification




Notes: 1. Address pin to be connected to the A10 pin of SDRAM.
2. The waveform for DACKn is when active low is specified.

**Figure 9.17 Basic Timing for Burst Write (Auto-Precharge)**

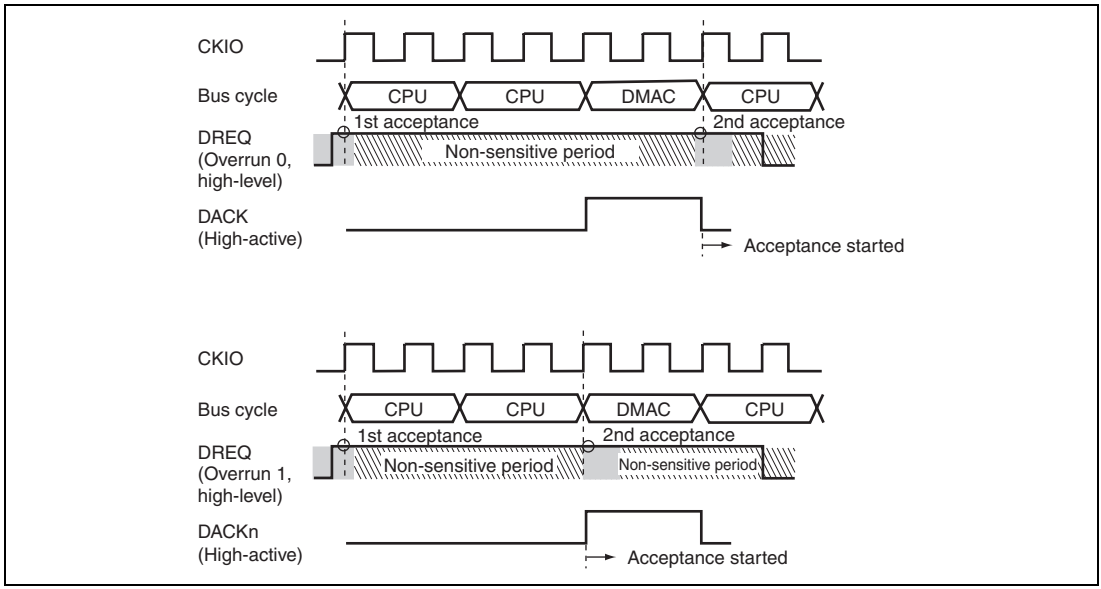



**Figure 10.14 Example of DREQ Input Detection in Cycle Steal Mode Level Detection**

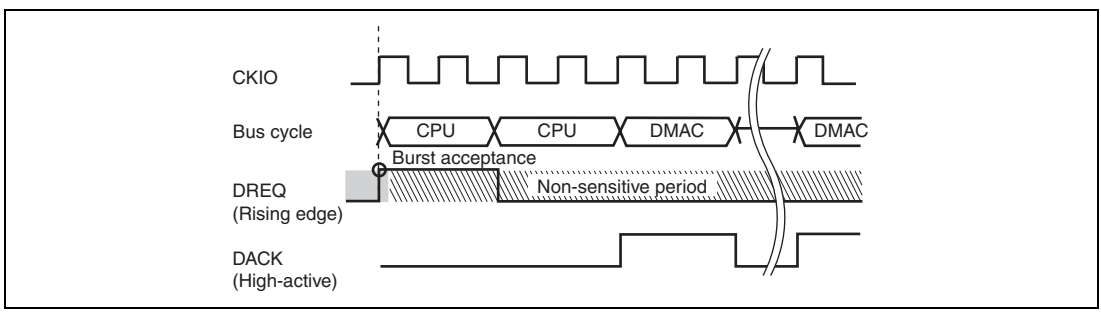



**Figure 10.15 Example of DREQ Input Detection in Burst Mode Edge Detection**

### 18.3.1 Receive Shift Register (SCRSR)

SCRSR receives serial data. Data input at the RxD pin is loaded into the SCRSR in the order received, LSB (bit 0) first, converting the data to parallel form. When one byte has been received, it is automatically transferred to the SCFRDR, which is a receive FIFO data register. The CPU cannot read from or write to the SCRSR directly.

### 18.3.2 Receive FIFO Data Register (SCFRDR)

The 64-byte receive FIFO data register (SCFRDR) stores serial receive data. The SCIF completes the reception of one byte of serial data by moving the received data from the receive shift register (SCRSR) into the SCFRDR for storage. Continuous receive is enabled until 64 bytes are stored.

The CPU can read but not write the SCFRDR. When data is read without received data in the SCFRDR, the value is undefined. When the received data in this register becomes full, the subsequent serial data is lost.

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 7 to 0 | SCFRD7 to SCFRD0 | Undefined | R | FIFO Data Registers for Serial Receive Data |

### 18.3.3 Transmit Shift Register (SCTSR)

SCTSR transmits serial data. The SCIF loads transmit data from the transmit FIFO data register (SCFTDR) into the SCTSR, then transmits the data serially from the TxD pin, LSB (bit 0) first. After transmitting one data byte, the SCI automatically loads the next transmit data from the SCFTDR into the SCTSR and starts transmitting again. The CPU cannot read or write the SCTSR directly.

### 18.3.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is a 64-byte 8-bit-length FIFO register that stores data for serial transmission. When the SCIF detects that the transmit shift register (SCTSR) is empty, it moves transmit data written in the SCFTDR into the SCTSR and starts serial transmission. Continuous serial transmission is performed until the transmit data in the SCFTDR becomes empty. The CPU can always write to the SCFTDR.

When the transmit data in the SCFTDR is full (64 bytes), next data cannot be written. If attempted to write, the data is ignored.

In serial transmission, the SCIF operates as described below.

1. When data is written into the transmit FIFO data register (SCFTDR), the SCIF transfers the data from SCFTDR to the transmit shift register (SCTSR) and starts transmitting. Confirm that the TDFE flag in the serial status register (SCSSR) is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is (64 – transmit trigger setting).
2. When data is transferred from SCFTDR to SCTSR and transmission is started, consecutive transmit operations are performed until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR falls below the transmit trigger number set in the FIFO control register (SCFCR), the TDFE flag is set. If the TIE bit in the serial control register (SCSR) is set to 1 at this time, a transmit-FIFO-data-empty interrupt request is generated. When the number of transmit data matches the data set in the transmit data stop register (SCTDSR) while the transmit data stop function is used, the transmit operation is stopped and the TSF flag in the serial status register (SCSSR) is set. When the TSIE bit in the serial control register (SCSCR) is set to 1, transmit data stop interrupt request is generated. A common interrupt vector is assigned to the transmit-FIFO-data-empty interrupt and the transmit-data-stop interrupt.

   The serial transmit data is sent from the TxD pin in the following order.

   A. Start bit: One-bit 0 is output.
   B. Transmit data: 8-bit or 7-bit data is output in LSB-first order.
   C. Parity bit: One parity bit (even or odd parity) is output. (A format in which a parity bit is not output can also be selected.)
   D. Stop bit(s): One- or two-bit 1s (stop bits) are output.
   E. Mark state: 1 is output continuously until the start bit that starts the next transmission is sent.

3. The SCIF checks the SCFTDR transmit data at the timing for sending the stop bit. If data is present, the data is transferred from SCFTDR to SCTSR, the stop bit is sent, and then serial transmission of the next frame is started.

   If there is no transmit data, the TEND flag in the serial status register (SCSSR) is set to 1, the stop bit is sent, and then the line goes to the mark state in which 1 is output continuously.

### 21.3.7 Status Register (SISTR)

SISTR is a 16-bit read-only register that shows the SIOF state. Each bit in this register becomes an SIOF interrupt source when the corresponding bit in SIIER is set to 1.

SISTR is initialized in module stop mode.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 15 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 14 | TCRDY | 0 | R | Transmit Control Data Ready<br>0: Indicates that a write to SITCR is disabled<br>1: Indicates that a write to SITCR is enabled<br>• If SITCR is written when this bit is cleared to 0, SITCR is over-written and the previous contents of SITCR are not output from the SIOFTxD pin.<br>• This bit is valid when the TXE bit in SITCR is set to 1.<br>• This bit indicates a state of the SIOF. If SITCR is written, the SIOF clears this bit.<br>• If the issue of interrupts by this bit is enabled, an SIOF interrupt is issued. |
| 13 | TFEMP | 0 | R | Transmit FIFO Empty<br>0: Indicates that transmit FIFO is not empty<br>1: Indicates that transmit FIFO is empty<br>• This bit is valid when the TXE bit in SICTR is 1.<br>• This bit indicates a state; if SITDR is written, the SIOF clears this bit.<br>• If the issue of interrupts by this bit is enabled, an SIOF interrupt is issued. |

### (2) Regarding Transmit and Receive Classification

The transmit sources and receive sources are signals indicating the state; after being set, if the state changes, they are automatically cleared by the SIOF.

When the DMA transfer is used, a DMA transfer request is pulled low (0 level) for one cycle at the end of DMA transfer.

### (3) Processing when Errors Occur

On occurrence of each of the errors indicated as a status in SISTR, the SIOF performs the following operations.

- Transmit FIFO underflow (TFUDF)
  The immediately preceding transmit data is again transmitted.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  An undefined value is output on the bus.
- FS error (FSERR)
  The internal counter is reset according to the FSYN signal in which an error occurs.
- Assign error (SAERR)
  — If the same slot is assigned to both serial data and control data, the slot is assigned to serial data.
  — If the same slot is assigned to two control data items, data cannot be transferred correctly.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 1 | EP3 TS | 0 | R/W | EP3 (Interrupt) Transmit Complete<br>[Setting condition]<br>When data to be transmitted to the host is written to EP3, then data is normally transferred from the host to the function, and an ACK handshake is returned.<br>[Clearing conditions]<br>• When reset<br>• When 0 is written to by CPU |
| 0 | VBUSF | 0 | R/W | USB Disconnection Detection<br>The USBF_VBUS pin of this module is used for detecting connection/disconnection.<br>[Setting condition]<br>When the function is connected to the USB bus or disconnected from it.<br>[Clearing conditions]<br>• When reset<br>• When 0 is written to by CPU. |

### 25.3.3 Interrupt Flag Register 2 (IFR2)

IFR2 is an interrupt flag register for SURSS, SURSF, CFDN, SOF, SETC, and SETI. When each flag is set to 1 and an interrupt is enabled in the corresponding bit of IER2, an interrupt occurs as specified by the corresponding bit in ISR2. Clearing is performed by writing 0 to the bit to be cleared. Writing 1 is not valid and nothing is changed.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7, 6 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |
| 5 | SURSS | 0 | R | Suspend/Resume Status<br>Status bit indicating the state of the bus<br>0: Normal state<br>1: Suspend state |

| Image for Display in Memory (X-Resolution × Y-Resolution) | LCD Module (X-Resolution × Y-Resolution) | Number of Colors for Display | | Number of Column Address Bits of SDRAM | Burst Length of LCDC (LDSMR*) |
|---|---|---|---|---|---|
| 80 × 160 | 160 × 80 | Monochrome | 2 bpp | 8 bits | Not more than 16 bursts |
| | | | | 9 bits | — |
| | | | | 10 bits | — |
| | | | 4 bpp (packed) | 8 bits | Not more than 8 bursts |
| | | | | 9 bits | Not more than 16 bursts |
| | | | | 10 bits | — |
| | | | 4 bpp (unpacked) | 8 bits | 4 bursts |
| | | | | 9 bits | Not more than 8 bursts |
| | | | | 10 bits | Not more than 16 bursts |
| | | | 6 bpp | 8 bits | 4 bursts |
| | | | | 9 bits | Not more than 8 bursts |
| | | | | 10 bits | Not more than 16 bursts |
| | | Color | 4 bpp (packed) | 8 bits | Not more than 8 bursts |
| | | | | 9 bits | Not more than 16 bursts |
| | | | | 10 bits | — |
| | | | 4 bpp (unpacked) | 8 bits | 4 bursts |
| | | | | 9 bits | Not more than 8 bursts |
| | | | | 10 bits | Not more than 16 bursts |
| | | | 8 bpp | 8 bits | 4 bursts |
| | | | | 9 bits | Not more than 8 bursts |
| | | | | 10 bits | Not more than 16 bursts |
| | | | 16 bpp | 8 bits | Unusable |
| | | | | 9 bits | 4 bursts |
| | | | | 10 bits | Not more than 8 bursts |

### 30.4.2 Data Format

Figure 30.2 shows the data format used by the smart card interface. The smart card interface performs a parity check for each frame during reception.

During reception in T = 0 mode, if a parity error is detected, an error signal is returned to the transmit side, requesting data retransmission. When the transmit side samples the error signal, it retransmits the same data.

During reception in T = 1 mode, if a parity error is detected, an error signal is not returned. During transmission, error signals are not sampled and data is not retransmitted.

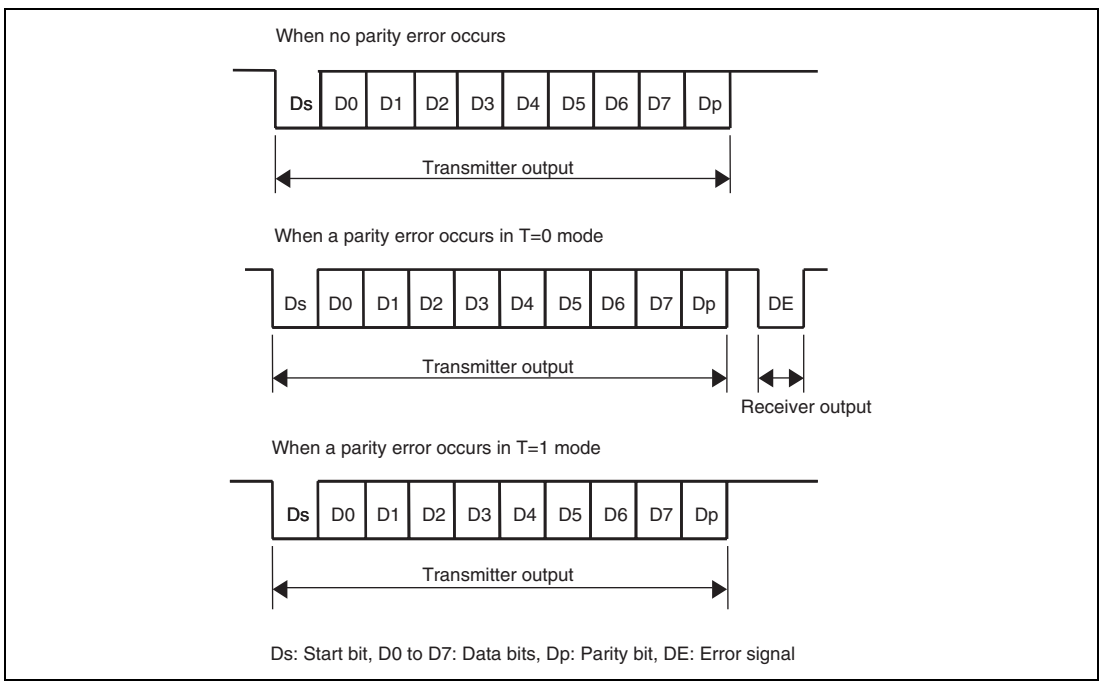



**Figure 30.2 Data Format Used by Smart Card Interface**

The operation sequence is as follows.

1. When not in use, the data line is in a high-impedance state and fixed at high level by a pull-up resistance.
2. The transmit side initiates transmission of one frame of data. The data frame begins with the start bit (Ds: low level). This is followed by eight data bits (D0 to D7) and the parity bit (Dp).

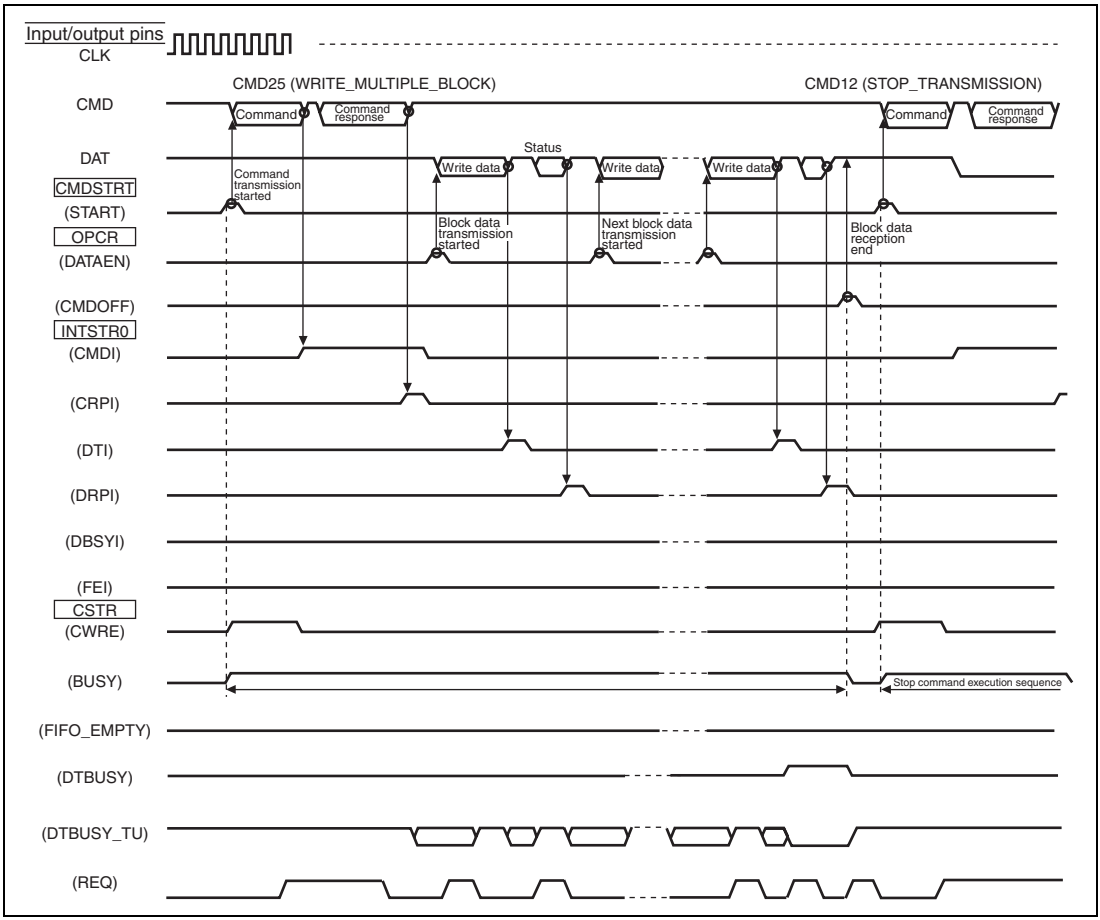



**Figure 31.17 Example of Command Sequence for Commands with Write Data (Multiblock Transfer)**

| Bit | Pin Name | I/O | Bit | Pin Name | I/O |
|---|---|---|---|---|---|
| 187 | SIOF1_MCLK/SD_DAT1/TPU_TI3B/ PTU3 | IN | 168 | PCC_RESET/PINT7/PTK3 | OUT |
| 186 | SIOF1_SYNC/SD_DAT2/PTU4 | IN | 167 | $\overline{\text{ASEBRKAK}}$/PTJ5 | OUT |
| 185 | SIM_CLK/SCIF1_SCK/SD_DAT3/ PTV0 | IN | 166 | $\overline{\text{AUDSYNC}}$/PTJ0 | OUT |
| 184 | SIM_RST/SCIF1_RxD/SD_WP/PTV1 | IN | 165 | AUDCK/PTJ6 | OUT |
| 183 | SIM_D/SCIF1_TxD/SD_CD/PTV2 | IN | 164 | AUDATA0/PTJ1 | OUT |
| 182 | $\overline{\text{MMC\_ODMOD}}$/$\overline{\text{SCIF1\_RTS}}$/ LCD_VCPWC/TPU_TO2/PTV3 | IN | 163 | AUDATA1/PTJ2 | OUT |
| 181 | MMC_VDDON/$\overline{\text{SCIF1\_CTS}}$/ LCD_VEPWC/TPU_TO3/PTV4 | IN | 162 | AUDATA2/PTJ3 | OUT |
| 180 | USB1d_TXENL/PINT8/ $\overline{\text{PCC\_CD1}}$/PTG0 | IN | 161 | AUDATA3/PTJ4 | OUT |
| 179 | USB1d_SPEED/PINT9/ $\overline{\text{PCC\_CD2}}$/PTG1 | IN | 160 | IRQ0/$\overline{\text{IRL0}}$/PTP0 | OUT |
| 178 | USB1d_DPLS/PINT10/AFE_HC1/ PCC_BVD1/PTG2 | IN | 159 | IRQ1/$\overline{\text{IRL1}}$/PTP1 | OUT |
| 177 | USB1d_DMNS/PINT11/AFE_RLYCNT/ PCC_BVD2/PTG3 | IN | 158 | IRQ2/$\overline{\text{IRL2}}$/PTP2 | OUT |
| 176 | USB1d_TXDPLS/AFE_SCLK/$\overline{\text{IOIS16}}$/ $\overline{\text{PCC\_IOIS16}}$/PTG4 | IN | 157 | IRQ3/$\overline{\text{IRL3}}$/PTP3 | OUT |
| 175 | USB1d_TXSE0/IRQ4/AFE_TXOUT/ $\overline{\text{PCC\_DRV}}$/PTG5 | IN | 156 | SCIF0_SCK/PTT0 | OUT |
| 174 | USB1d_RCV/IRQ5/AFE_FS/ $\overline{\text{PCC\_REG}}$/PTG6 | IN | 155 | SCIF0_RxD/IrRX/PTT1 | OUT |
| 173 | USB1d_SUSPEND/$\overline{\text{REFOUT}}$/ $\overline{\text{IRQOUT}}$/PTP4 | IN | 154 | SCIF0_TxD/IrTX/PTT2 | OUT |
| 172 | $\overline{\text{USB1\_ovr\_current}}$/USBF_VBUS | IN | 153 | $\overline{\text{SCIF0\_RTS}}$/TPU_TO0/PTT3 | OUT |
| 171 | $\overline{\text{PCC\_VS1}}$/PINT4/PTK0 | OUT | 152 | $\overline{\text{SCIF0\_CTS}}$/TPU_TO1/PTT4 | OUT |
| 170 | $\overline{\text{PCC\_VS2}}$/PINT5/PTK1 | OUT | 151 | MMC_CLK/SIOF1_SCK/SD_CLK/ TPU_TI2A/PTU0 | OUT |
| 169 | PCC_RDY/PINT6/PTK2 | OUT | 150 | MMC_CMD/SIOF1_RxD/SD_CMD/ TPU_TI2B_PTU1 | OUT |

## 37.1 Register Addresses

Entries under Access Size indicate number of bits.

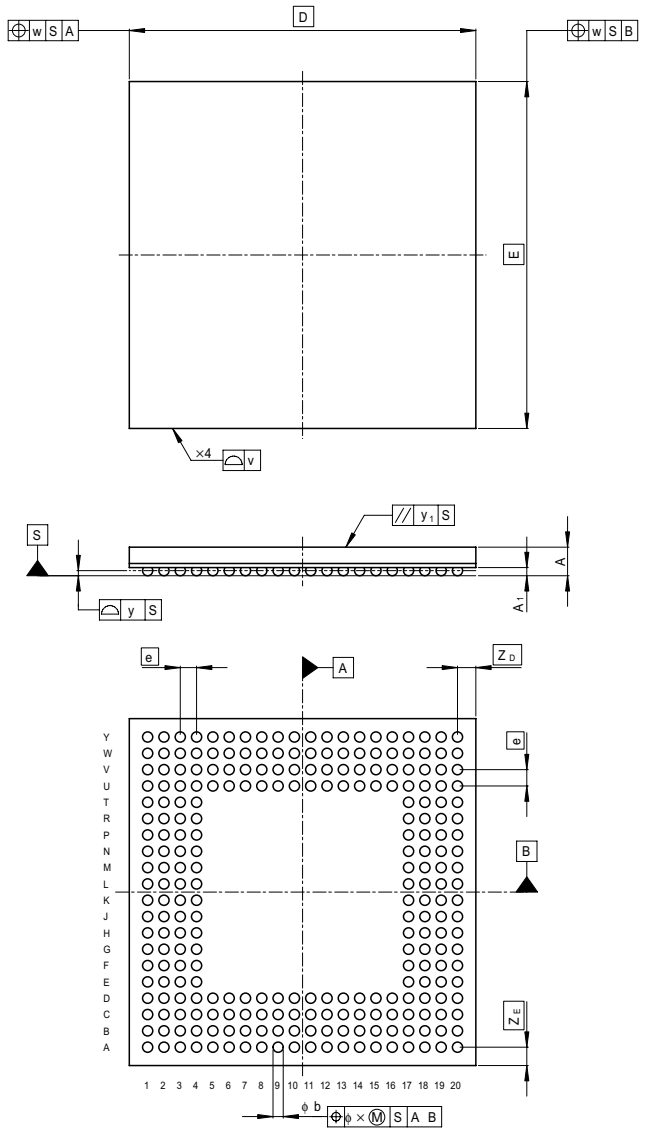
Note: Access to undefined or reserved address is prohibited. Since operation or continued operation is not guaranteed when these registers are accessed, do not attempt such access.

| Register Name | Abbreviation | Number of Bits | Address | Module | Access Size |
|---|---|---|---|---|---|
| MMU control register | MMUCR | 32 | H'FFFF FFE0 | MMU | 32 |
| Page table entry register high | PTEH | 32 | H'FFFF FFF0 | | 32 |
| Page table entry register low | PTEL | 32 | H'FFFF FFF4 | | 32 |
| Translation table base register | TTB | 32 | H'FFFF FFF8 | | 32 |
| Cache control register 2 | CCR2 | 32 | H'A400 00B0 | Cache | 32 |
| Cache control register 3 | CCR3 | 32 | H'A400 00B4 | | 32 |
| Cache control register 1 | CCR1 | 32 | H'FFFF FFEC | | 32 |
| Interrupt event register 2 | INTEVT2 | 32 | H'A400 0000 | Exception handling | 32 |
| TRAPA exception register | TRA | 32 | H'FFFF FFD0 | | 32 |
| Exception event register | EXPEVT | 32 | H'FFFF FFD4 | | 32 |
| Interrupt event register | INTEVT | 32 | H'FFFF FFD8 | | 32 |
| Exception address register | TEA | 32 | H'FFFF FFFC | | 32 |
| Interrupt priority register F | IPRF | 16 | H'A408 0000 | INTC | 16 |
| Interrupt priority register G | IPRG | 16 | H'A408 0002 | | 16 |
| Interrupt priority register H | IPRH | 16 | H'A408 0004 | | 16 |
| Interrupt priority register I | IPRI | 16 | H'A408 0006 | | 16 |
| Interrupt priority register J | IPRJ | 16 | H'A408 0008 | | 16 |
| Interrupt request register 5 | IRR5 | 8 | H'A408 0020 | | 8 |
| Interrupt request register 6 | IRR6 | 8 | H'A408 0022 | | 8 |
| Interrupt request register 7 | IRR7 | 8 | H'A408 0024 | | 8 |
| Interrupt request register 8 | IRR8 | 8 | H'A408 0026 | | 8 |
| Interrupt request register 9 | IRR9 | 8 | H'A408 0028 | | 8 |
| Interrupt request register 0 | IRR0 | 8 | H'A414 0004 | | 8 |

| Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 | Module |
|---|---|---|---|---|---|---|---|---|---|
| TIER_2 | — | — | — | — | — | — | — | — | TPU |
| | — | — | TC1EU | TC1EV | TG1ED | TG1EC | TG1EB | TG1EA | |
| TSR_2 | — | — | — | — | — | — | — | — | |
| | TCFD | — | TCFU | TCFV | TGFD | TGFC | TGFB | TGFA | |
| TCNT_2 | | | | | | | | | |
| TGRA_2 | | | | | | | | | |
| TGRB_2 | | | | | | | | | |
| TGRC_2 | | | | | | | | | |
| TGRD_2 | | | | | | | | | |
| TCR_3 | — | — | — | — | — | — | — | — | |
| | CCLR2 | CCLR1 | CCLR0 | CKEG1 | CKEG0 | TPSC2 | TPSC1 | TPSC0 | |
| TMDR_3 | — | — | — | — | — | — | — | — | |
| | — | BFWT | BFB | BFA | — | MD2 | MD1 | MD0 | |
| TIOR_3 | — | — | — | — | — | — | — | — | |
| | — | — | — | — | — | IOA2 | IOA1 | IOA0 | |
| TIER_3 | — | — | — | — | — | — | — | — | |
| | — | — | TC1EU | TC1EV | TG1ED | TG1EC | TG1EB | TG1EA | |
| TSR_3 | — | — | — | — | — | — | — | — | |
| | TCFD | — | TCFU | TCFV | TGFD | TGFC | TGFB | TGFA | |
| TCNT_3 | | | | | | | | | |
| TGRA_3 | | | | | | | | | |
| TGRB_3 | | | | | | | | | |

# C. Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA256-17x17-0.80 | PLBG0256GA-A | BP-256H/BP-256HV | 0.6g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 17.0 | — |
| E | — | 17.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.9 | — |
| $Z_E$ | — | 0.9 | — |

**Figure C.1 Package Dimensions (PLBG0256GA-A (BP-256H/HV))**