What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
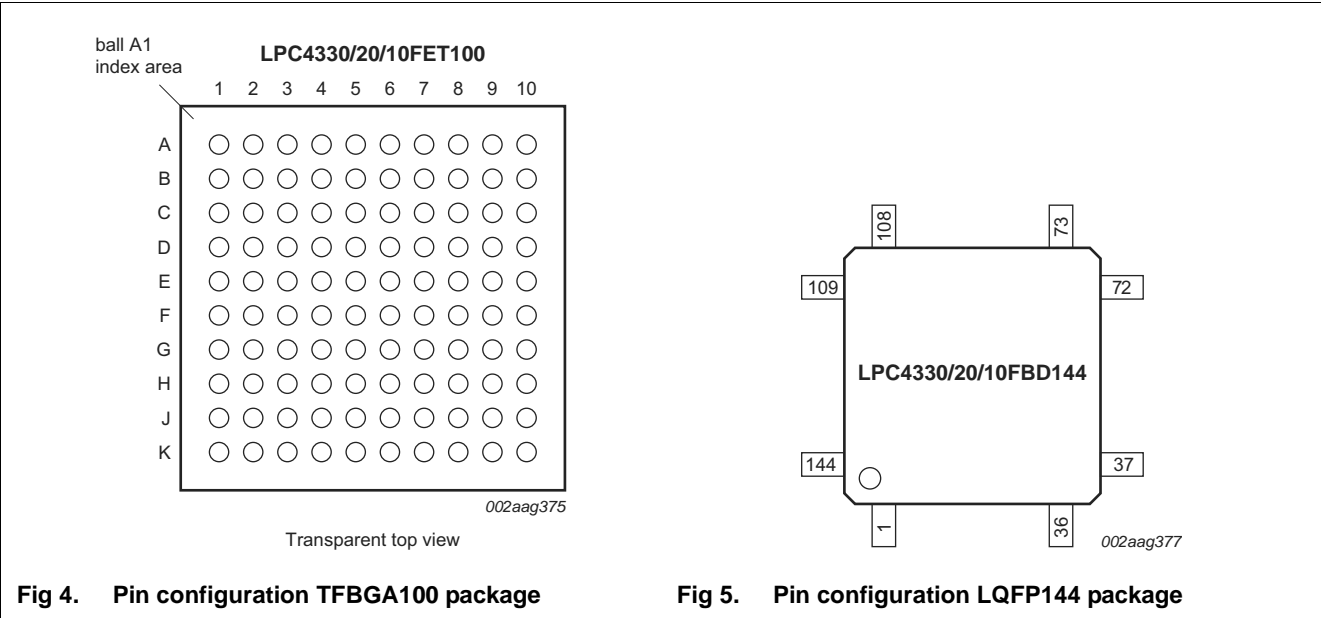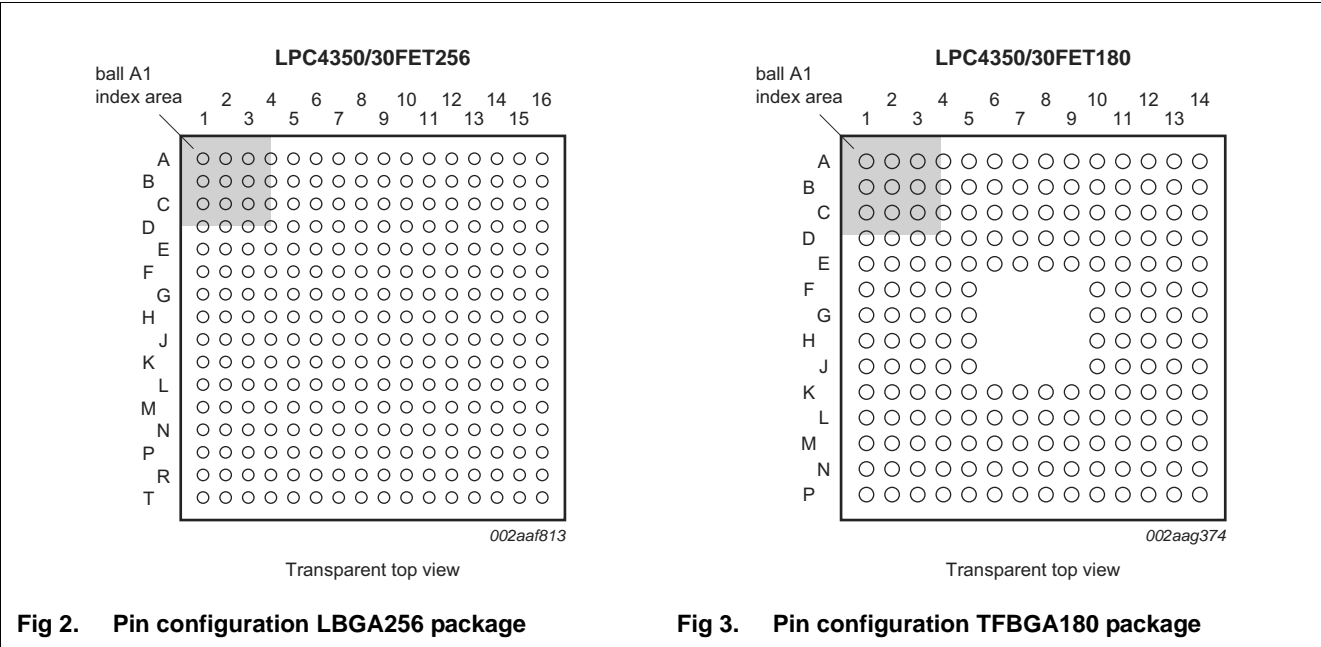
Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4320fet100-551

6. Pinning information

6.1 Pinning

Fig 2.   Pin configuration LBGA256 package

Fig 3.   Pin configuration TFBGA180 package

Fig 4.   Pin configuration TFBGA100 package

Fig 5.   Pin configuration LQFP144 package

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Table 3. **Pin description** …continued
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
PA_3	H11	E10	-	-	[3]	N; PU	I/O	**GPIO4[10]** — General purpose digital input/output pin.
							I	**QEI_PHA** — Quadrature Encoder Interface PHA input.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
PA_4	G13	E12	-	-	[2]	N; PU	-	**R** — Function reserved.
							O	**CTOUT_9** — SCTimer/PWM output 9. Match output 3 of timer 3.
							-	**R** — Function reserved.
							I/O	**EMC_A23** — External memory address line 23.
							I/O	**GPIO5[19]** — General purpose digital input/output pin.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
PB_0	B15	D14	-	-	[2]	N; PU	-	**R** — Function reserved.
							O	**CTOUT_10** — SCTimer/PWM output 10. Match output 3 of timer 3.
							O	**LCD_VD23** — LCD data.
							-	**R** — Function reserved.
							I/O	**GPIO5[20]** — General purpose digital input/output pin.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
							-	**R** — Function reserved.
PB_1	A14	A13	-	-	[2]	N; PU	-	**R** — Function reserved.
							I	**USB1_ULPI_DIR** — ULPI link DIR signal. Controls the ULP data line direction.
							O	**LCD_VD22** — LCD data.
							-	**R** — Function reserved.
							I/O	**GPIO5[21]** — General purpose digital input/output pin.
							O	**CTOUT_6** — SCTimer/PWM output 6. Match output 2 of timer 1.
							-	**R** — Function reserved.
							-	**R** — Function reserved.

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Table 3. **Pin description** …*continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
PC_11	L5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
						I	**U1_DCD —** Data Carrier Detect input for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[10] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[11] —** General purpose digital input/output pin.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
						I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
						I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_TXD —** Transmitter output for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[12] —** General purpose digital input/output pin.
						I/O	**SGPIO12 —** General purpose digital input/output pin.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
						I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						I	**U1_RXD —** Receiver input for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[13] —** General purpose digital input/output pin.
						I/O	**SGPIO13 —** General purpose digital input/output pin.
						O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
						I/O	**SD_DAT7 —** SD/MMC data bus line 7.

Table 3.   Pin description *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
PD_4	T2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
						I/O	**EMC_D18 —** External memory data line 18.
						-	**R —** Function reserved.
						I/O	**GPIO6[18] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO8 —** General purpose digital input/output pin.
PD_5	P6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3.
						I/O	**EMC_D19 —** External memory data line 19.
						-	**R —** Function reserved.
						I/O	**GPIO6[19] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO9 —** General purpose digital input/output pin.
PD_6	R6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
						I/O	**EMC_D20 —** External memory data line 20.
						-	**R —** Function reserved.
						I/O	**GPIO6[20] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO10 —** General purpose digital input/output pin.
PD_7	T6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
						I/O	**EMC_D21 —** External memory data line 21.
						-	**R —** Function reserved.
						I/O	**GPIO6[21] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO11 —** General purpose digital input/output pin.

Table 3.   **Pin description** *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See <u>Table 2</u>.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
PE_7	F15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
						I	**U1_CTS —** Clear to Send input for UART1.
						I/O	**EMC_D26 —** External memory data line 26.
						I/O	**GPIO7[7] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_8	F14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
						I	**U1_DSR —** Data Set Ready input for UART 1.
						I/O	**EMC_D27 —** External memory data line 27.
						I/O	**GPIO7[8] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_9	E16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
						I	**U1_DCD —** Data Carrier Detect input for UART 1.
						I/O	**EMC_D28 —** External memory data line 28.
						I/O	**GPIO7[9] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_10	E14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
						O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I/O	**EMC_D29 —** External memory data line 29.
						I/O	**GPIO7[10] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

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Table 3. **Pin description** *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
PF_3	E10	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[18] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
PF_4	D10	D6	H4	120	[2]	O; PU	I/O	**SSP1_SCK —** Serial clock for SSP1.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							O	**TRACECLK —** Trace clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I2S-bus specification*.
PF_5	E9	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							I/O	**GPIO7[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							AI	**ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. **Pin description** *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
WAKEUP1	A10	C8	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
WAKEUP2	C9	E5	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low-power modes. A pulse with a duration > 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins							
ADC0_0/ ADC1_0/DAC	E3	B6	A2	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	C4	A1	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	B3	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	B4	A3	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	A5	-	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	C3	-	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	A4	-	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	B5	-	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC							
RTC_ALARM	A11	A10	C3	129	[11]	O	O	RTC controlled output. This pin has an internal pull-up. The reset state of this pin is LOW after POR. For all other types of reset, the reset state depends on the state of the RTC alarm interrupt.
RTCX1	A8	A8	A5	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B7	B5	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
Crystal oscillator pins							
XTAL1	D1	C1	B1	12	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	D1	C1	13	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins							
USB0_VDDA 3V3_DRIVER	F3	E3	D1	16		-	-	Separate analog 3.3 V power supply for driver.

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Table 3. **Pin description** *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144	Reset state [1]	Type	Description
USB0 _VDDA3V3	G3	F3	D2	17	-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	G3	D3	19	-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	F1	F2	23	-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	A6	B2	137	-	-	Analog power supply and ADC reference voltage.
VBAT	B10	B9	C5	127	-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	D8, E8	E4, E5, F4	94, 131, 59, 25		-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-	-	-	[12] -	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	H5, H10, K8, G10	F10, K5	5, 36, 41, 71, 77, 107, 111, 141	[12] -	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VDD	-	-	-	-			Power supply for main regulator, I/O, and OTP.
VSS	G9, H7, J10, J11, K8	F10, D7, E6, E7, E9, K6, K9	-	-	[13] [14] -	-	Ground.

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7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-CODE bus, and the D-code bus. The I-CODE and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC4350/30/20/10 use a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slaves ports of the matrix to be accessed simultaneously by different bus masters.

An ARM Cortex-M0 co-processor is included in the LPC4350/30/20/10, capable of off-loading the main ARM Cortex-M4 application processor. Most peripheral interrupts are connected to both processors. The processors communicate with each other via an interprocessor communication protocol.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 CPU incorporates a 3-stage pipeline, uses a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals, and includes an internal prefetch unit that supports speculative branching. The ARM Cortex-M4 supports single-cycle digital signal processing and SIMD instructions. A hardware floating-point processor is integrated in the core. The processor includes an NVIC with up to 53 interrupts.

7.3 ARM Cortex-M0 co-processor

The ARM Cortex-M0 is a general purpose, 32-bit microprocessor, which offers high performance and very low-power consumption. The ARM Cortex-M0 co-processor uses a 3-stage pipeline von-Neumann architecture and a small but powerful instruction set providing high-end processing hardware. In LPC43x0, the Cortex-M0 coprocessor hardware multiply is implemented as a 32-cycle iterative multiplier. The co-processor incorporates an NVIC with 32 interrupts.

7.4 Interprocessor communication

The ARM Cortex-M4 and ARM Cortex-M0 interprocessor communication is based on using shared SRAM as mailbox and one processor raising an interrupt on the other processor's NVIC, for example after it has delivered a new message in the mailbox. The receiving processor can reply by raising an interrupt on the sending processor's NVIC to acknowledge the message.

7.9.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.10 On-chip static RAM

The LPC4350/30/20/10 support up to 200 kB local SRAM and an additional 64 kB AHB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.11 In-System Programming (ISP)

In-System Programming (ISP) means programming or reprogramming the on-chip SRAM memory, using the boot loader software and the USART0 serial port. ISP can be performed when the part resides in the end-user board. ISP loads data into on-chip SRAM and execute code from on-chip SRAM.

7.12 Boot ROM

The internal ROM memory is used to store the boot code of the LPC4350/30/20/10. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from UART interfaces and external static memory such as NOR flash, quad SPI flash, and USB0 and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Several boot modes are available depending on the values of the OTP bits BOOT_SRC. If the OTP memory is not programmed or the BOOT_SRC bits are all zero, the boot mode is determined by the states of the boot pins P2_9, P2_8, P1_2, and P1_1.

Table 4.   Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
Pin state	0	0	0	0	Boot source is defined by the reset state of P1_1, P1_2, P2_8, and P2_9 pins. See Table 5.
USART0	0	0	0	1	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	0	0	1	0	Boot from Quad SPI flash connected to the SPIFI interface using pins P3_3 to P3_8.
EMC 8-bit	0	0	1	1	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.

Table 4. **Boot mode when OTP BOOT_SRC bits are programmed** *…continued*

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
   Remark: Pin functions for SPIFI and SSP0 boot are different.

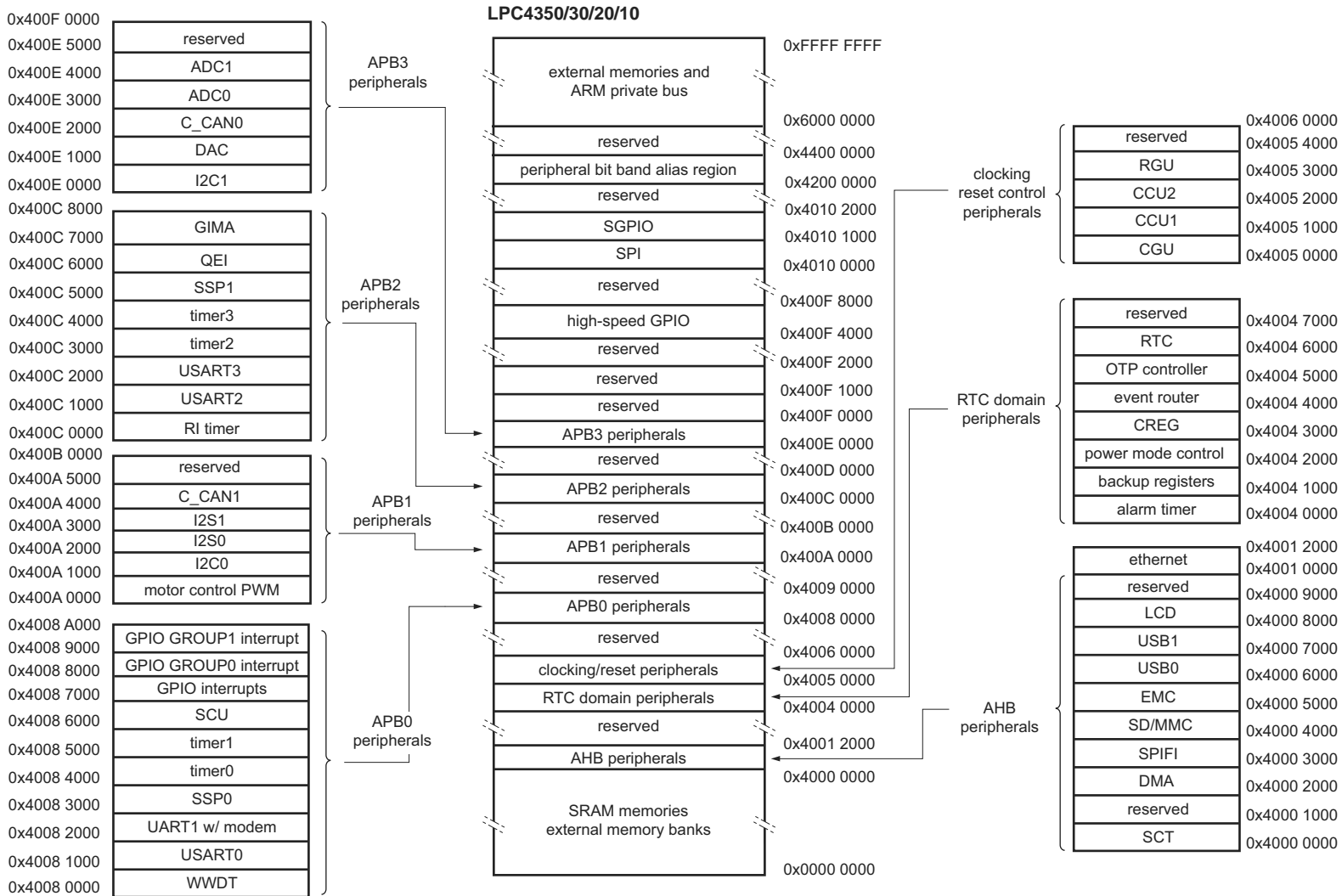**Table 5.** **Boot mode when OPT BOOT_SRC bits are zero**

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
   Remark: Pin functions for SPIFI and SSP0 boot are different.

7.13 Memory mapping

The memory map shown in Figure 7 and Figure 8 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

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APB3 peripherals:

Address	Block
0x400F 0000	
0x400E 5000	reserved
0x400E 4000	ADC1
0x400E 3000	ADC0
0x400E 2000	C_CAN0
0x400E 1000	DAC
0x400E 0000	I2C1

APB2 peripherals:

Address	Block
0x400C 8000	
0x400C 7000	GIMA
0x400C 6000	QEI
0x400C 5000	SSP1
0x400C 4000	timer3
0x400C 3000	timer2
0x400C 2000	USART3
0x400C 1000	USART2
0x400C 0000	RI timer

APB1 peripherals:

Address	Block
0x400B 0000	
0x400A 5000	reserved
0x400A 4000	C_CAN1
0x400A 3000	I2S1
0x400A 2000	I2S0
0x400A 1000	I2C0
0x400A 0000	motor control PWM

APB0 peripherals:

Address	Block
0x4008 A000	
0x4008 9000	GPIO GROUP1 interrupt
0x4008 8000	GPIO GROUP0 interrupt
0x4008 7000	GPIO interrupts
0x4008 6000	SCU
0x4008 5000	timer1
0x4008 4000	timer0
0x4008 3000	SSP0
0x4008 2000	UART1 w/ modem
0x4008 1000	USART0
0x4008 0000	WWDT

Main memory map:

Address	Block
0xFFFF FFFF	external memories and ARM private bus
0x6000 0000	reserved
0x4400 0000	peripheral bit band alias region
0x4200 0000	reserved
0x4010 2000	SGPIO
0x4010 1000	SPI
0x4010 0000	reserved
0x400F 8000	high-speed GPIO
0x400F 4000	reserved
0x400F 2000	reserved
0x400F 1000	reserved
0x400F 0000	APB3 peripherals
0x400E 0000	reserved
0x400D 0000	APB2 peripherals
0x400C 0000	reserved
0x400B 0000	APB1 peripherals
0x400A 0000	reserved
0x4009 0000	APB0 peripherals
0x4008 0000	reserved
0x4006 0000	clocking/reset peripherals
0x4005 0000	RTC domain peripherals
0x4004 0000	reserved
0x4001 2000	AHB peripherals
0x4000 0000	SRAM memories external memory banks
0x0000 0000	

clocking reset control peripherals:

Address	Block
0x4006 0000	reserved
0x4005 4000	RGU
0x4005 3000	CCU2
0x4005 2000	CCU1
0x4005 1000	CGU
0x4005 0000	

RTC domain peripherals:

Address	Block
0x4004 7000	reserved
0x4004 6000	RTC
0x4004 5000	OTP controller
0x4004 4000	event router
0x4004 3000	CREG
0x4004 2000	power mode control
0x4004 1000	backup registers
0x4004 0000	alarm timer

AHB peripherals:

Address	Block
0x4001 2000	ethernet
0x4001 0000	reserved
0x4000 9000	LCD
0x4000 8000	USB1
0x4000 7000	USB0
0x4000 6000	EMC
0x4000 5000	SD/MMC
0x4000 4000	SPIFI
0x4000 3000	DMA
0x4000 2000	reserved
0x4000 1000	SCT
0x4000 0000	

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Fig 8.   LPC4350/30/20/10 Memory mapping (peripherals)

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.16.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Counters can be configured as up-counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - up to 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

7.16.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.16.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.
- Each slice has a 32-bit pattern match filter.

- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.17.8 Ethernet

Remark: The Ethernet peripheral is available on parts LPC4350/30. See Table 2.

7.17.8.1 Features

- 10/100 Mbit/s.

- DMA support.

- Power management remote wake-up frame and magic packet detection.

- Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation.
    - Supports IEEE 802.3x flow control for full-duplex operation.
    - Optional forwarding of received pause control frames to the user application in full-duplex operation.
    - Back-pressure support for half-duplex operation.
    - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.

- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.18 Digital serial peripherals

7.18.1 UART1

The LPC4350/30/20/10 contain one UART with standard transmit and receive data lines. UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.18.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.

- 16 B Receive and Transmit FIFOs.

- Register locations conform to 16C550 industry standard.

- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.

- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.

- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.

- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.

- Support for RS-485/9-bit/EIA-485 mode (UART1).

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- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.

- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.20 Analog peripherals

7.20.1 Analog-to-Digital Converter (ADC0/1)

7.20.1.1 Features

- 10-bit successive approximation analog to digital converter.

- Input multiplexing among 8 pins.

- Power-down mode.

- Measurement range 0 to VDDA.

- Sampling frequency up to 400 kSamples/s.

- Burst conversion mode for single or multiple inputs.

- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.

- Individual result registers for each A/D channel to reduce interrupt overhead.

- DMA support.

7.20.2 Digital-to-Analog Converter (DAC)

7.20.2.1 Features

- 10-bit resolution.

- Monotonic by design (resistor string architecture).

- Controllable conversion speed.

- Low-power consumption.

7.21 Peripherals in the RTC power domain

7.21.1 RTC

The Real-Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.21.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.

- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.

- Dedicated battery power supply pin.

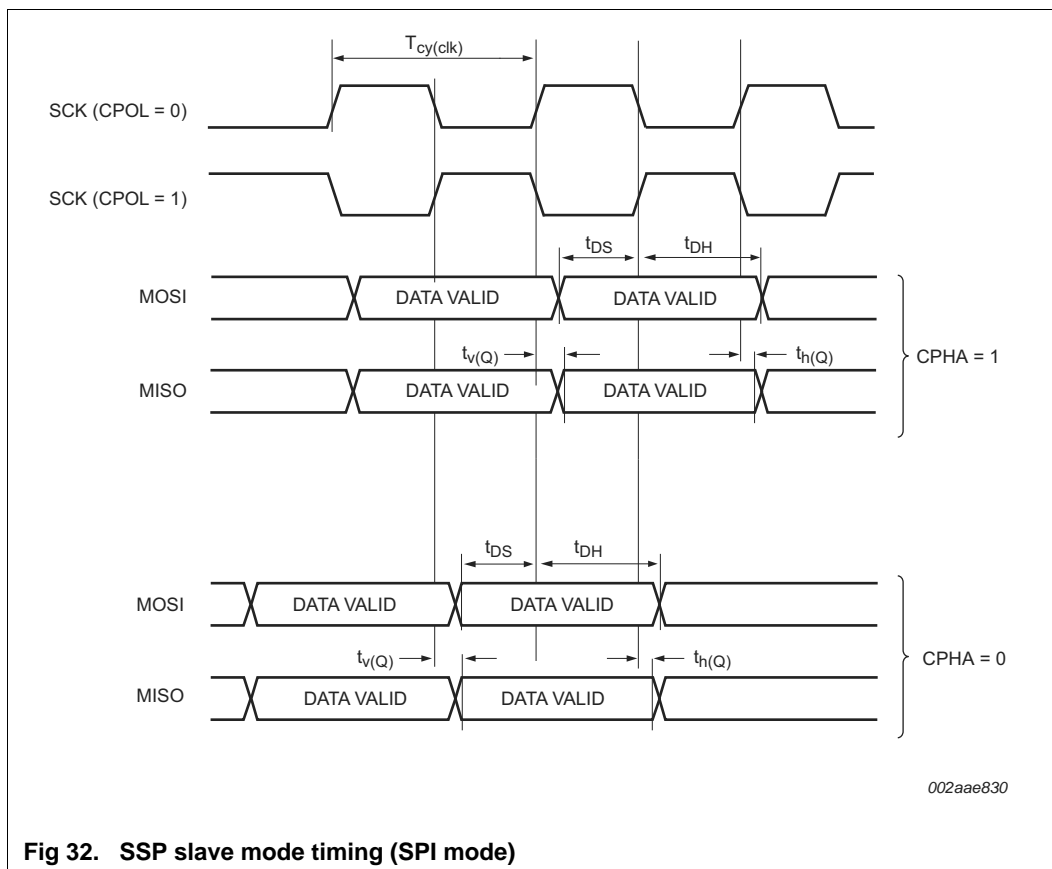- RTC power supply is isolated from the rest of the chip.

Fig 32. SSP slave mode timing (SPI mode)

11.14 SGPIO timing

The following considerations apply to SGPIO timing:

- SGPIO input signals are synchronized by the internal clock SGPIO_CLOCK. To guarantee that no samples are missed, all input signals should have a duration of at least one SGPIO_CLOCK cycle plus the set-up and hold times.

- When an external clock input is used to generate output data, synchronization causes a latency of at least one SGPIO_CLOCK cycle. The maximum output data rate is one output every two SGPIO_CLOCK cycles.

- Synchronization also causes a latency of one SGPIO_CLOCK cycle when sampling several inputs. This may cause inputs with very similar timings to be sampled with a difference of one SGPIO_CLOCK cycle.

Table 28.   Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{EMC\_DYCSn}$, $\overline{EMC\_RAS}$, $\overline{EMC\_CAS}$, $\overline{EMC\_WE}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ =3.3 V ± 10 %; RD = 1 (see LPC43xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	DYCS delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.1 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(DYCS)}$	DYCS hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$4.9 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	$0.5 + 0.5 \times T_{cy(clk)}$	$1.1 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	$2.9 + 0.5 \times T_{cy(clk)}$	$4.6 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	$\overline{WE}$ valid delay time	-	$3.2 + 0.5 \times T_{cy(clk)}$	$5.9 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(WE)}$	$\overline{WE}$ hold time	$1.3 + 0.5 \times T_{cy(clk)}$	$1.4 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.0 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	$0.2 + 0.5 \times T_{cy(clk)}$	$0.8 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	$3.8 + 0.5 \times T_{cy(clk)}$	$6.3 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	$0.3 + 0.5 \times T_{cy(clk)}$	$0.9 + 0.5 \times T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	$3.1 + 0.5 \times T_{cy(clk)}$	$5.1 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	$0.5 \times T_{cy(clk)}$	$0.7 + 0.5 \times T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	$3.8 + 0.5 \times T_{cy(clk)}$	$6.2 + 0.5 \times T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	$0.5 \times T_{cy(clk)}$	$0.7 + 0.5 \times T_{cy(clk)}$	-	ns

Table 29.   Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 85 °C; $V_{DD(IO)}$ =3.3 V ± 10 %; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1]   Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.

11.16 USB interface

Table 30. Dynamic characteristics: USB0 and USB1 pins (full-speed)
$C_L = 50\ pF$; $R_{pu} = 1.5\ k\Omega$ on D+ to $V_{DD(IO)}$; $3.0\ V \leq V_{DD(IO)} \leq 3.6\ V$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4	-	20	ns
t_f	fall time	10 % to 90 %		4	-	20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90	-	111.11	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 37		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 37		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 37	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 37	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Remark: If only USB0 (HS USB) is used, the pins VDDREG and VDDIO can be at different voltages within the operating range but should have the same ramp up time. If USB1(FS USB) is used, the pins VDDREG and VDDIO should be a minimum of 3.0 V and be tied together.
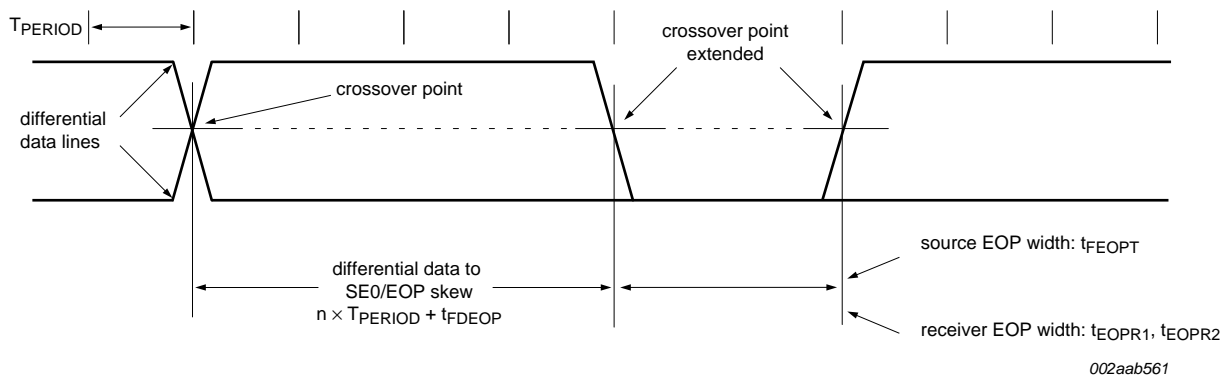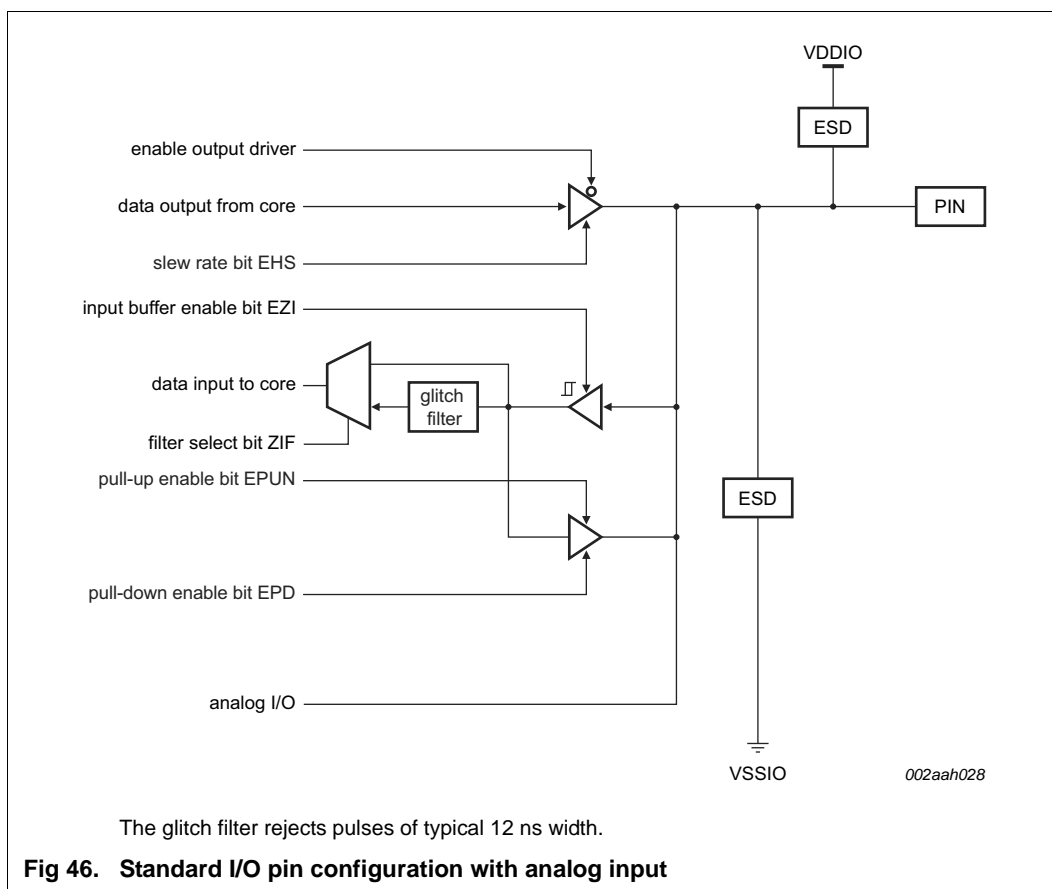

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Fig 37. Differential data-to-EOP transition skew and EOP width

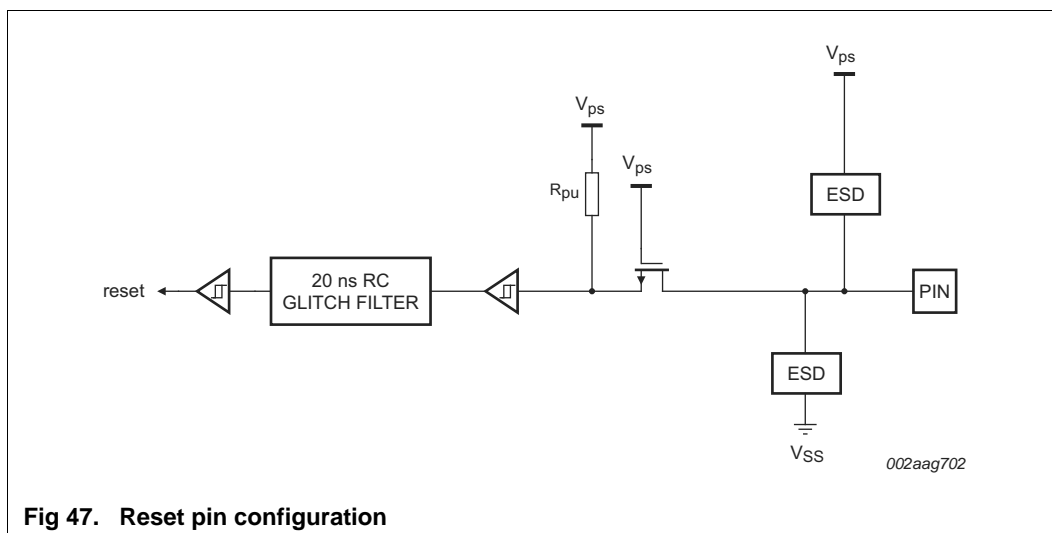**Table 39.   LCD panel connections for STN dual panel mode** …continued

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 40.   LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4	PB_0	BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3	PB_1	BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2	PB_2	BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1	PB_3	BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0	P7_1	BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity	P7_2	BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

The glitch filter rejects pulses of typical 12 ns width.

Fig 46. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

Fig 47. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 48) or bus-powered device (see Figure 49).

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