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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	264K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4330fet100-551

6. Pinning information

6.1 Pinning

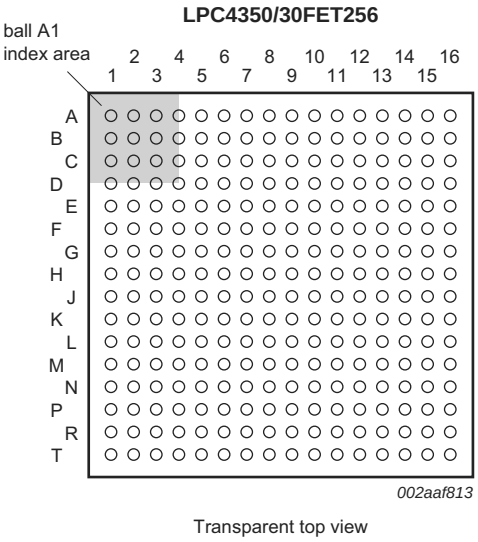


Fig 2. Pin configuration LBGA256 package

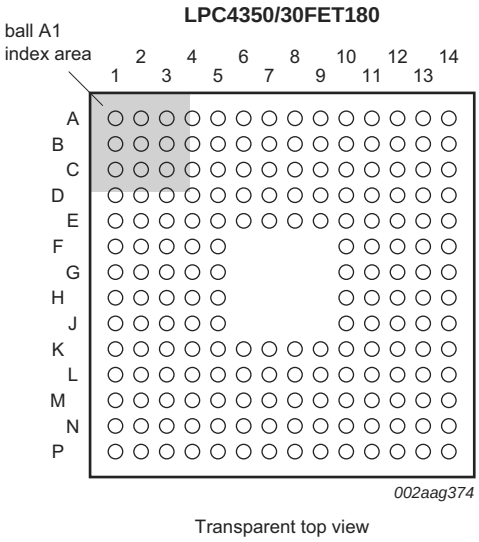


Fig 3. Pin configuration TFBGA180 package

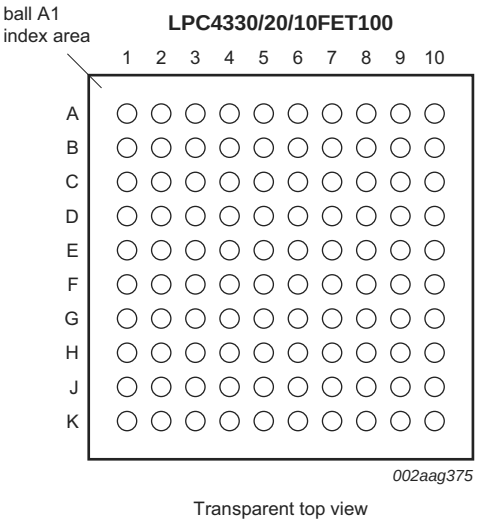


Fig 4. Pin configuration TFBGA100 package

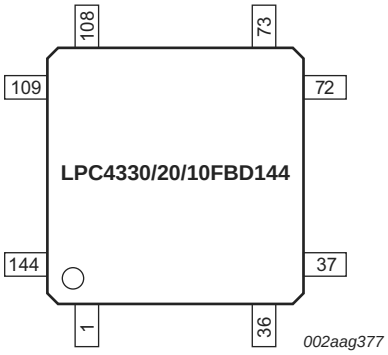


Fig 5. Pin configuration LQFP144 package

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P2_8	J16	H14	C6	98	[2]	N; PU	I/O	**SGPIO15 —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_9	H16	G14	B10	102	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	F14	E8	104	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	E13	A9	105	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P4_2	D3	A2	-	8	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							O	**LCD_VD3 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	B2	-	7	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							AI	**ADC0_0 —** DAC output; ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_4	B1	A1	-	9	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**LCD_VD1 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD20 —** LCD data.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							O	**DAC —** DAC output. Shared between 10-bit ADC0/1 and DAC.. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P5_6	T13	M11	-	63	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I/O	**EMC_D10 —** External memory data line 10.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							O	**T1_MAT2 —** Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_7	R12	N11	-	65	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
							O	**MCOA2 —** Motor control PWM channel 2, output A.
							I/O	**EMC_D11 —** External memory data line 11.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							O	**T1_MAT3 —** Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_0	M12	M10	H7	73	[2]	N; PU	-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_1	R15	P14	G5	74	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
							O	**EMC_DYCS1 —** SDRAM chip select 1.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P6_9	J15	H13	F8	97	[2]	N; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_DYCS0 —** SDRAM chip select 0.
							-	**R —** Function reserved.
							O	**T2_MAT2 —** Match output 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_10	H15	G13	-	100	[2]	N; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
							O	**MCABORT —** Motor control PWM, LOW-active fast abort.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_11	H12	F11	C9	101	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
							-	**R —** Function reserved.
							O	**T2_MAT3 —** Match output 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_12	G15	F13	-	103	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_4	C8	C6	-	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	A7	-	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	-	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_11	L5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[11] —** General purpose digital input/output pin.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[12] —** General purpose digital input/output pin.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SD_DAT6 —** SD/MMC data bus line 6.
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[13] —** General purpose digital input/output pin.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_DAT7 —** SD/MMC data bus line 7.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_0	N2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_15 —** SCTimer/PWM output 15. Match output 3 of timer 3.
							O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
							-	**R —** Function reserved.
							I/O	**GPIO6[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1	P1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[15] —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
							-	**R —** Function reserved.
							I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2	R1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							I/O	**EMC_D16 —** External memory data line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO6 —** General purpose digital input/output pin.
PD_3	P4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_6 —** SCTimer/PWM output 7. Match output 2 of timer 1.
							I/O	**EMC_D17 —** External memory data line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO7 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_7	F15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**EMC_D26 —** External memory data line 26.
							I/O	**GPIO7[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_8	F14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_4 —** SCTimer/PWM output 4. Match output 3 of timer 3.
							I	**U1_DSR —** Data Set Ready input for UART 1.
							I/O	**EMC_D27 —** External memory data line 27.
							I/O	**GPIO7[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_9	E16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_4 —** SCTimer/PWM input 4. Capture input 2 of timer 1.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							I/O	**EMC_D28 —** External memory data line 28.
							I/O	**GPIO7[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_10	E14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_3 —** SCTimer/PWM input 3. Capture input 1 of timer 1.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I/O	**EMC_D29 —** External memory data line 29.
							I/O	**GPIO7[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
USB0_VDDA3V3	G3	F3	D2	17		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA_TERM	H3	G3	D3	19		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA_REF	G1	F1	F2	23		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	A6	B2	137		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	B9	C5	127		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	D8, E8	E4, E5, F4	94, 131, 59, 25			-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-	-	-	[12]	-	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	H5, H10, K8, G10	F10, K5	5, 36, 41, 71, 77, 107, 111, 141	[12]	-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VDD	-	-	-	-				Power supply for main regulator, I/O, and OTP.
VSS	G9, H7, J10, J11, K8	F10, D7, E6, E7, E9, K6, K9	-	-	[13] [14]	-	-	Ground.

- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.17.8 Ethernet

Remark: The Ethernet peripheral is available on parts LPC4350/30. See Table 2.

7.17.8.1 Features

- 10/100 Mbit/s.
- DMA support.
- Power management remote wake-up frame and magic packet detection.
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.18 Digital serial peripherals

7.18.1 UART1

The LPC4350/30/20/10 contain one UART with standard transmit and receive data lines. UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.18.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.
- Support for RS-485/9-bit/EIA-485 mode (UART1).

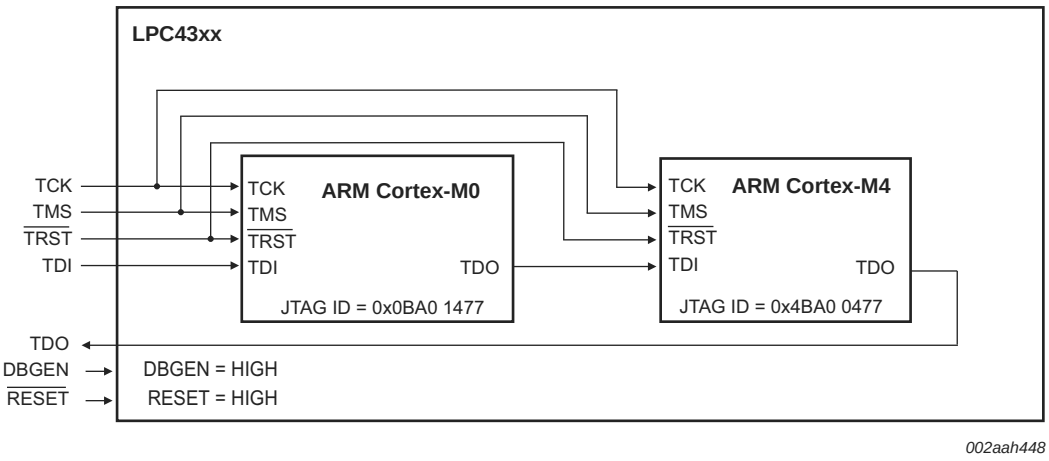


Fig 10. Dual-core debug configuration

[5] PLL1 disabled; IRC running; CCLK = 12 MHz.

[6] V_{BAT} = 3.6 V.

[7] $V_{DD(IO)} = V_{DDA}$ = 3.6 V; over entire frequency range CCLK = 12 MHz to 180 MHz.

[8] On pin VBAT; T_{amb} = 25 °C.

[9] $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V. Input leakage increases when $V_{DD(IO)}$ is floating or grounded. It is recommended to keep $V_{DD(REG)(3V3)}$ and $V_{DD(IO)}$ powered in deep power-down mode.

[10] V_{ps} corresponds to the output of the power switch (see Figure 9) which is determined by the greater of V_{BAT} and $V_{DD(Reg)(3V3)}$.

[11] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[12] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[13] To V_{SS}.

[14] The values specified are simulated and absolute values.

[15] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

[16] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

[17] The parameter value specified is a simulated value excluding bond capacitance.

[18] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[19] $V_{DD(IO)}$ present.

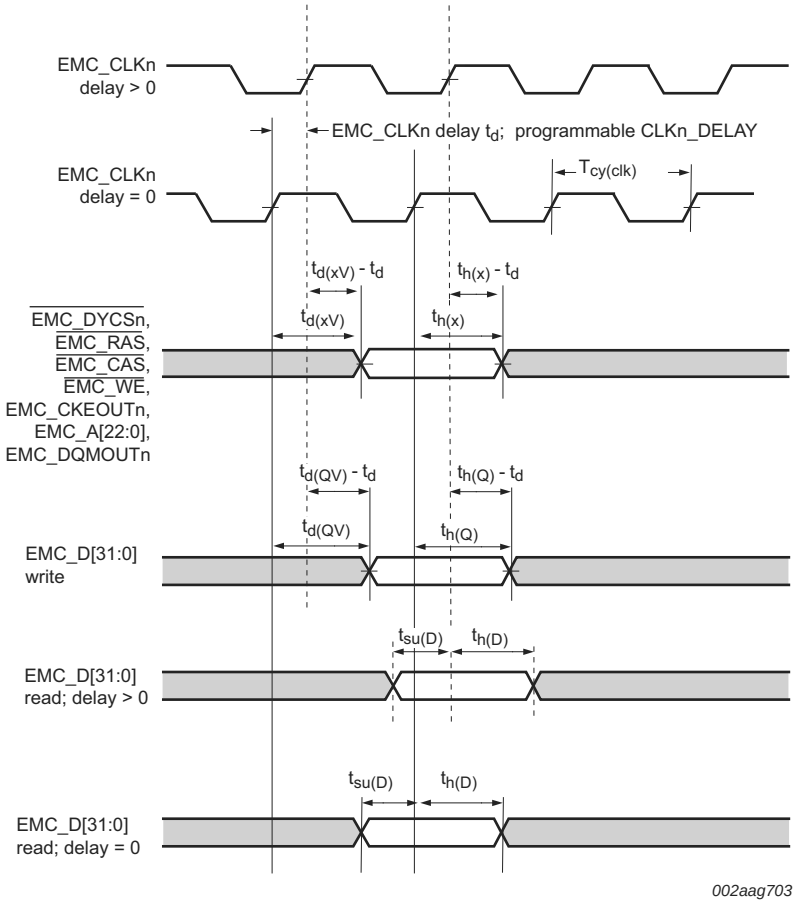
[20] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

11.15 External memory interface

Table 27. Dynamic characteristics: Static asynchronous external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

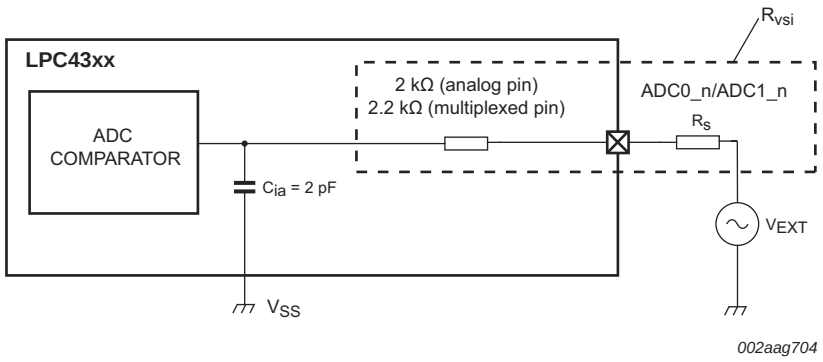
Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time			-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time			−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time			−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1		−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time		[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time		[4]	0	-	1.8	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time			−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1		−1.5 + (WAITWEN + 1) × $T_{cy(clk)}$	-	0.2 + (WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1	[2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1	[2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1	[2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0		−0.7 + (WAITWEN + 1) × $T_{cy(clk)}$	-	1.8 + (WAITWEN + 1) × $T_{cy(clk)}$	ns



For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 29.

Remark: For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

Fig 36. SDRAM timing



$Rs < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 42. ADC interface to pins

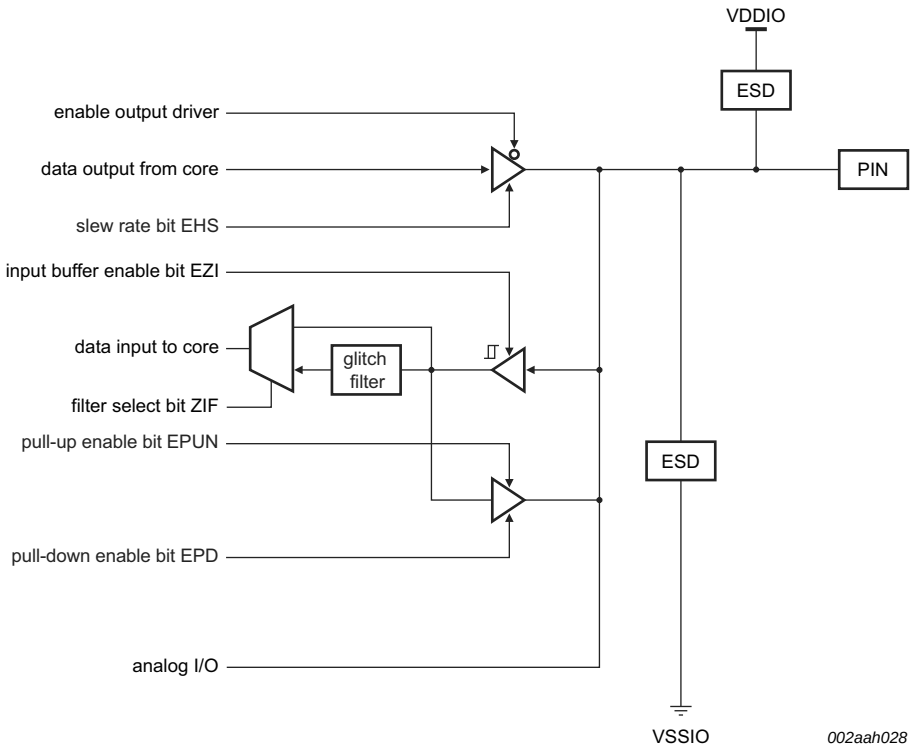
Table 37. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±1.0	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.8	-	LSB
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1]	-	±0.3	-	%
		2.2 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[2]		0.4		μσ

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.



The glitch filter rejects pulses of typical 12 ns width.

Fig 46. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

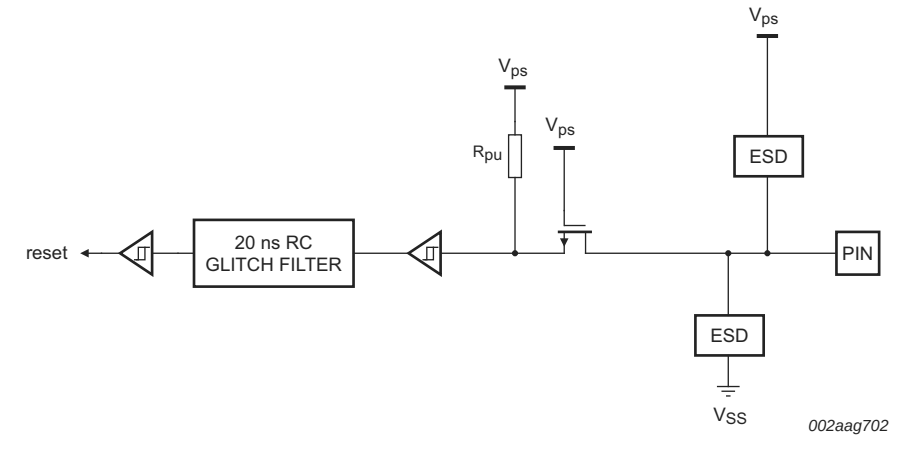


Fig 47. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 48) or bus-powered device (see Figure 49).

Table 44. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Parameter C_I corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 10. • Table 19 “Dynamic characteristic: I/O pins[1]” added. • IRC accuracy changed from 1 % to 1.5 % over the full temperature range. See Table 17 “Dynamic characteristic: IRC oscillator”. • Description of internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins.See Table 3. • Description of DEBUG pin updated. • Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.22.7 “System PLL1”. • Section 13.7 “Suggested USB interface solutions” added. • SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 “SSP master mode timing (SPI mode)”. • Parameters t_{lead}, t_{lag}, and t_d added in Table 23 “Dynamic characteristics: SSP pins in SPI mode”. • Reset state of the RTC alarm pin RTC_ALARM added. See Table 3. • SRAM location for parts LPC4320 corrected in Figure 7. • IEEE standard 802.3 compliance added to Section 11.16. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals.\ • Signal polarity of EMC_CKEOUT and EMC_DQMOUT corrected. Both signals are active HIGH. • • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 26 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 26 “Dynamic characteristics: Static asynchronous external memory interface”.			
LPC4350_30_20_10 v.4.1	20131211	Product data sheet	-	LPC4350_30_20_10 v.4
Modifications:	• Description of $\overline{\text{RESET}}$ pin updated in Table 3. • Layout of local SRAM at address 0x1008 0000 clarified in Figure 7 “LPC4350/30/20/10 Memory mapping (overview)”. • Maximum value for $V_{i(RMS)}$ added in Section 13.3 “RTC oscillator”. • V_O for RTC_ALARM pin added in Table 10. • RTC_ALARM and WAKEUPn pins added to Table 10. • Table note 9 added in Table 10. • Timing parameters in Table 31 “Dynamic characteristics: SD/MMC” corrected. • Band gap characteristics removed. • OTP memory size available for general purpose use corrected. • Part LPC4350FBD208 removed.			
LPC4350_30_20_10 v.4	20130326	Product data sheet	-	LPC4350_30_20_10 v.3.7

Table 44. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Temperature range for simulated timing characteristics corrected to T_{amb} = −40 °C to +85 °C in Section 11 “Dynamic characteristics”. • SPIFI timing added. See Section 11.15. • SPIFI maximum data rate changed to 52 MB per second. • Editorial updates. • Figure 25 and Figure 26 updated for full temperature range. • Section 7.23 “Serial Wire Debug/JTAG” updated. • The following changes were made on the TFBGA180 pinout in Table 3: – P1_13 moved from ball D6 to L8. – P7_5 moved from ball C7 to A7. – PF_4 moved from ball L8 to D6. – $\overline{\text{RESET}}$ moved from ball B7 to C7. – RTCX2 moved from ball A7 to B7. – Ball G10 changed from VSS to VDDIO.			
LPC4350_30_20_10 v.3.4	20120904	Preliminary data sheet	-	LPC4350_30_20_10 v.3.3
Modifications:	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • Minimum value for all supply voltages changed to -0.5 V in Table 6.			
LPC4350_30_20_10 v.3.3	20120821	Preliminary data sheet	-	LPC4350_30_20_10 v.3.2
Modifications:	• Parameter t_{wake} updated in Table 13 for wake-up from deep power-down mode and reset. • Dynamic characteristics of the SD/MMC controller updated in Table 28. • Dynamic characteristics of the LCD controller updated in Table 29. • Dynamic characteristics of the SSP controller updated in Table 21. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”,“USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10. • AES removed. AES is available on parts LPC43Sxx only. • Pin configuration diagrams corrected for LQFP packages (Figure 5 and Figure 6). • Figure 10 updated. • All power consumption data updated in Table 10 and Section 10.1 “Power consumption”. • BOD levels updated in Table 12. • SWD debug option removed for Cortex-M0 core.			
LPC4350_30_20_10 v.3.2	20120604	Preliminary data sheet	-	LPC4350_30_20_10 v.3.1
LPC4350_30_20_10 v.3.1	20120105	Objective data sheet	-	LPC4350_30_20_10 v.3
LPC4350_30_20_10 v.3	20111205	Objective data sheet	-	LPC4350_30_20_10 v.2.1
LPC4350_30_20_10 v.2.1	20110923	Objective data sheet	-	LPC4350_30_20_10 v.2
LPC4350_30_20_10 v.2	20110714	Objective data sheet	-	LPC4350_30_20_10 v.1
LPC4350_30_20_10 v.1	20101029	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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