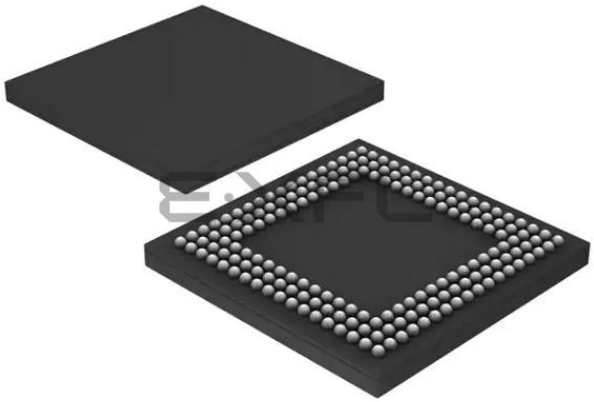

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	118
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	264K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4330fet180-551

- One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
- One standard I^2C-bus interface with monitor mode and with standard I/O pins.
- Two I^2S interfaces, each with DMA support and with one input and one output.

- Digital peripherals
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024 H $\times$ 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - Secure Digital Input Output (SD/MMC) card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
  - Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control Pulse Width Modulator (PWM) for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer (WWDT).
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.
- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P7_4	C8	C6	-	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	A7	-	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCTimer/PWM output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_6	C7	F5	-	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCTimer/PWM output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PB_2	B12	B11	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							O	**LCD_VD21 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[22] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_3	A13	A12	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
							O	**LCD_VD20 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[23] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_4	B11	B10	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[24] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_5	A12	A11	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[25] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PF_3	E10	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							I/O	**GPIO7[18] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
PF_4	D10	D6	H4	120	[2]	O; PU	I/O	**SSP1_SCK —** Serial clock for SSP1.
							I	**GP_CLKIN —** General-purpose clock input to the CGU.
							O	**TRACECLK —** Trace clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S0_RX_SCK —** I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
PF_5	E9	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							I/O	**GPIO7[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							AI	**ADC1_4 —** ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PF_9	D6	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							O	**CTOUT_1 —** SCTimer/PWM output 1. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**GPIO7[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**SD_WP —** SD/MMC card write protect input.
							-	**R —** Function reserved.
							AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[25] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							-	**R —** Function reserved.
							AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed *…continued*

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

7.13 Memory mapping

The memory map shown in Figure 7 and Figure 8 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

7.14 One-Time Programmable (OTP) memory

The OTP provides 64 bit + 256 bit One-Time Programmable (OTP) memory for general-purpose use.

7.15 General-Purpose I/O (GPIO)

The LPC4350/30/20/10 provide eight GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.15.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request (GPIO interrupts).
- Two GPIO group interrupts can be triggered by any pin or pins in each port (GPIO group0 and group1 interrupts).

7.16 Configurable digital peripherals

7.16.1 State Configurable Timer (SCTimer/PWM) subsystem

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.16.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Counters can be configured as up-counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs and interrupts.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - up to 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states

7.16.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.16.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.
- Each slice has a 32-bit pattern match filter.

- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.17.7 LCD controller

Remark: The LCD controller is available on LPC4350 only. See Table 2.

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.17.7.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.

- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position-compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.19.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.19.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.19.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.19.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

7.22.4 Internal RC oscillator (IRC)

The IRC is used as the clock source for the WWDT and/or as the clock that drives the PLLs and the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1.5 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC4350/30/20/10 use the IRC as the clock source. The boot loader then configures the PLL1 to provide a 96 MHz clock for the core and the PLL0USB or PLL0AUDIO as needed if an external boot source is selected.

7.22.5 PLL0USB (for USB0)

PLL0 is a dedicated PLL for the USB0 High-speed controller.

PLL0 accepts an input clock frequency from an external oscillator in the range of 14 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The CCO operates in the range of 4.3 MHz to 550 MHz.

7.22.6 PLL0AUDIO (for audio)

The audio PLL PLL0AUDIO is a general-purpose PLL with a small step size. This PLL accepts an input clock frequency derived from an external oscillator or internal IRC. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). A sigma-delta converter modulates the PLL divider ratios to obtain the desired output frequency. The output frequency can be set as a multiple of the sampling frequency f_s to $32 \times f_s$, $64 \times f_s$, $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, $512 \times f_s$ and the sampling frequency f_s can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96,192) kHz. Many other frequencies are possible as well using the integrated fractional divider.

7.22.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.22.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC4350/30/20/10.

7.22.9 Power control

The LPC4350/30/20/10 feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

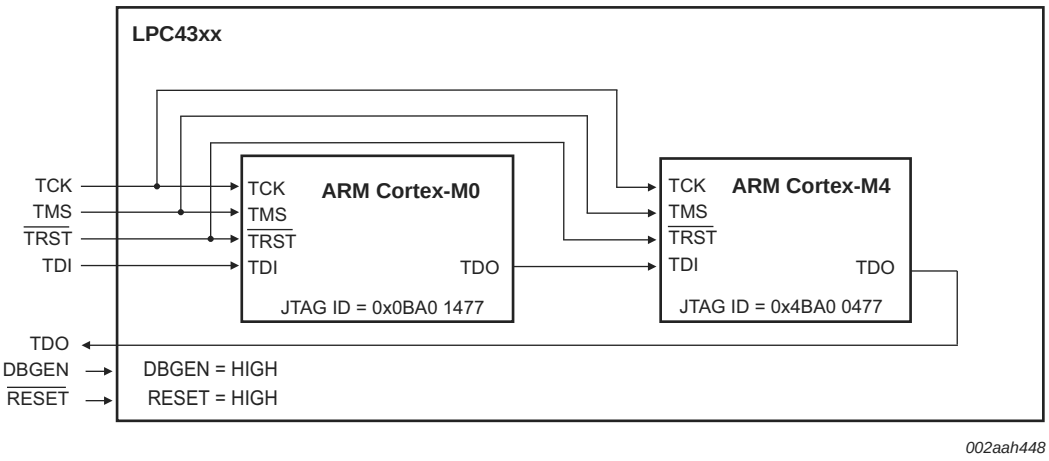
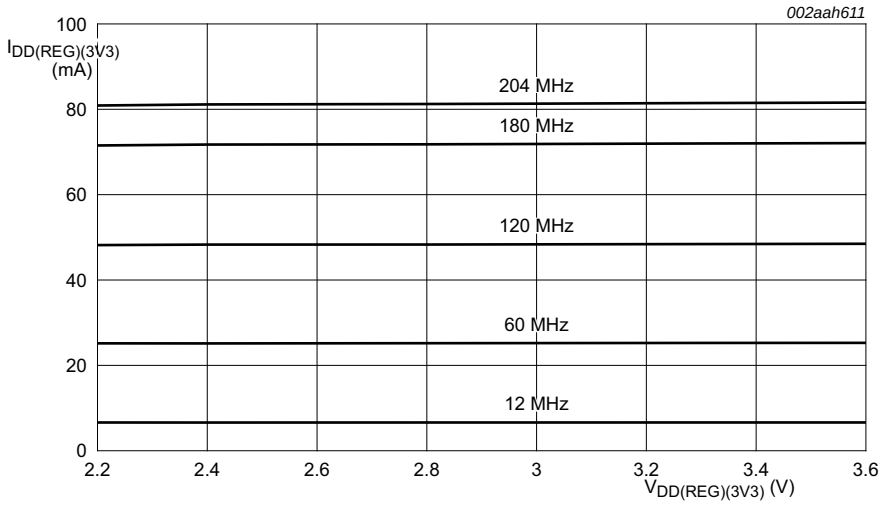


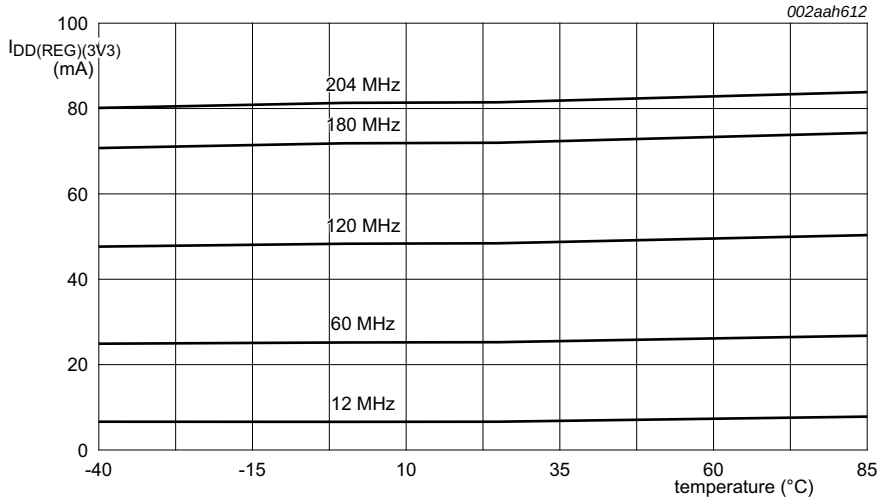
Fig 10. Dual-core debug configuration

10.1 Power consumption



Conditions: T_{amb} = 25 °C; active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V, Active mode entered executing code while(1){} from SRAM; M0-core in reset; internal pull-up resistors disabled; PLL1 enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus temperature in Active mode

Table 11. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
LCD	CLK_M4_LCD	0.85	1.72
ETHERNET	CLK_M4_ETHERNET	1.05	2.09
UART0	CLK_M4_UART0, CLK_APB0_UART0	0.3	0.38
UART1	CLK_M4_UART1, CLK_APB0_UART1	0.27	0.48
UART2	CLK_M4_UART2, CLK_APB2_UART2	0.27	0.47
UART3	CLK_M4_USART3, CLK_APB2_UART3	0.29	0.49
TIMER0	CLK_M4_TIMER0	0.07	0.14
TIMER1	CLK_M4_TIMER1	0.07	0.14
TIMER2	CLK_M4_TIMER2	0.07	0.15
TIMER3	CLK_M4_TIMER3	0.06	0.11
SDIO	CLK_M4_SDIO, CLK_SDIO	0.79	1.37
SCTimer/PWM	CLK_M4_SCT	0.52	1.05
SSP0	CLK_M4_SSP0, CLK_APB0_SSP0	0.12	0.21
SSP1	CLK_M4_SSP1, CLK_APB2_SSP1	0.15	0.28
DMA	CLK_M4_DMA	1.88	3.71
WWDT	CLK_M4_WWDT	0.05	0.08
QEI	CLK_M4_QEI	0.33	0.68
USB0	CLK_M4_USB0, CLK_USB0	1.46	3.32
USB1	CLK_M4_USB1, CLK_USB1	2.83	5.03
RITIMER	CLK_M4_RITIMER	0.04	0.08
EMC	CLK_M4_EMC, CLK_M4_EMC_DIV	3.6	6.97
SCU	CLK_M4_SCU	0.09	0.23
CREG	CLK_M4_CREG	0.37	0.72
SGPIO	CLK_PERIPH_SGPIO	0.1	0.17
SPI	CLK_SPI	0.07	0.11

11. Dynamic characteristics

11.1 Wake-up times

Table 14. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	3 × $T_{cy(clk)}$	5 × $T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	250	-	µs
		after reset		-	250	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.2 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 10). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 15. Dynamic characteristic: external clock

T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Max	Unit
f_{osc}	oscillator frequency			1	25	MHz
$T_{cy(clk)}$	clock cycle time			40	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)}$ × 0.4	$T_{cy(clk)}$ × 0.6	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)}$ × 0.4	$T_{cy(clk)}$ × 0.6	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

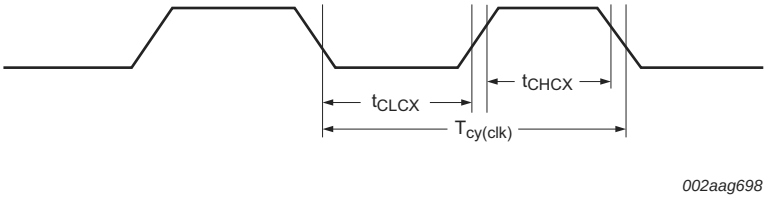


Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

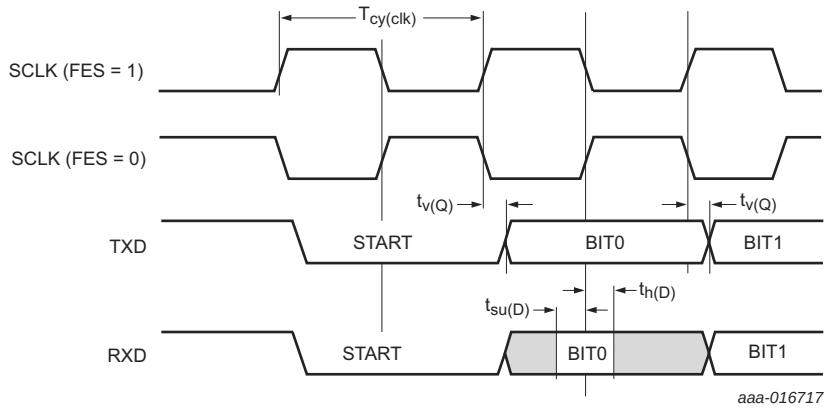


Fig 30. USART timing

Table 26. Dynamic characteristics: SGPIO

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D)}$	data input set-up time			2	-	-	ns
$t_{h(D)}$	data input hold time		[1]	T_{SGPIO} + 2	-	-	ns
$t_{su(D)}$	data input set-up time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{h(D)}$	data input hold time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{v(Q)}$	data output valid time		[1]	-	-	2 × T_{SGPIO}	ns
$t_{h(Q)}$	data output hold time		[1]	T_{SGPIO}	-		ns
$t_{v(Q)}$	data output valid time	sampled by SGPIO_CLOCK	[1]	−3	-	3	ns
$t_{h(Q)}$	data output hold time	sampled by SGPIO_CLOCK	[1]	−3	-	3	ns

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO\_CLOCK}$.

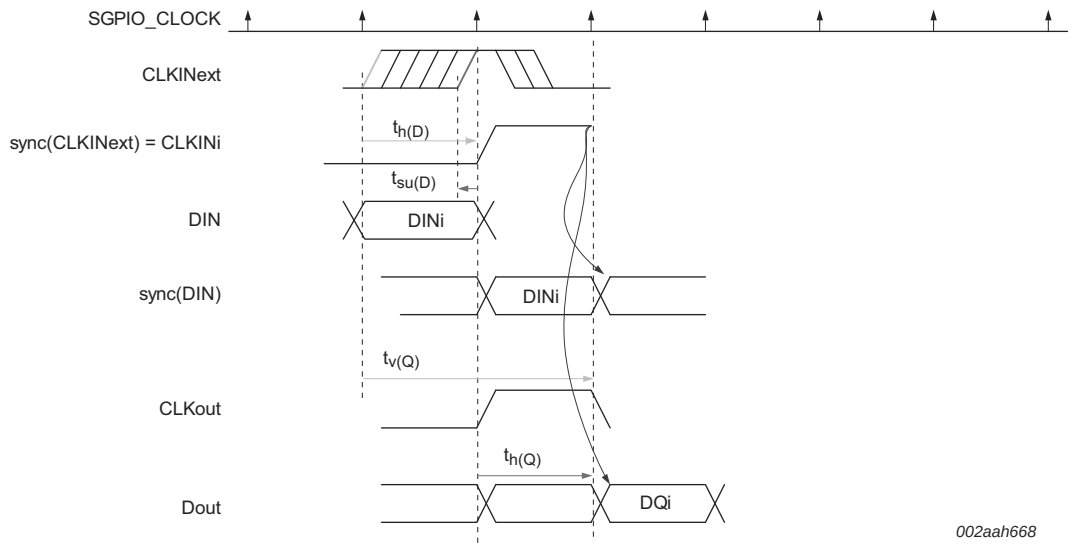


Fig 33. SGPIO timing

Table 27. Dynamic characteristics: Static asynchronous external memory interface *…continued*

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted resulting in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 0	[2]	−0.9 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	PB = 0	[2] [5]	−1.9 + $T_{cy(clk)}$	-	−0.5 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 0	[1] [2]	−2.5 + $T_{cy(clk)}$	-	1.4 + $T_{cy(clk)}$	ns
t_{CSHEOW}	$\overline{CS}$ HIGH to end of write time		[5]	−2.0	-	0	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		−2.5	-	1.4	ns
t_{WEHANV}	WE HIGH to address invalid time	PB = 1		−0.9 + $T_{cy(clk)}$	-	2.4 + $T_{cy(clk)}$	ns

[1] Parameters specified for 40 % of $V_{DD(IO)}$ for rising edges and 60 % of $V_{DD(IO)}$ for falling edges.

[2] $T_{cy(clk)}$ = 1/CCLK (see LPC43xx User manual).

[3] End Of Read (EOR): longest of t_{CSHOEH}, t_{OEHANV}, $t_{CSHBLSH}$.

[4] Start Of Read (SOR): longest of t_{CSLAV}, t_{CSLOEL}, $t_{CSLBLSL}$.

[5] End Of Write (EOW): earliest of address not valid or $\overline{EMC\_BLSn}$ HIGH.

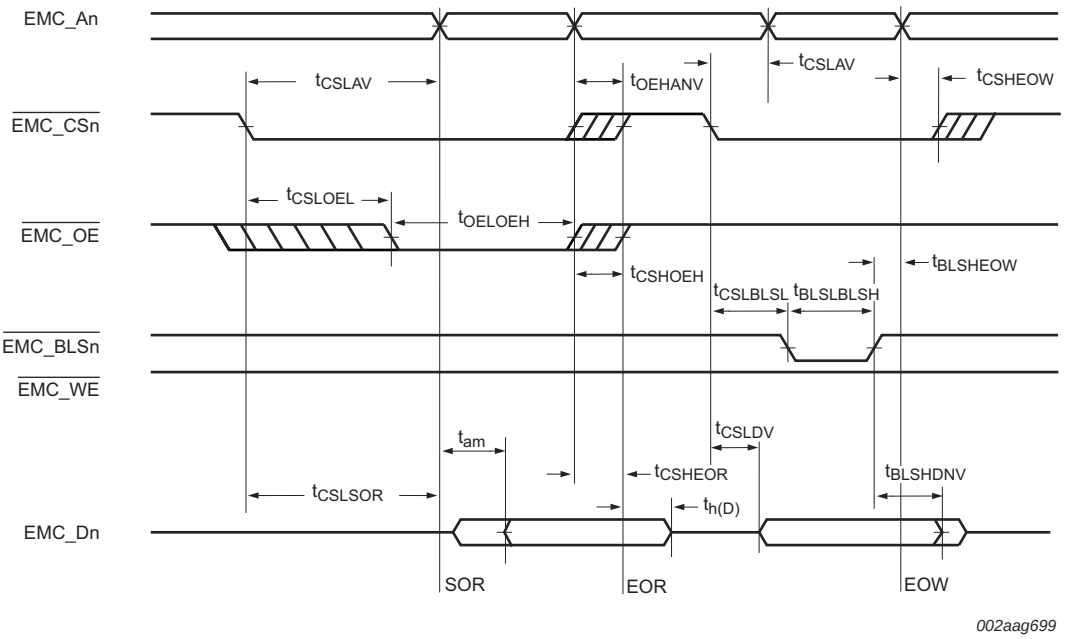
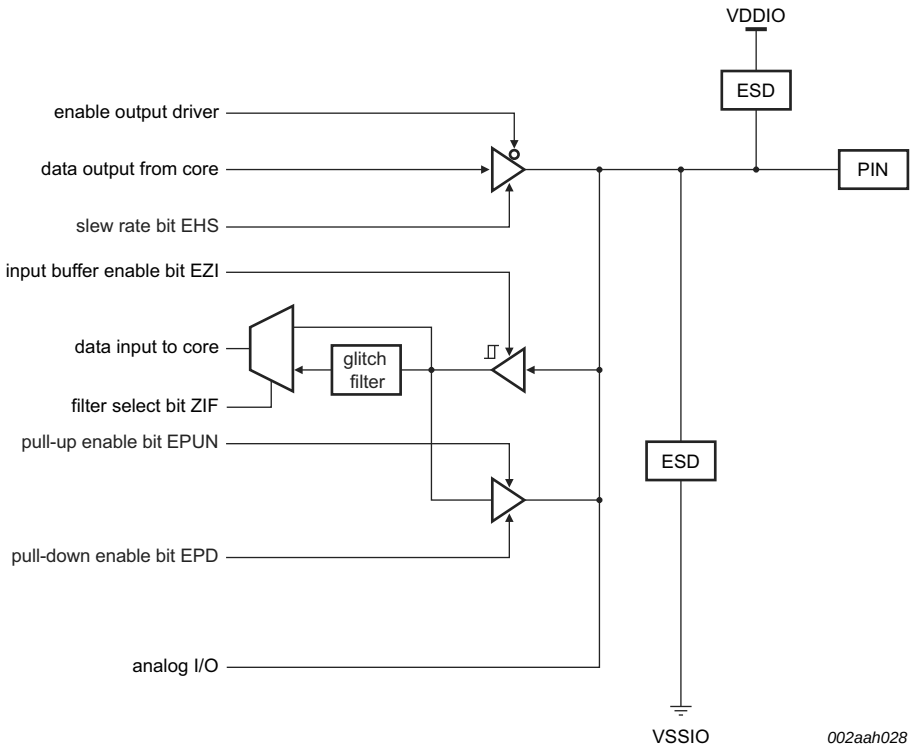


Fig 34. External static memory read/write access (PB = 0)



The glitch filter rejects pulses of typical 12 ns width.

Fig 46. Standard I/O pin configuration with analog input

13.6 Reset pin configuration

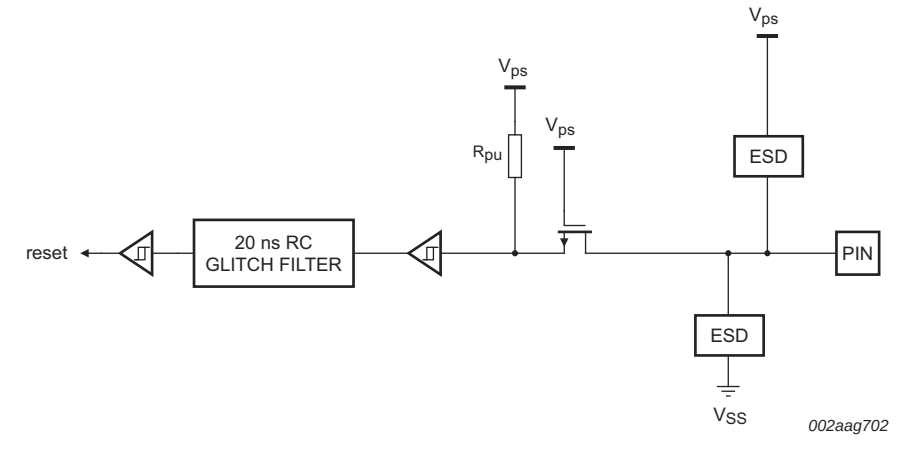
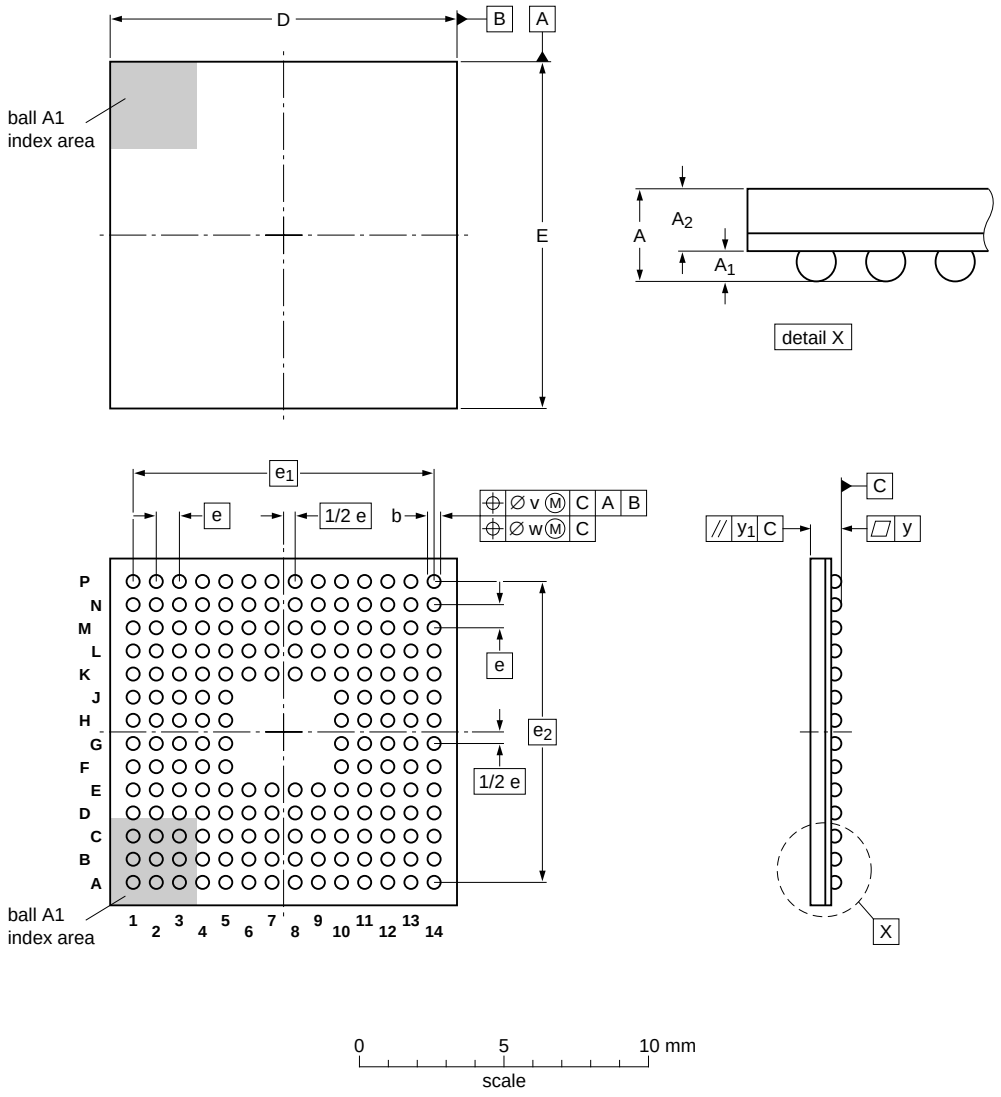


Fig 47. Reset pin configuration

13.7 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 48) or bus-powered device (see Figure 49).

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 52. Package outline of the TFBGA180 package