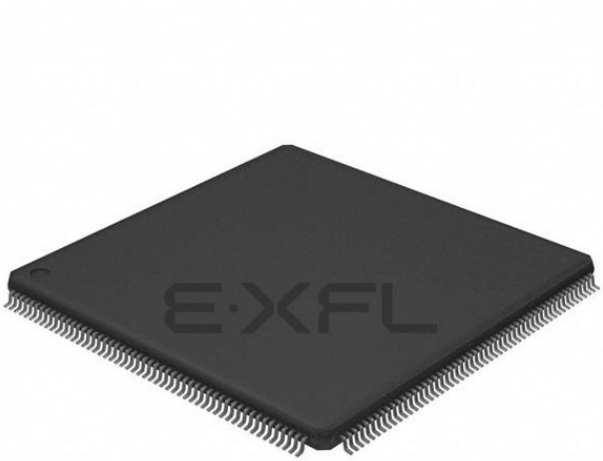

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	142
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	264K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4350fbd208-551

- Cortex-M0 Processor core
  - ARM Cortex-M0 co-processor capable of off-loading the main ARM Cortex-M4 application processor.
  - Running at frequencies of up to 204 MHz.
  - JTAG and built-in NVIC.
- On-chip memory
  - Up to 264 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - 64 kB ROM containing boot code and on-chip software drivers.
  - 64 bit + 256 bit general-purpose One-Time Programmable (OTP) memory.
- Clock generation unit
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC (IRC) oscillator trimmed to 1.5 % accuracy over temperature and voltage.
  - Ultra-low power Real-Time Clock (RTC) crystal oscillator.
  - Three PLLs allow CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. The second PLL is dedicated to the High-speed USB, the third PLL can be used as audio PLL.
  - Clock output.
- Configurable digital peripherals
  - Serial GPIO (SGPIO) interface.
  - State Configurable Timer (SCTimer/PWM) subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY (USB0).
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY (USB1).
  - USB interface electrical test software included in ROM USB stack.
  - Four 550 UARTs with DMA support: one UART with full modem interface; one UART with IrDA interface; three USARTs support UART synchronous mode and a smart card interface conforming to ISO7816 specification.
  - Up to two C_CAN 2.0B controllers with one channel each. Use of C_CAN controller excludes operation of all other peripherals connected to the same bus bridge. See Figure 1 and Ref. 2.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.
  - One SPI controller.

- One Fast-mode Plus I^2C-bus interface with monitor mode and with open-drain I/O pins conforming to the full I^2C-bus specification. Supports data rates of up to 1 Mbit/s.
- One standard I^2C-bus interface with monitor mode and with standard I/O pins.
- Two I^2S interfaces, each with DMA support and with one input and one output.

- Digital peripherals
  - External Memory Controller (EMC) supporting external SRAM, ROM, NOR flash, and SDRAM devices.
  - LCD controller with DMA support and a programmable display resolution of up to 1024 H $\times$ 768 V. Supports monochrome and color STN panels and TFT color panels; supports 1/2/4/8 bpp Color Look-Up Table (CLUT) and 16/24-bit direct pixel mapping.
  - Secure Digital Input Output (SD/MMC) card interface.
  - Eight-channel General-Purpose DMA controller can access all memories on the AHB and all DMA-capable AHB slaves.
  - Up to 164 General-Purpose Input/Output (GPIO) pins with configurable pull-up/pull-down resistors.
  - GPIO registers are located on the AHB for fast access. GPIO ports have DMA support.
  - Up to eight GPIO pins can be selected from all GPIO pins as edge and level sensitive interrupt sources.
  - Two GPIO group interrupt modules enable an interrupt based on a programmable pattern of input states of a group of GPIO pins.
  - Four general-purpose timer/counters with capture and match capabilities.
  - One motor control Pulse Width Modulator (PWM) for three-phase motor control.
  - One Quadrature Encoder Interface (QEI).
  - Repetitive Interrupt timer (RI timer).
  - Windowed watchdog timer (WWDT).
  - Ultra-low power Real-Time Clock (RTC) on separate power domain with 256 bytes of battery powered backup registers.
  - Alarm timer; can be battery powered.
- Analog peripherals
  - One 10-bit DAC with DMA support and a data conversion rate of 400 kSamples/s.
  - Two 10-bit ADCs with DMA support and a data conversion rate of 400 kSamples/s. Up to eight input channels per ADC.
- Unique ID for each device.
- Power
  - Single 3.3 V (2.2 V to 3.6 V) power supply with on-chip internal voltage regulator for the core supply and the RTC power domain.
  - RTC power domain can be powered separately by a 3 V battery supply.
  - Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
  - Processor wake-up from Sleep mode via wake-up interrupts from various peripherals.
  - Wake-up from Deep-sleep, Power-down, and Deep power-down modes via external interrupts and interrupts generated by battery powered blocks in the RTC power domain.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P3_1	G11	D10	F7	114	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I	**CAN0_RD —** CAN receiver input.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							I/O	**GPIO5[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
P3_2	F11	D9	G6	116	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	B13	A7	118	[4]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_SCK —** Serial clock for SPI.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P5_2	R4	M3	-	46	[2]	N; PU	I/O	**GPIO2[11] —** General purpose digital input/output pin.
							I	**MCI1 —** Motor control PWM channel 1, input.
							I/O	**EMC_D14 —** External memory data line 14.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I	**T1_CAP2 —** Capture input 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_3	T8	P6	-	54	[2]	N; PU	I/O	**GPIO2[12] —** General purpose digital input/output pin.
							I	**MCI0 —** Motor control PWM channel 0, input.
							I/O	**EMC_D15 —** External memory data line 15.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART 1.
							I	**T1_CAP3 —** Capture input 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_4	P9	N7	-	57	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART 1.
							O	**T1_MAT0 —** Match output 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_5	P10	N8	-	58	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							I/O	**EMC_D9 —** External memory data line 9.
							-	**R —** Function reserved.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							O	**T1_MAT1 —** Match output 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
P9_6	L11	M9	-	72	[2]	N; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for USART0.
PA_0	L12	L10	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**I2S1_RX_MCLK —** I2S1 receive master clock.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
PA_1	J14	H12	-	-	[3]	N; PU	I/O	**GPIO4[8] —** General purpose digital input/output pin.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_2	K15	J13	-	-	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PB_2	B12	B11	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							O	**LCD_VD21 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[22] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_3	A13	A12	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D6 —** ULPI link bidirectional data line 6.
							O	**LCD_VD20 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[23] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCTimer/PWM output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_4	B11	B10	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[24] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_5	A12	A11	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[25] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCTimer/PWM input 7.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PC_3	F5	-	-	-	[5]	N; PU	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**GPIO6[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
							AI	**ADC1_0 —** DAC output; ADC1 and ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_4	F4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**GPIO6[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							I/O	**SD_DAT0 —** SD/MMC data bus line 0.
PC_5	G4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							-	**R —** Function reserved.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**GPIO6[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							I/O	**SD_DAT1 —** SD/MMC data bus line 1.
PC_6	H6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							I/O	**GPIO6[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PD_8	P8	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCTimer/PWM input 6. Capture input 1 of timer 3.
							I/O	**EMC_D22 —** External memory data line 22.
							-	**R —** Function reserved.
							I/O	**GPIO6[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
PD_9	T11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D23 —** External memory data line 23.
							-	**R —** Function reserved.
							I/O	**GPIO6[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
PD_10	P11	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_1 —** SCTimer/PWM input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
							-	**R —** Function reserved.
							I/O	**GPIO6[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PD_11	N9	M7	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS3}}$ —** LOW active Chip Select 3 signal.
							-	**R —** Function reserved.
							I/O	**GPIO6[25] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							O	**CTOUT_14 —** SCTimer/PWM output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

LCD, Ethernet, USB0, and USB1 functions are not available on all parts. See Table 2.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
Clock pins								
CLK0	N5	M4	K3	45	[4]	O; PU	O	**EMC_CLK0 —** SDRAM clock 0.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							O	**EMC_CLK01 —** SDRAM clock 0 and clock 1 combined.
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
CLK1	T10	-	-	-	[4]	O; PU	O	**EMC_CLK1 —** SDRAM clock 1.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CGU_OUT0 —** CGU spare clock output 0.
							-	**R —** Function reserved.
							O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
CLK2	D14	P10	K6	99	[4]	O; PU	O	**EMC_CLK3 —** SDRAM clock 3.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							O	**EMC_CLK23 —** SDRAM clock 2 and clock 3 combined.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.
CLK3	P12	-	-	-	[4]	O; PU	O	**EMC_CLK2 —** SDRAM clock 2.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							I/O	**I2S1_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed *…continued*

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
EMC 16-bit	0	1	0	0	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	0	1	0	1	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Boot from device connected to USART0 using pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Boot from device connected to USART3 using pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

7.13 Memory mapping

The memory map shown in Figure 7 and Figure 8 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

Table 10. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pu}	pull-up current	V_I = 0 V	[14][15] [16]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	μA
I/O pins - high drive strength: standard drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[12]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[12]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

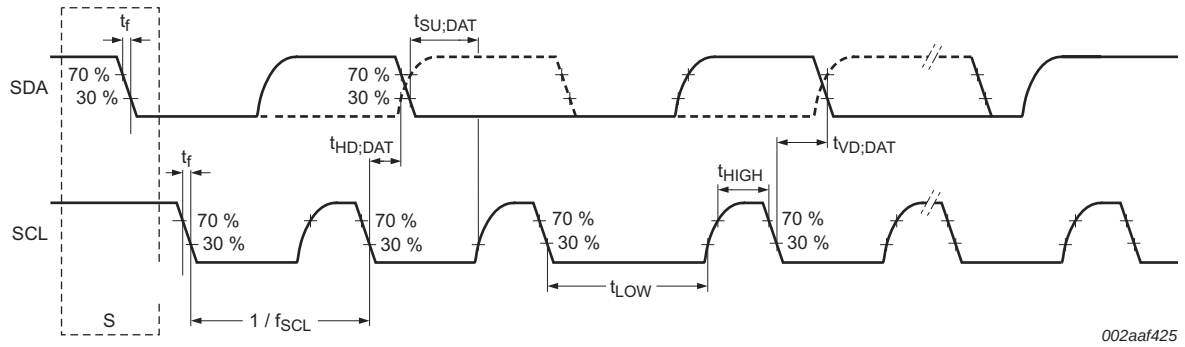


Fig 27. I^2C-bus pins clock timing

11.9 I^2S-bus interface

Table 22. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = −40 °C to +85 °C ; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns; corresponds to the SCK signal in the *I^2S-bus specification*.

11.11 SSP interface

Table 24. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		13.6	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.8	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.0	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.1	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)} + 3.2$	-	$0.5 \times T_{cy(clk)} + 6.1$	ns
		microwire frame format		$T_{cy(clk)} + 3.2$	-	$T_{cy(clk)} + 6.1$	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

11.13 SSP/SPI timing diagrams

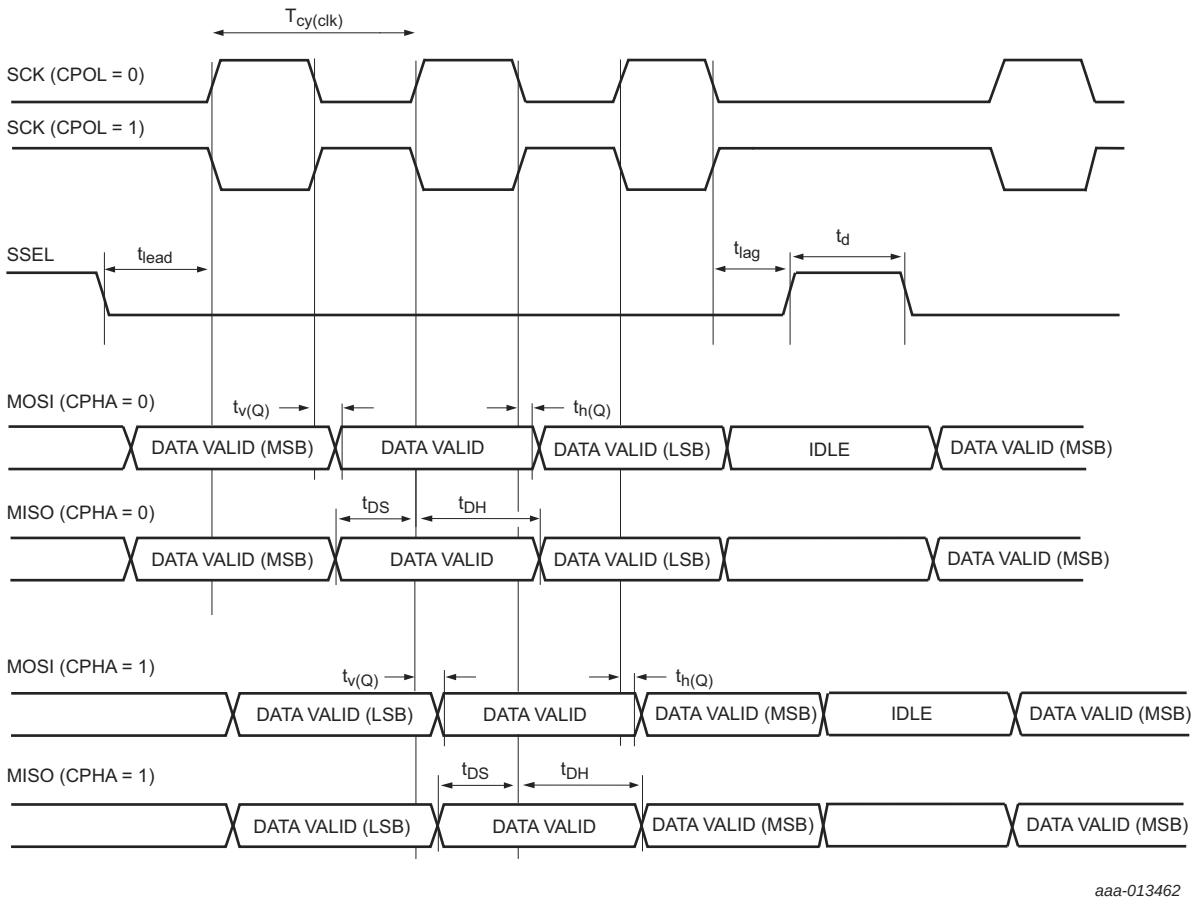


Fig 31. SSP_master mode timing (SPI mode)

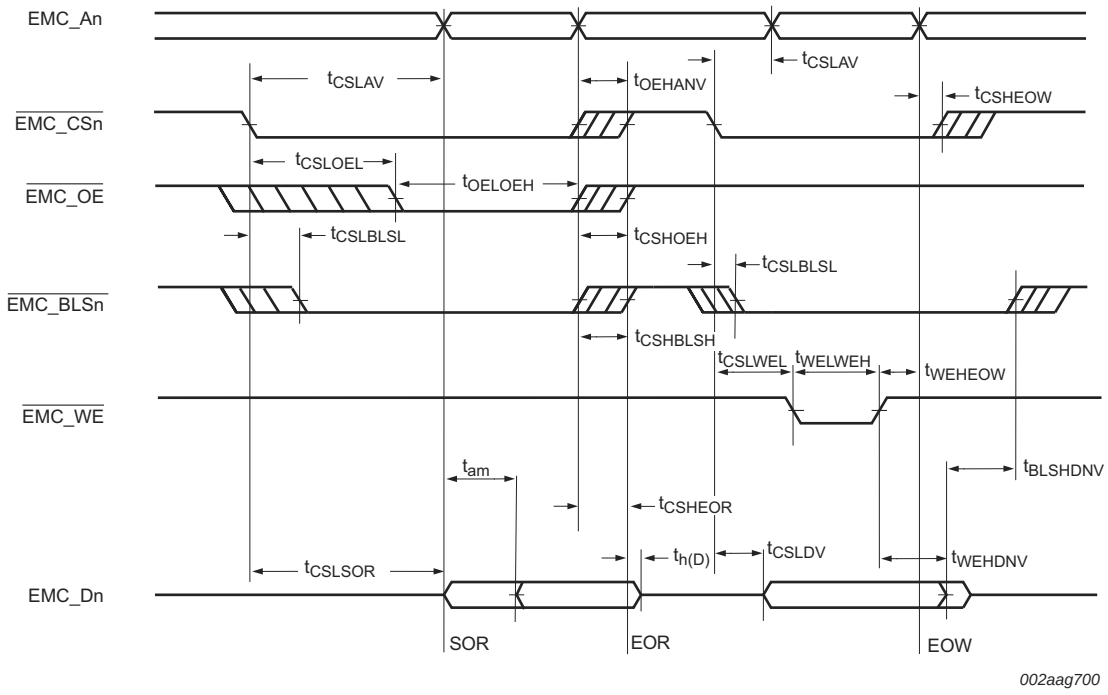


Fig 35. External static memory read/write access (PB = 1)

Table 32. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 85 °C; 2.2 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

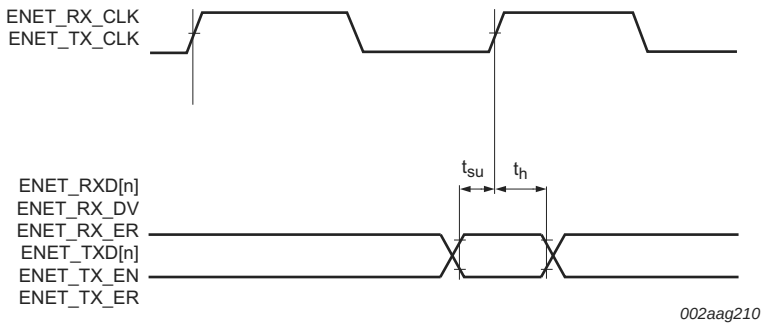


Fig 38. Ethernet timing

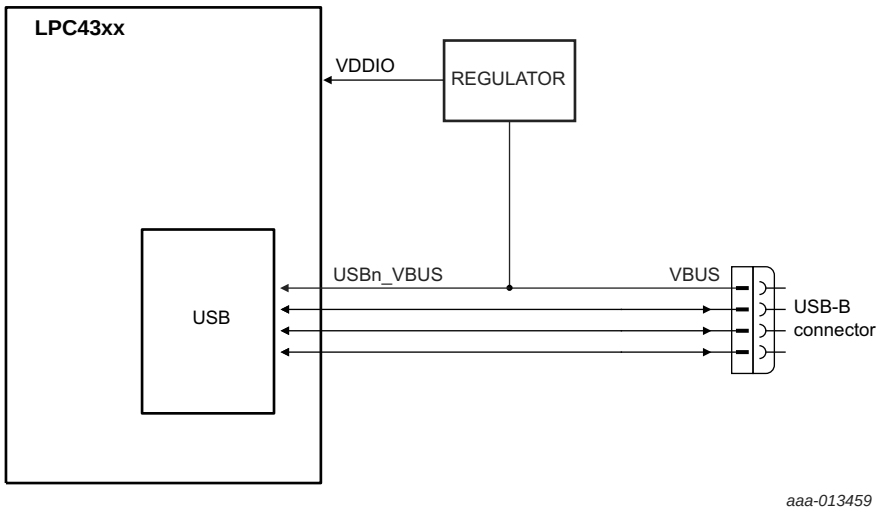


Fig 49. USB interface on a bus-powered device

Remark: If the VBUS function of the USB1 interface is not connected, configure the pin function for GPIO using the function control bits in the SYSCON block.

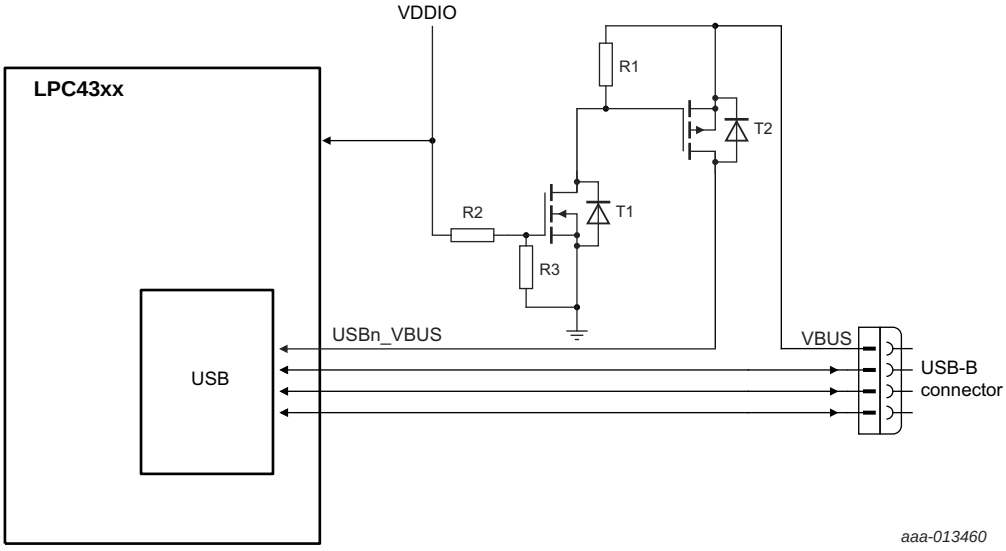
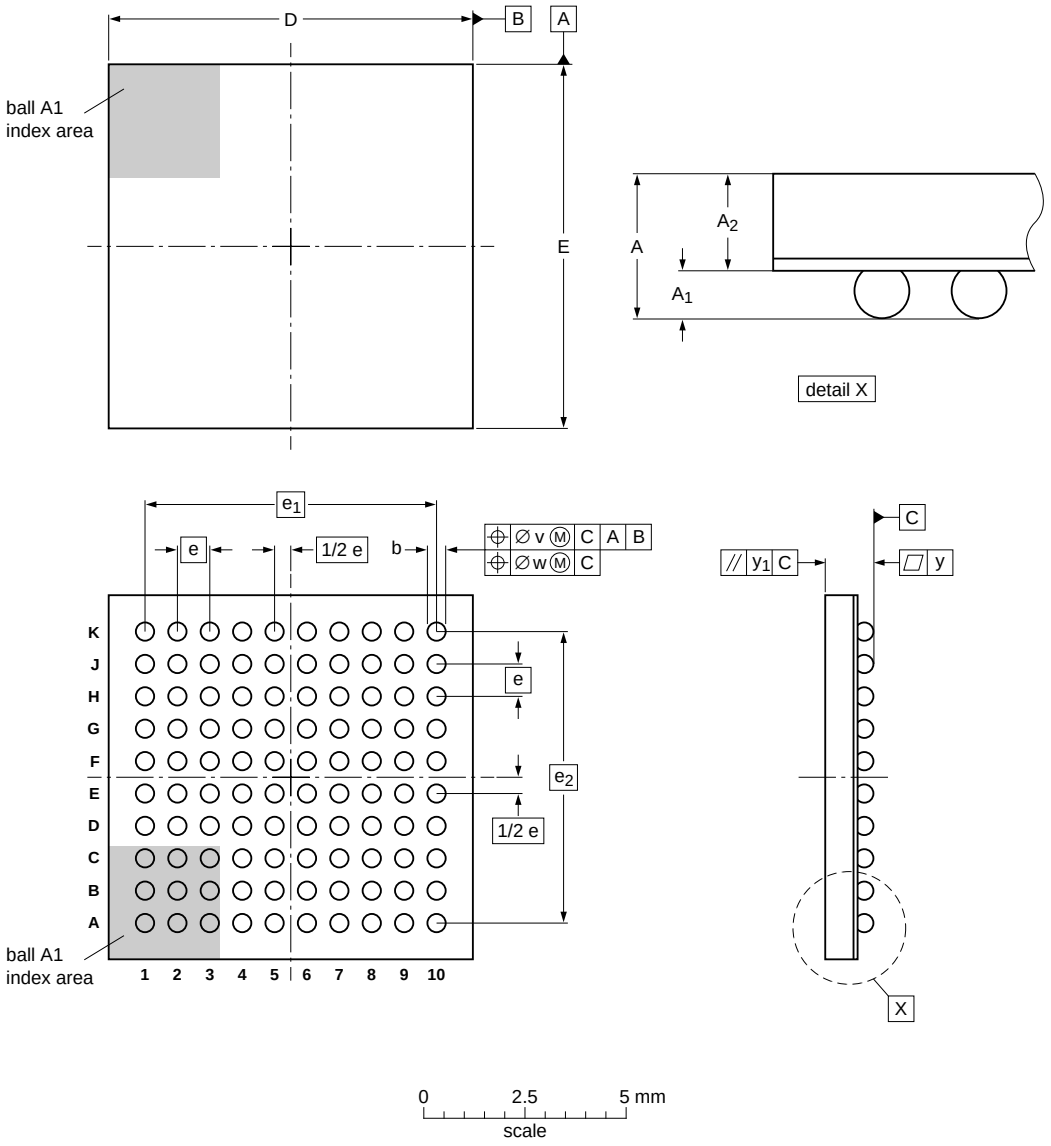


Fig 50. USB interface for USB operating in OTG mode

Remark: In OTG mode, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDDIO is not present.

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 53. Package outline of the TFBGA100 package

18. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4350_30_20_10 v.4.6	20160314	Product data sheet	-	LPC4350_30_20_10 v.4.5
Modifications:	• Updated Table 28 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC4350_30_20_10 v.4.5	20151126	Product data sheet	-	LPC4350_30_20_10 v.4.4
Modifications:	• Fixed the revision number on the first page to v.4.5. In v.4.4 of the document, the revision number of the first page was v.4.3 while the document was at v.4.4. • Added a table note: The values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. See Table 27 “Dynamic characteristics: Static asynchronous external memory interface”. • Changed footnote 12 in Table 3 “Pin description” with the text: VPP is internally connected to VDDIO for all packages with the exception of the LFBGA256 package. • Updated Figure 29 “I2S-bus timing (receive)”: for signal I2Sx_RX_WS changed second half of the signal from tsu(D) to th(D).			
LPC4350_30_20_10 v.4.4	20151117	Product data sheet	2015110031	LPC4350_30_20_10 v.4.3
Modifications:	• Added GPCLKIN section and table. See Section 11.6 “GPCLKIN” and Table 19 “Dynamic characteristic: GPCLKIN”. • Updated SSP slave and SSP master values in Table 24 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode.			
LPC4350_30_20_10 v.4.3	20150430	Product data sheet		LPC4350_30_20_10 v.4.2
Modifications:	• Updated Section 1 “General description”. • Table note 2 corrected in Table 10. • Updated USART dynamic characteristics table. See Table 23. • Updated SD/MMC dynamic characteristics table. See Table 33. • Updated SPIFI dynamic characteristics table. See Table 35. • Added SSP slave timing data. See Table 24. • Updated USB dynamic characteristics table: USB0 and USB1 pins (full-speed). t_r Min 4 ns, Max 20 ns; t_f Min 4 ns, Max 20 ns; t_{FRFM} Min 90 %, Max 111.11 %. See Table 30: • Added band gap characteristics table. See Table 13. • Added motor control PWM instead of PWM to Table 2. • Added remark to Table 30.			
LPC4350_30_20_10 v.4.2	20140818	Product data sheet	201408013F01	LPC4350_30_20_10 v.4.1

Table 44. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Temperature range for simulated timing characteristics corrected to T_{amb} = −40 °C to +85 °C in Section 11 “Dynamic characteristics”. • SPIFI timing added. See Section 11.15. • SPIFI maximum data rate changed to 52 MB per second. • Editorial updates. • Figure 25 and Figure 26 updated for full temperature range. • Section 7.23 “Serial Wire Debug/JTAG” updated. • The following changes were made on the TFBGA180 pinout in Table 3: – P1_13 moved from ball D6 to L8. – P7_5 moved from ball C7 to A7. – PF_4 moved from ball L8 to D6. – $\overline{\text{RESET}}$ moved from ball B7 to C7. – RTCX2 moved from ball A7 to B7. – Ball G10 changed from VSS to VDDIO.			
LPC4350_30_20_10 v.3.4	20120904	Preliminary data sheet	-	LPC4350_30_20_10 v.3.3
Modifications:	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • Minimum value for all supply voltages changed to -0.5 V in Table 6.			
LPC4350_30_20_10 v.3.3	20120821	Preliminary data sheet	-	LPC4350_30_20_10 v.3.2
Modifications:	• Parameter t_{wake} updated in Table 13 for wake-up from deep power-down mode and reset. • Dynamic characteristics of the SD/MMC controller updated in Table 28. • Dynamic characteristics of the LCD controller updated in Table 29. • Dynamic characteristics of the SSP controller updated in Table 21. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”,“USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10. • AES removed. AES is available on parts LPC43Sxx only. • Pin configuration diagrams corrected for LQFP packages (Figure 5 and Figure 6). • Figure 10 updated. • All power consumption data updated in Table 10 and Section 10.1 “Power consumption”. • BOD levels updated in Table 12. • SWD debug option removed for Cortex-M0 core.			
LPC4350_30_20_10 v.3.2	20120604	Preliminary data sheet	-	LPC4350_30_20_10 v.3.1
LPC4350_30_20_10 v.3.1	20120105	Objective data sheet	-	LPC4350_30_20_10 v.3
LPC4350_30_20_10 v.3	20111205	Objective data sheet	-	LPC4350_30_20_10 v.2.1
LPC4350_30_20_10 v.2.1	20110923	Objective data sheet	-	LPC4350_30_20_10 v.2
LPC4350_30_20_10 v.2	20110714	Objective data sheet	-	LPC4350_30_20_10 v.1
LPC4350_30_20_10 v.1	20101029	Objective data sheet	-	-