Renesas Electronics America Inc - R5F10WLFAFA#X0 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	42
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wlfafa-x0

Absolute Maximum Ratings (3/3)

	Parameter	Symbol	Conditions		Ratings	Unit
<R>	Output current, high	I_{OH1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	–40	mA
<R>			Total of all pins –170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	–170	mA
<R>		I_{OH2}	Per pin	P20, P21	–0.5	mA
<R>			Total of all pins		–1	mA
<R>	Output current, low	I_{OL1}	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
			Total of all pins 170 mA	P40 to P47, P130	70	mA
<R>				P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
<R>		I_{OL2}	Per pin	P20, P21	1	mA
<R>			Total of all pins		2	mA
	Operating ambient temperature	T_A	In normal operation mode		–40 to +85	°C
			In flash memory programming mode			
	Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20, P21		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –10.0 mA	V_{DD} – 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	V_{DD} – 0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 and P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 and P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 and P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL3} = 1.0 mA			0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

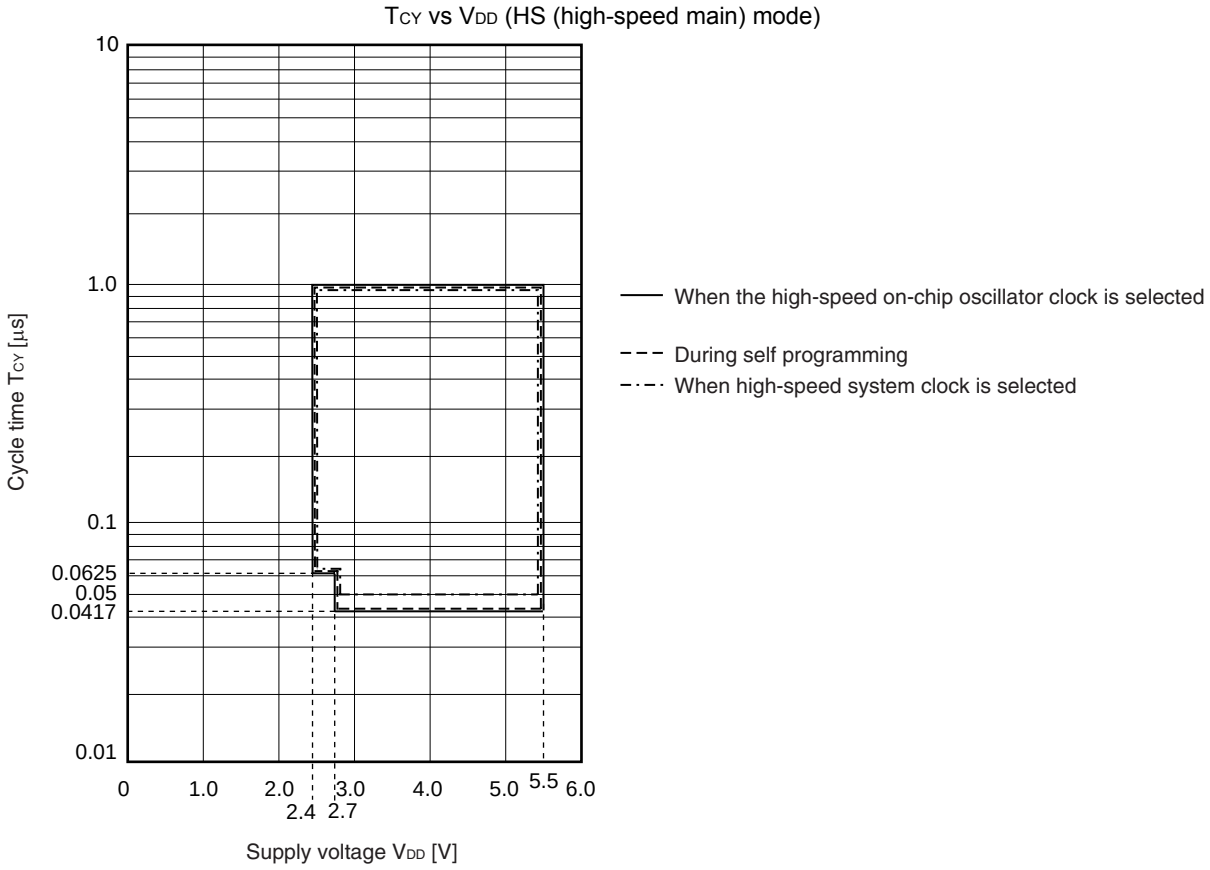
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1						0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 2, 3	f_{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4						0.04		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz					0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V				1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1						75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1						75.0		μA
LVD operating current	I_{LVD} Notes 1, 7						0.08		μA
Comparator operating current	I_{CMP} Notes 1, 11	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				6.5		μA
			Comparator low-speed mode				1.7		μA
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode				8.0		μA
			Comparator high-speed mode				4.0		μA
			Comparator low-speed mode				1.3		μA
Self-programming operating current	I_{FSP} Notes 1, 9						2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8						2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	While the mode is shifting Note 10				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation					0.70	0.84	mA
LCD operating current	I_{LCD1} Notes 1, 12, 13	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.20	μA
	I_{LCD2} Note 1, 12	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V (V_{LCD} = 04H)		0.85	2.20	μA
					V_{DD} = 5.0 V, V_{L4} = 5.1 V (V_{LCD} = 12H)		1.55	3.70	μA
	I_{LCD3} Note 1, 12	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20	0.50	μA

(**Notes** and **Remarks** are listed on the next page.)

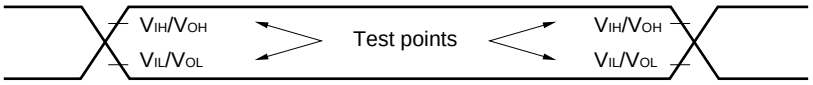
Note Operation is not possible if 1.6 V ≤ V_{DD} < 1.8 V in LV (low-voltage main) mode while the system is operating on the subsystem clock.

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)
m: Unit number (m = 0), n: Channel number (n = 0 to 7))

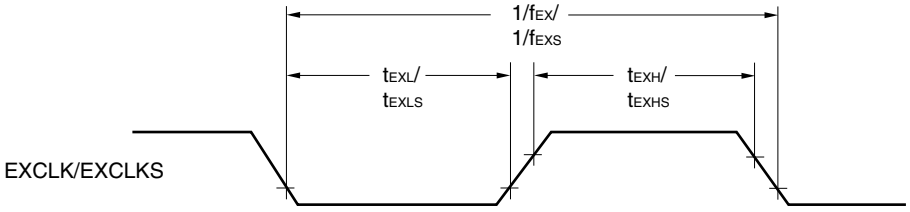
Minimum Instruction Execution Time during Main System Clock Operation



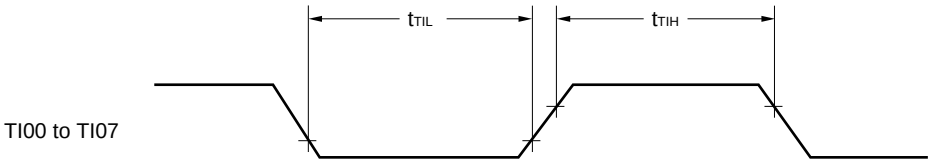
AC Timing Test Points

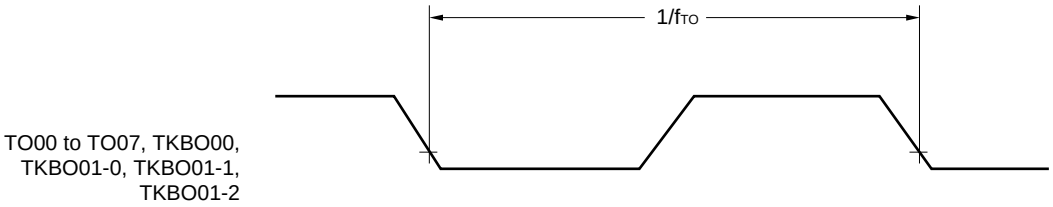


External System Clock Timing

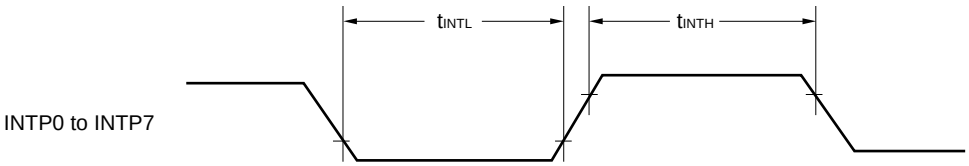


TI/TO Timing

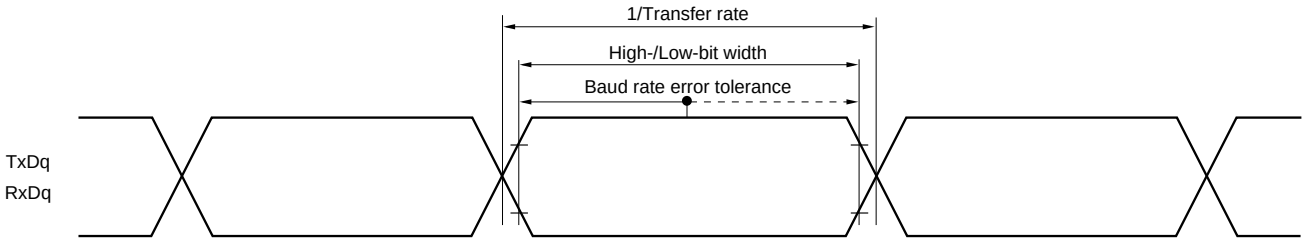




Interrupt Request Input Timing



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (simplified I²C mode)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		–		–		250 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1850		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK}+ 85 Note 2		1/f_{MCK}+ 145 Note 2		1/f_{MCK}+ 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK}+ 145 Note 2		1/f_{MCK}+ 145 Note 2		1/f_{MCK}+ 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+ 230 Note 2		1/f_{MCK}+ 230 Note 2		1/f_{MCK}+ 230 Note 2		ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–		–		1/f_{MCK}+ 290 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	–	–	–	–	0	405	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps

2. Condition in HS (high-speed main) mode

3. Use it with $V_{DD} \geq V_b$.

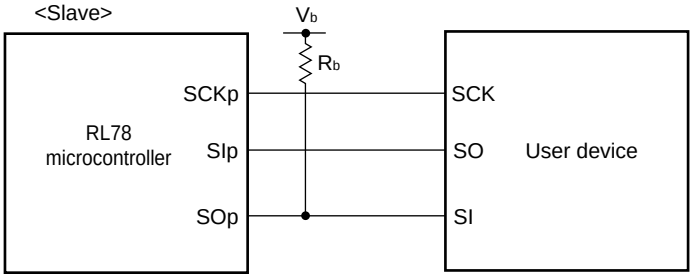
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	When power supply rises	3.98	4.06	4.14	V
			When power supply falls	3.90	3.98	4.06	V
		V_{LVD1}	When power supply rises	3.68	3.75	3.82	V
			When power supply falls	3.60	3.67	3.74	V
		V_{LVD2}	When power supply rises	3.07	3.13	3.19	V
			When power supply falls	3.00	3.06	3.12	V
		V_{LVD3}	When power supply rises	2.96	3.02	3.08	V
			When power supply falls	2.90	2.96	3.02	V
		V_{LVD4}	When power supply rises	2.86	2.92	2.97	V
			When power supply falls	2.80	2.86	2.91	V
		V_{LVD5}	When power supply rises	2.76	2.81	2.87	V
			When power supply falls	2.70	2.75	2.81	V
		V_{LVD6}	When power supply rises	2.66	2.71	2.76	V
			When power supply falls	2.60	2.65	2.70	V
		V_{LVD7}	When power supply rises	2.56	2.61	2.66	V
			When power supply falls	2.50	2.55	2.60	V
		V_{LVD8}	When power supply rises	2.45	2.50	2.55	V
			When power supply falls	2.40	2.45	2.50	V
		V_{LVD9}	When power supply rises	2.05	2.09	2.13	V
			When power supply falls	2.00	2.04	2.08	V
		V_{LVD10}	When power supply rises	1.94	1.98	2.02	V
			When power supply falls	1.90	1.94	1.98	V
		V_{LVD11}	When power supply rises	1.84	1.88	1.91	V
			When power supply falls	1.80	1.84	1.87	V
		V_{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
		V_{LVD13}	When power supply rises	1.64	1.67	1.70	V
			When power supply falls	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

"G: Industrial applications (T_A = –40 to +105°C) differ from "A: Consumer applications" in function as follows:

Fields of Application	A: Consumer applications	G: Industrial applications
Operating ambient temperature	T_A = –40 to +85°C	T_A = –40 to +105°C
Operation mode operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V: ±1.0 % @ T_A = –20 to +85°C ±1.5 % @ T_A = –40 to –20°C 1.6 V ≤ V_{DD} < 1.8 V: ±5.0 % @ T_A = –20 to +85°C ±5.5 % @ T_A = –40 to –20°C	2.4 V ≤ V_{DD} ≤ 5.5 V: ±2.0 % @ T_A = +85 to +105°C ±1.0 % @ T_A = –20 to +85°C ±1.5 % @ T_A = –40 to –20°C
Serial array unit	UART CSI: f_{CLK}/2 (16 Mbps supported), f_{CLK}/4 Simplified I^2C	UART CSI: f_{CLK}/4 Simplified I^2C
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fase mode
Voltage detector	• Rising: 1.67 V to 4.06 V (14 levels) • Falling: 1.63 V to 3.98 V (14 levels)	• Rising: 2.61 V to 4.06 V (8 levels) • Falling: 2.55 V to 3.98 V (8 levels)

Remark Electrical specifications of G: Industrial applications (T_A = –40 to +105°C) differ from "A: Consumer applications". For details, see **3.1** to **3.11** below.

Absolute Maximum Ratings (2/3)

Parameter	Symbol	Conditions		Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage[Note 1]		–0.3 to +2.8 and –0.3 to V_{L4} +0.3	V
	V_{L2}	V_{L2} voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{L3}	V_{L3} voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{L4}	V_{L4} voltage[Note 1]		–0.3 to +6.5	V
	V_{LCAP}	CAPL, CAPH voltage[Note 1]		–0.3 to V_{L4} +0.3[Note 2]	V
	V_{OUT}	COM0 to COM7 SEG0 to SEG50 output voltage	External resistance division method	–0.3 to V_{DD} +0.3[Note 2]	V
			Capacitor split method	–0.3 to V_{DD} +0.3[Note 2]	V
			Internal voltage boosting method	–0.3 to V_{L4} +0.3[Note 2]	V

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS}: Reference voltage

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNotes 1, 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to +105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–2		+2	%
		–20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1		+1	%
		–40 to –20°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

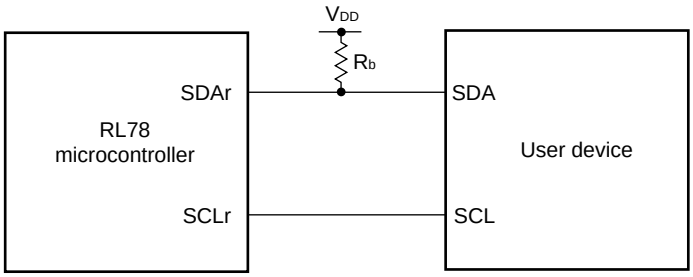
2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

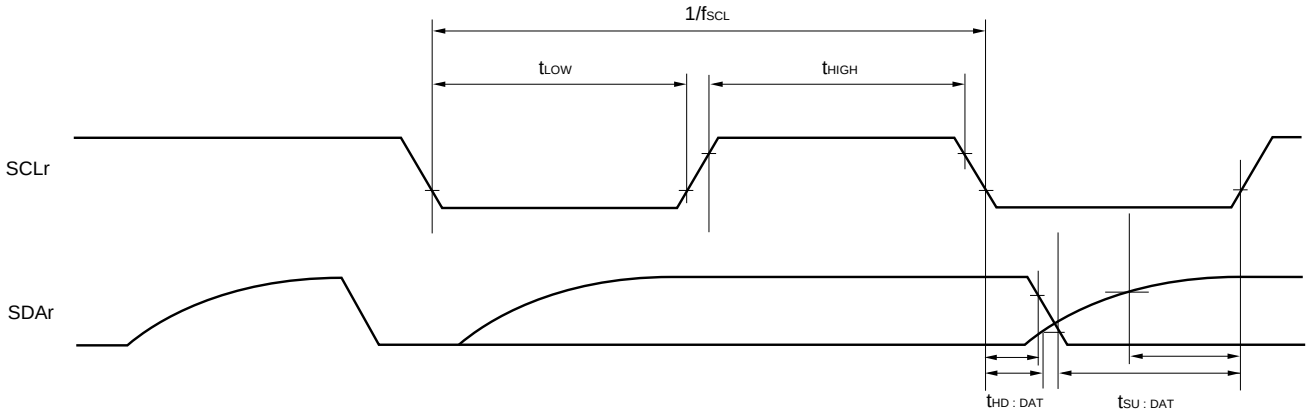
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 and P21, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port mode and when external clock is input			1	μA
				Resonator connected			10	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P20 and P21, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port mode and when external clock is input			–1	μA
				Resonator connected			–10	μA
On-chip pull-up resistance	R_{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$V_I = V_{SS}$		10	20	100	kΩ
	R_{U2}	P40 to P44	$V_I = V_{SS}$		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)

<R> **3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$f_{MCK}/12$[Note]	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$f_{MCK}/12$[Note]	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		$f_{MCK}/12$[Note]	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps

Note Transfer rate in SNOOZE mode is 4800 bps only.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Note 5**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

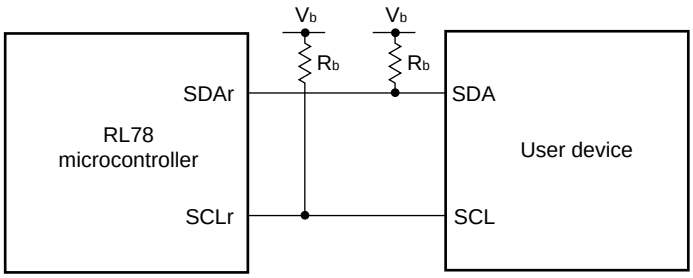
$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

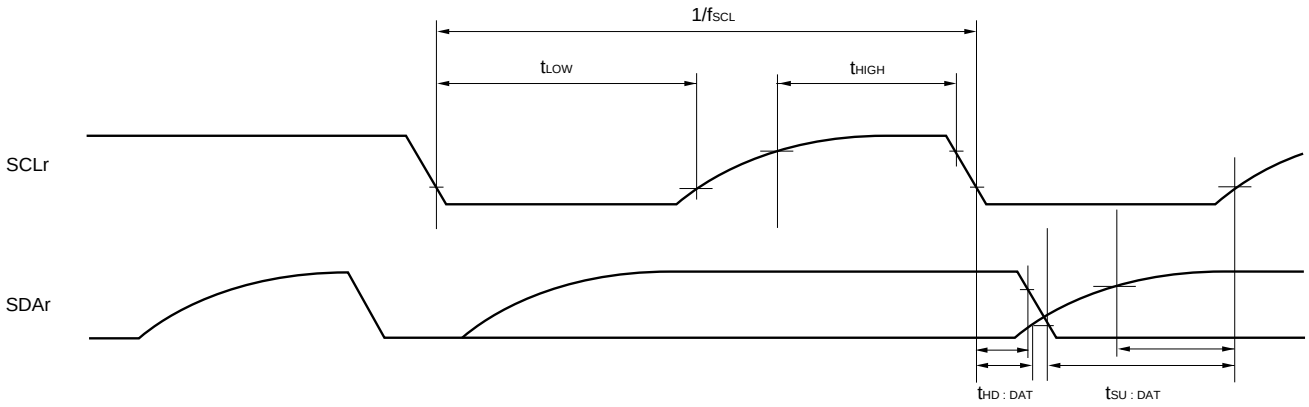
* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02)

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.2%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. See **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pins: ANI0, ANI1, ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0, ANI1, ANI16 to ANI25	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0, ANI1, ANI16 to ANI25		0		V_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))		V_{BGR}[Note 3]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))		V_{TMPS25}[Note 3]			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See **3.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.3 Comparator

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref			0		V_{DD} – 1.4	V
	Ivcmp			–0.3		V_{DD} + 0.3	V
Output delay	td	V_{DD} = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode		0.66V_{DD}	0.76V_{DD}	0.86V_{DD}	V
Low-electric-potential reference voltage	VTW–	Comparator high-speed mode, window mode		0.14V_{DD}	0.24V_{DD}	0.34V_{DD}	V
Operation stabilization wait time	t_{CMP}			100			μs
Internal reference output voltage[Note]	V_{BGR}	2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.50	V

Note Cannot be used in subsystem clock operation and STOP mode.

3.6.4 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply rises	1.45	1.51	1.57	V
	V_{PDR}	When power supply falls	1.44	1.50	1.56	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode and when the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.