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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	42
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wlgafa-30

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	−0.3 to V_{DD} +0.3[Note 2]	V
	V_{I2}	P60 and P61 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	EXCLK, EXCLKS, $\overline{RESET}$	−0.3 to V_{DD} +0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	−0.3 to V_{DD} +0.3[Note 2]	V
Analog input voltage	V_{AI1}	ANI0, ANI1, ANI16 to ANI26	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

  2. Must be 6.5 V or lower.

  3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

  2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

  3. Vss: Reference voltage

RENESAS

Absolute Maximum Ratings (3/3)

	Parameter	Symbol	Conditions			Ratings	Unit
<R> <R>	Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130		−40	mA
			Total of all pins −170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130		−170	mA
<R> <R>		I$_{OH2}$	Per pin	P20, P21		−0.5	mA
			Total of all pins			−1	mA
<R>	Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130		40	mA
			Total of all pins 170 mA	P40 to P47, P130		70	mA
<R>				P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127		100	mA
<R> <R>		I$_{OL2}$	Per pin	P20, P21		1	mA
			Total of all pins			2	mA
	Operating ambient temperature	T$_A$	In normal operation mode			−40 to +85	°C
			In flash memory programming mode				
	Storage temperature	T$_{stg}$				−65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130				20.0[Note 2]	mA
		Per pin for P60 and P61				15.0[Note 2]	mA
		Total of P40 to P47, P130 (When duty = 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			70.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			15.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			9.0	mA
			1.6 V ≤ V$_{DD}$ < 1.8 V			4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70%[Note 3])	4.0 V ≤ V$_{DD}$ ≤ 5.5 V			90.0	mA
			2.7 V ≤ V$_{DD}$ < 4.0 V			35.0	mA
			1.8 V ≤ V$_{DD}$ < 2.7 V			20.0	mA
			1.6 V ≤ V$_{DD}$ < 1.8 V			10.0	mA
		Total of all pins (When duty = 70%[Note 3])				160.0	mA
	I$_{OL2}$	Per pin for P20 and P21				0.4[Note 2]	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			0.8	mA

<R>

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from an output pin to the V$_{SS}$ pin

　2. Do not exceed the total current value.

　3. Output current value under conditions where the duty factor ≤ 70%.

　　The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I$_{OL}$ = 70.0 mA
  　　Total output current of pins = (70.0 × 0.7)/(80 × 0.01) ≅ 61.25 mA

　　However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T$_A$ = –40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V$_{DD}$ ≤ 5.5 V	2.2		V$_{DD}$	V
			TTL input buffer 3.3 V ≤ V$_{DD}$ < 4.0 V	2.0		V$_{DD}$	V
			TTL input buffer 1.6 V ≤ V$_{DD}$ < 3.3 V	1.5		V$_{DD}$	V
	V$_{IH3}$	P20, P21		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60, P61		0.7V$_{DD}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0		0.2V$_{DD}$	V
	V$_{IL2}$	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V$_{DD}$ < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20, P21		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60, P61		0		0.3V$_{DD}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2V$_{DD}$	V

Caution **The maximum value of V$_{IH}$ of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V$_{DD}$, even in the N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol		Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			$f_{MCK}/6$ [Note 1]		$f_{MCK}/6$ [Note 1]		$f_{MCK}/6$ [Note 1]	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		4.0		1.3		0.6	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$f_{MCK}/6$ [Note 1]		$f_{MCK}/6$ [Note 1]		$f_{MCK}/6$ [Note 1]	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		4.0		1.3		0.6	Mbps
			1.8 V (2.4 V [Note 4]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			$f_{MCK}/6$ [Note s1, 2]		$f_{MCK}/6$ [Notes 1, 2]		$f_{MCK}/6$ [Notes 1, 2]	bps
				Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ [Note 3]		4.0		1.3		0.6	Mbps

Notes 1. Transfer rate in SNOOZE mode is 4800 bps only.

     2. Use it with $V_{DD} ≥ V_b$.

     3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

         HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

                                   16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

         LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

         LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

     4. Condition in the HS (high-speed main) mode

Caution   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).** For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

       2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

       3. f_{MCK}: Serial array unit operation clock frequency

          (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = −40 to +85°C, 2.7 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200		1150		1150		ns
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t$_{KH1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		ns
SCKp low-level width	t$_{KL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑)[Note 1]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑)[Note 1]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output[Note 1]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130		130	ns
SIp setup time (to SCKp↓)[Note 2]	t$_{SIK1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		33		110		110		ns
SIp hold time (from SCKp↓)[Note 2]	t$_{KSI1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOp output[Note 2]	t$_{KSO1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			10		10		10	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input channel	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0, ANI1	–	See **2.6.1 (2)**.	See **2.6.1 (3)**.
ANI16 to ANI25	See **2.6.1 (1)**.		
Internal reference voltage Temperature sensor output voltage	See **2.6.1 (1)**.		–

(1)　When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pins: ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]		1.2	±8.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI16 to ANI25	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.60	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$[Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V[Note 4]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI25		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode))			V$_{BGR}$[Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode))			V$_{TMPS25}$[Note 5]		V

(**Notes** are listed on the next page.)

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T$_A$ = –40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$[Note 3],
Reference voltage (–) = AV$_{REFM}$[Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$[Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

   2. This value is indicated as a ratio (%FSR) to the full-scale value.

   3. See **2.6.2 Temperature sensor/internal reference voltage characteristics**.

   4. When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.

   Zero-scale error: Add ±0.35%FSR to the AV$_{REFM}$ MAX. value.

   Integral linearity error: Add ±0.5 LSB to the AV$_{REFM}$ MAX. value.

   Differential linearity error: Add ±0.2 LSB to the AV$_{REFM}$ MAX. value.

2.6.2 Temperature sensor /internal reference voltage characteristics

(T$_A$ = –40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference output voltage	V$_{BGR}$	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$				5	μs

2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = −40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	When power supply rises	3.98	4.06	4.14	V
			When power supply falls	3.90	3.98	4.06	V
		V_{LVD1}	When power supply rises	3.68	3.75	3.82	V
			When power supply falls	3.60	3.67	3.74	V
		V_{LVD2}	When power supply rises	3.07	3.13	3.19	V
			When power supply falls	3.00	3.06	3.12	V
		V_{LVD3}	When power supply rises	2.96	3.02	3.08	V
			When power supply falls	2.90	2.96	3.02	V
		V_{LVD4}	When power supply rises	2.86	2.92	2.97	V
			When power supply falls	2.80	2.86	2.91	V
		V_{LVD5}	When power supply rises	2.76	2.81	2.87	V
			When power supply falls	2.70	2.75	2.81	V
		V_{LVD6}	When power supply rises	2.66	2.71	2.76	V
			When power supply falls	2.60	2.65	2.70	V
		V_{LVD7}	When power supply rises	2.56	2.61	2.66	V
			When power supply falls	2.50	2.55	2.60	V
		V_{LVD8}	When power supply rises	2.45	2.50	2.55	V
			When power supply falls	2.40	2.45	2.50	V
		V_{LVD9}	When power supply rises	2.05	2.09	2.13	V
			When power supply falls	2.00	2.04	2.08	V
		V_{LVD10}	When power supply rises	1.94	1.98	2.02	V
			When power supply falls	1.90	1.94	1.98	V
		V_{LVD11}	When power supply rises	1.84	1.88	1.91	V
			When power supply falls	1.80	1.84	1.87	V
		V_{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
		V_{LVD13}	When power supply rises	1.64	1.67	1.70	V
			When power supply falls	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

RENESAS

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V$_{DD}$		−0.5 to +6.5	V
REGC pin input voltage	V$_{IREGC}$	REGC	−0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1]	V
Input voltage	V$_{I1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	−0.3 to V$_{DD}$ +0.3[Note 2]	V
	V$_{I2}$	P60 and P61 (N-ch open-drain)	−0.3 to +6.5	V
	V$_{I3}$	EXCLK, EXCLKS, $\overline{RESET}$	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Output voltage	V$_{O1}$	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	−0.3 to V$_{DD}$ +0.3[Note 2]	V
Analog input voltage	V$_{AI1}$	ANI0, ANI1, ANI16 to ANI26	−0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF(+)}$ +0.3[Notes 2, 3]	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV$_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV$_{REF(+)}$: + side reference voltage of the A/D converter.

3. Vss: Reference voltage

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)**Note**	Ceramic resonator/ crystal resonator	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f$_{XT}$)**Note**	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency**Notes 1, 2**	f$_{IH}$			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to +105°C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−2		+2	%
		−20 to +85°C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−1		+1	%
		−40 to −20°C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V$_{DD}$ ≤ 5.5 V	2.2		V$_{DD}$	V
			TTL input buffer 3.3 V ≤ V$_{DD}$ < 4.0 V	2.0		V$_{DD}$	V
			TTL input buffer 2.4 V ≤ V$_{DD}$ < 3.3 V	1.5		V$_{DD}$	V
	V$_{IH3}$	P20, P21		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60, P61		0.7V$_{DD}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0		0.2V$_{DD}$	V
	V$_{IL2}$	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer 4.0 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V$_{DD}$ < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ V$_{DD}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20, P21		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60, P61		0		0.3V$_{DD}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V

Caution **The maximum value of V$_{IH}$ of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V$_{DD}$, even in the N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL}[Note 1]						0.20		μA
RTC2 operating current	I_{RTC}[Notes 1, 2, 3]	f_{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I_{TMKA}[Notes 1, 2, 4]						0.04		μA
Watchdog timer operating current	I_{WDT}[Notes 1, 2, 5]	f_{IL} = 15 kHz					0.22		μA
A/D converter operating current	I_{ADC}[Notes 1, 6]	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V				1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}[Note 1]						75.0		μA
Temperature sensor operating current	I_{TMPS}[Note 1]						75.0		μA
LVD operating current	I_{LVD}[Notes 1, 7]						0.08		μA
Comparator operating current	I_{CMP}[Notes 1, 11]	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				6.5		μA
			Comparator low-speed mode				1.7		μA
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode				8.0		μA
			Comparator high-speed mode				4.0		μA
			Comparator low-speed mode				1.3		μA
Self-programming operating current	I_{FSP}[Notes 1, 9]						2.00	12.20	mA
BGO operating current	I_{BGO}[Notes 1, 8]						2.00	12.20	mA
SNOOZE operating current	I_{SNOZ}[Note 1]	ADC operation	While the mode is shifting[Note 10]				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation					0.70	0.84	mA
LCD operating current	I_{LCD1}[Notes 1, 12, 13]	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.20.	μA
	I_{LCD2}[Note 1, 12]	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V (V_{LCD} = 04H)		0.85	2.20	μA
					V_{DD} = 5.0 V, V_{L4} = 5.1 V (V_{LCD} = 12H)		1.55	3.70	μA
	I_{LCD3}[Note 1, 12]	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20	0.50	μA

(**Notes** and **Remarks** are listed on the next page.)

Simplified I^{2}C mode connection diagram (during communication at same potential)
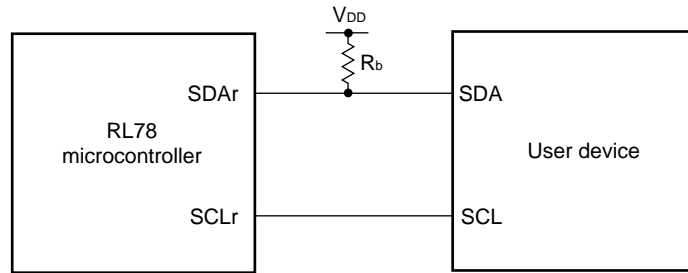
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
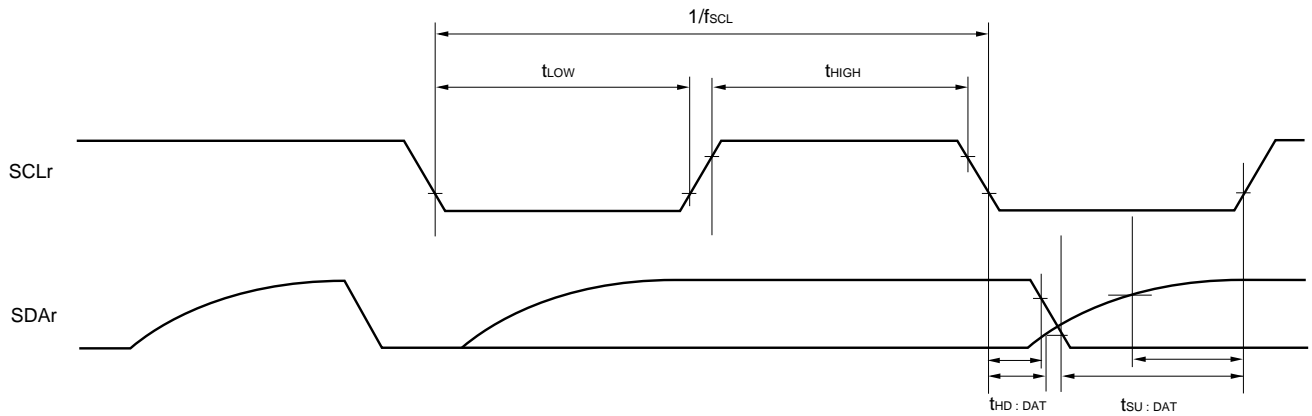
Remarks 1. R$_b$[Ω]: Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)

<R>

3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			f$_{MCK}$/12**Note**	bps
				Theoretical value of the maximum transfer rate f$_{CLK}$ = 24 MHz, f$_{MCK}$ = f$_{CLK}$		2.0	Mbps
			2.7 V ≤ V$_{DD}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V			f$_{MCK}$/12**Note**	bps
				Theoretical value of the maximum transfer rate f$_{CLK}$ = 24 MHz, f$_{MCK}$ = f$_{CLK}$		2.0	Mbps
			2.4 V ≤ V$_{DD}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			f$_{MCK}$/12**Note**	bps
				Theoretical value of the maximum transfer rate f$_{CLK}$ = 24 MHz, f$_{MCK}$ = f$_{CLK}$		2.0	Mbps

Note   Transfer rate in SNOOZE mode is 4800 bps only.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1.   V$_b$[V]: Communication line voltage

2.   q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

3.   f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Notes 5. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V $\leq V_{DD}$ < 3.3 V and 1.6 V $\leq V_b \leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

 * This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)

RENESAS
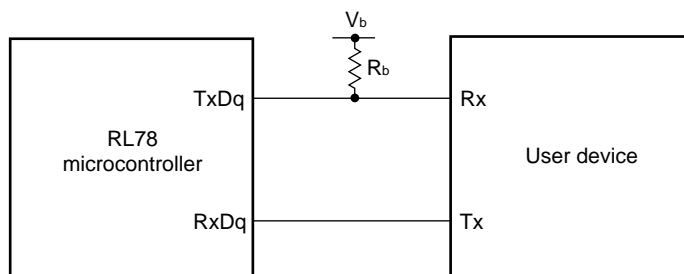
3.5.2 Serial interface IICA

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz	–	–	0	400	kHz
		Normal mode: f$_{CLK}$ ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0[Note 3]	3.45	0[Note 3]	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C$_b$ (communication line capacitance) and the value of R$_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
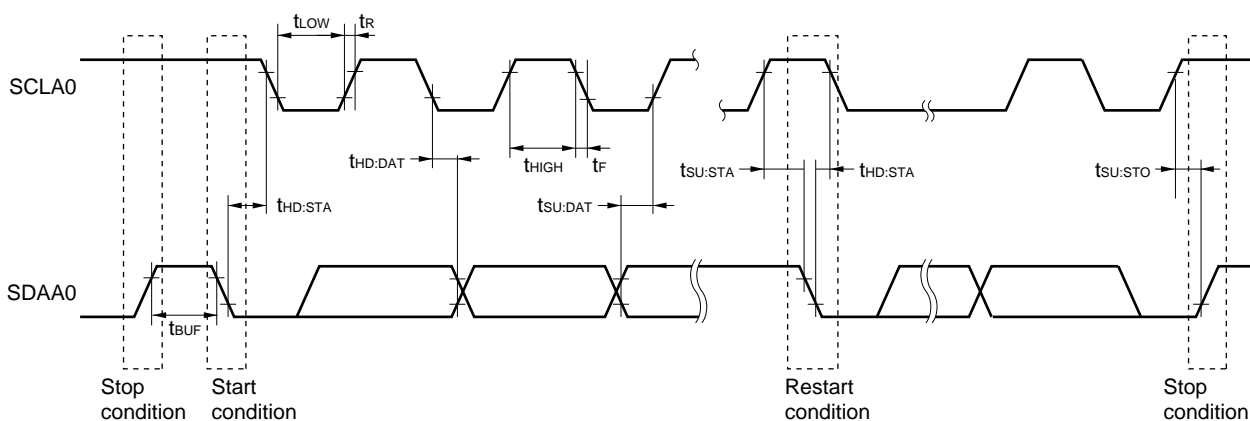
3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0, ANI1	–	See **3.6.1 (2)**.	See **3.6.1 (3)**.
ANI16 to ANI25	See **3.6.1 (1)**.		
Internal reference voltage Temperature sensor output voltage	See **3.6.1 (1)**.		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pins: ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[1]	AINL	10-bit resolution AV_{REFP} = V_{DD}[3]	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI16 to ANI25	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}[3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error[1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}[3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[1]	ILE	10-bit resolution AV_{REFP} = V_{DD}[3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error[1]	DLE	10-bit resolution AV_{REFP} = V_{DD}[3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI25		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))			V_{BGR}[4]		V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))			V_{TMPS25}[4]		V

(**Notes** are listed on the next page.)

(3) When reference voltage (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = V$_{BGR}$[Note 3],
Reference voltage (–) = AV$_{REFM}$[Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$[Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).
   2. This value is indicated as a ratio (%FSR) to the full-scale value.
   3. See **3.6.2 Temperature sensor/internal reference voltage characteristics**.
   4. When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.
   Zero-scale error: Add ±0.35%FSR to the AV$_{REFM}$ MAX. value.
   Integral linearity error: Add ±0.5 LSB to the AV$_{REFM}$ MAX. value.
   Differential linearity error: Add ±0.2 LSB to the AV$_{REFM}$ MAX. value.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference output voltage	V$_{BGR}$	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$				5	μs

		Description	
Rev.	**Date**	**Page**	**Summary**
0.01	Apr 13, 2012	-	First Edition issued
0.02	Oct 31, 2012	-	Change of the number of segment pins • 64-pin products: 36 pins • 80-pin products: 51 pins
2.10	Aug 12, 2016	1	Modification of features of 16-bit timer and 16-bit timer KB20 (IH) in 1.1 Features
		5	Addition of product name (RL78/L13) and description (Top View) in 1.3.1 64-pin products
		6	Addition of product name (RL78/L13) and description (Top View) in 1.3.2 80-pin products
		10	Modification of functional overview of main system clock in 1.6 Outline of Functions
		15	Modification of description in Absolute Maximum Ratings (3/3)
		17, 18	Modification of description in 2.3.1 Pin characteristics
		38	Modification of remark 3 in 2.5.1 (4) During communication at same potential (simplified I^2C mode)
		68	Modification of the title and note, and addition of caution in 2.8 RAM Data Retention Characteristics
		70	Addition of Remark
		74	Modification of description in Absolute Maximum Ratings (T_A = 25 °C) (3/3)
		76	Modification of description in 3.3.1 Pin characteristics
		95	Modification of remark 3 in 3.5.1 (4) During communication at same potential (simplified I^2C mode)
		118	Modification of the title and note, and addition of caution in 3.8 RAM Data Retention Characteristics

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