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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	42
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wlgafb-v0

1.4 Pin Identification

ANI0, ANI1,		PCLBUZ0, PCLBUZ1:	Programmable Clock Output/ Buzzer Output
ANI16 to ANI25:	Analog Input	REGC:	Regulator Capacitance
AVREFM:	Analog Reference Voltage Minus	REMOOUT:	Remote control Output
AVREFP:	Analog Reference Voltage Plus	RESET:	Reset
CAPH, CAPL:	Capacitor for LCD	RTC1HZ:	Real-time Clock 2 Correction Clock (1 Hz) Output
COM0 to COM7:	LCD Common Output	RxD0 to RxD3:	Receive Data
EXCLK:	External Clock Input (Main System Clock)	SCK00, SCK10, SCLA0:	Serial Clock Input/Output
EXCLKS:	External Clock Input (Subsystem Clock)	SCL00, SCL10:	Serial Clock Output
INTP0 to INTP7:	External Interrupt Input	SDAA0, SDA00, SDA10:	Serial Data Input/Output
IVCMP0, IVCMP1:	Comparator Input	SEG0 to SEG50:	LCD Segment Output
IVREF0, IVREF1:	Comparator Reference Input	SI00, SI10:	Serial Data Input
KR0 to KR7:	Key Return	SO00, SO10:	Serial Data Output
P00 to P07:	Port 0	TI00 to TI07:	Timer Input
P10 to P17:	Port 1	TO00 to TO07,	
P20 to P27:	Port 2	TKBO00, TKBO01-0,	
P30 to P35:	Port 3	TKBO01-1, TKBO01-2:	Timer Output
P40 to P47:	Port 4	TOOL0:	Data Input/Output for Tool
P50 to P57:	Port 5	TOOLRxD, TOOLTxD:	Data Input/Output for External Device
P60, P61:	Port 6	TxD0 to TxD3:	Transmit Data
P70 to P77:	Port 7	VCOUT0, VCOUT1:	Comparator Output
P121 to P127:	Port 12	VDD:	Power Supply
P130, P137:	Port 13	VL1 to VL4:	LCD Power Supply
		VSS:	Ground
		X1, X2:	Crystal Oscillator (Main System Clock)
		XT1, XT2:	Crystal Oscillator (Subsystem Clock)

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			20.0 ^{Note 2}	mA
		Per pin for P60 and P61			15.0 ^{Note 2}	mA
		Total of P40 to P47, P130 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		70.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		15.0	mA
			1.8 V ≤ V _{DD} < 2.7 V		9.0	mA
			1.6 V ≤ V _{DD} < 1.8 V		4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V		90.0	mA
			2.7 V ≤ V _{DD} < 4.0 V		35.0	mA
			1.8 V ≤ V _{DD} < 2.7 V		20.0	mA
			1.6 V ≤ V _{DD} < 1.8 V		10.0	mA
		Total of all pins (When duty = 70% ^{Note 3})			160.0	mA
	I _{OL2}	Per pin for P20 and P21			0.4 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		0.8	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

$$\text{Total output current of pins} = (70.0 \times 0.7) / (80 \times 0.01) \cong 61.25 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of real-time clock 2.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.
6. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. **For shift time to the SNOOZE mode, see 21.3.3 SNOOZE mode in the RL78/L13 User's Manual.**
11. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates.
12. Current flowing only to the LCD controller/driver. The value of the current for the RL78 microcontrollers is the sum of the supply current (I_{DD1} or I_{DD2}) and LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}), when the LCD controller/driver operates in operation mode or HALT mode. However, not including the current flowing into the LCD panel. Conditions of the TYP. value and MAX. value are as follows.
 - Setting 20 pins as the segment function and blinking all
 - Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
 - Setting four time slices and 1/3 bias
13. Not including the current flowing into the external division resistor when using the external resistance division method.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

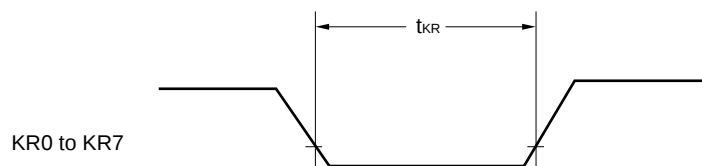
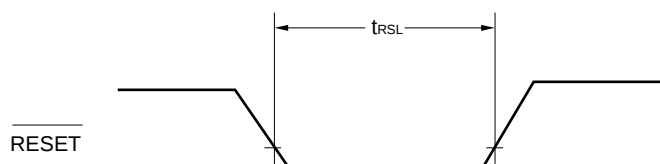
2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
3. f_{CLK}: CPU/peripheral hardware clock frequency
4. The temperature condition for the TYP. value is T_A = 25°C.

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f _{SUB}) operation ^{Note}		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V			1.0		4.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} < 1.8 V			120			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07, TKBO00, TKBO01-0 to TKBO01-2 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			12	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			16	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
			1.6 V ≤ V _{DD} < 1.8 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP7		1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	t _{KRH} , t _{KRL}	KR0 to KR7		1.8 V ≤ V _{DD} ≤ 5.5 V	250			ns
				1.6 V ≤ V _{DD} < 1.8 V	1			μs
IH-PWM output restart input high-level width	t _{IHR}	INTP0 to INTP7			2			f _{CLK}
TMKB2 forced output stop input high-level width	t _{IHR}	INTP0 to INTP2			2			f _{CLK}
RESET low-level width	t _{RSL}				10			μs

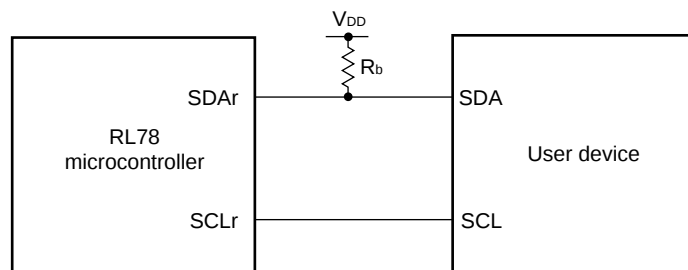
(Note and Remark are listed on the next page.)

Key Interrupt Input Timing **$\overline{\text{RESET}}$ Input Timing**

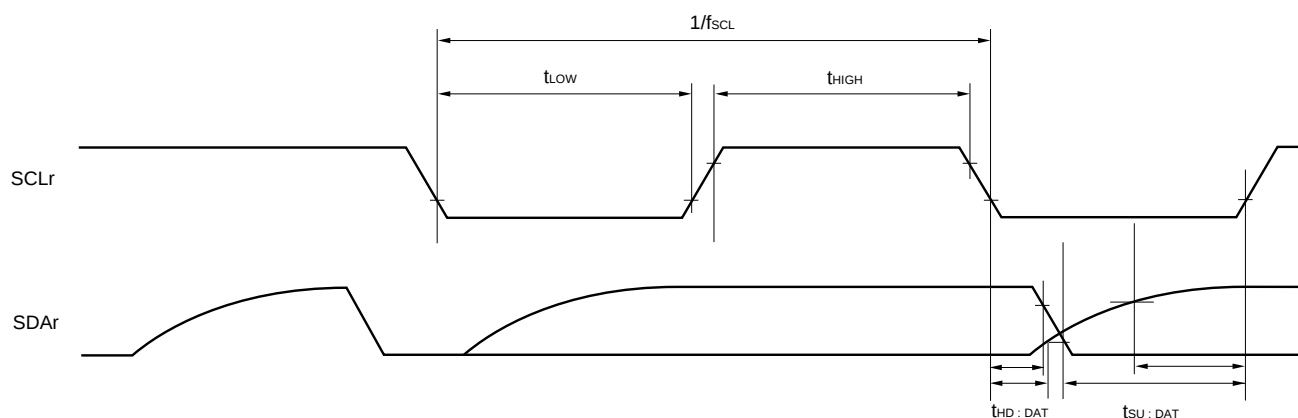
- Notes**
1. The value must also be equal to or less than $f_{MCK}/4$.
 2. Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.
 3. Condition in the HS (high-speed main) mode

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the $SDAr$ pin and the normal output mode for the $SCLr$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- Remarks**
1. $R_b[\Omega]$: Communication line ($SDAr$) pull-up resistance, $C_b[F]$: Communication line ($SDAr$, $SCLr$) load capacitance
 2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

<R>

(2) I²C fast mode(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

3. Condition in HS (high-speed main) mode

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	When power supply rises	3.98	4.06	4.14	V
			When power supply falls	3.90	3.98	4.06	V
		V _{LVD1}	When power supply rises	3.68	3.75	3.82	V
			When power supply falls	3.60	3.67	3.74	V
		V _{LVD2}	When power supply rises	3.07	3.13	3.19	V
			When power supply falls	3.00	3.06	3.12	V
		V _{LVD3}	When power supply rises	2.96	3.02	3.08	V
			When power supply falls	2.90	2.96	3.02	V
		V _{LVD4}	When power supply rises	2.86	2.92	2.97	V
			When power supply falls	2.80	2.86	2.91	V
		V _{LVD5}	When power supply rises	2.76	2.81	2.87	V
			When power supply falls	2.70	2.75	2.81	V
		V _{LVD6}	When power supply rises	2.66	2.71	2.76	V
			When power supply falls	2.60	2.65	2.70	V
		V _{LVD7}	When power supply rises	2.56	2.61	2.66	V
			When power supply falls	2.50	2.55	2.60	V
		V _{LVD8}	When power supply rises	2.45	2.50	2.55	V
			When power supply falls	2.40	2.45	2.50	V
		V _{LVD9}	When power supply rises	2.05	2.09	2.13	V
			When power supply falls	2.00	2.04	2.08	V
		V _{LVD10}	When power supply rises	1.94	1.98	2.02	V
			When power supply falls	1.90	1.94	1.98	V
		V _{LVD11}	When power supply rises	1.84	1.88	1.91	V
			When power supply falls	1.80	1.84	1.87	V
		V _{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
		V _{LVD13}	When power supply rises	1.64	1.67	1.70	V
			When power supply falls	1.60	1.63	1.66	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see 5.4 **System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2		+2	%
		-20 to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1		+1	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	$0.8V_{DD}$	V_{DD}	V
	V_{IH2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.2	V_{DD}	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0	V_{DD}	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	V_{DD}	V
	V_{IH3}	P20, P21	$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60, P61	$0.7V_{DD}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Normal input buffer	0	$0.2V_{DD}$	V
	V_{IL2}	P03, P05, P06, P16, P17, P34, P43, P44, P46, P47, P53, P55	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20, P21	0		$0.3V_{DD}$	V
	V_{IL4}	P60, P61	0		$0.3V_{DD}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the real-time clock 2 is included. The current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 6. The current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Reception			
		4.0 V $\leq V_{DD} \leq 5.5\text{ V}$, 2.7 V $\leq V_b \leq 4.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.7 V $\leq V_{DD} < 4.0\text{ V}$, 2.3 V $\leq V_b \leq 2.7\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.4 V $\leq V_{DD} < 3.3\text{ V}$, 1.6 V $\leq V_b \leq 2.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps

Note Transfer rate in SNOOZE mode is 4800 bps only.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $V_b[\text{V}]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Notes 5. The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq V_{\text{DD}} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

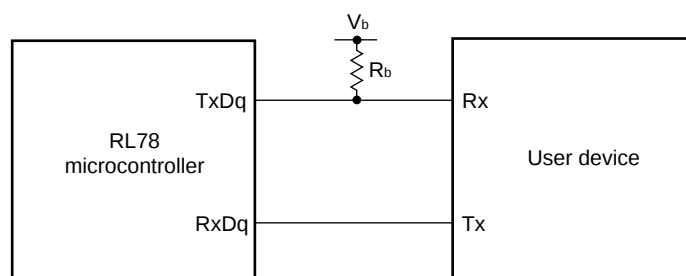
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

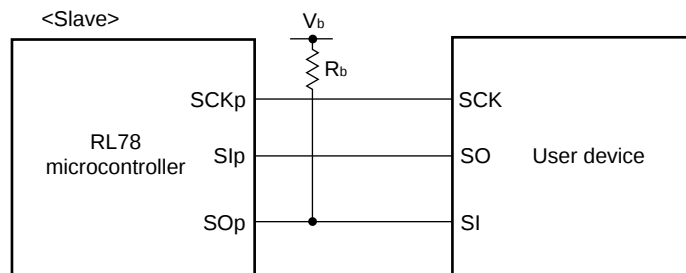
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



CSI mode connection diagram (during communication at different potential)

Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 340^{\text{Note 2}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 340^{\text{Note 2}}$		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	$1/f_{MCK} + 760^{\text{Note 2}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 760^{\text{Note 2}}$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$1/f_{MCK} + 570^{\text{Note 2}}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	0	1215	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

3.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	When power supply rises	3.90	4.06	4.22	V
			When power supply falls	3.83	3.98	4.13	V
		V _{LVD1}	When power supply rises	3.60	3.75	3.90	V
			When power supply falls	3.53	3.67	3.81	V
		V _{LVD2}	When power supply rises	3.01	3.13	3.25	V
			When power supply falls	2.94	3.06	3.18	V
		V _{LVD3}	When power supply rises	2.90	3.02	3.14	V
			When power supply falls	2.85	2.96	3.07	V
		V _{LVD4}	When power supply rises	2.81	2.92	3.03	V
			When power supply falls	2.75	2.86	2.97	V
		V _{LVD5}	When power supply rises	2.71	2.81	2.92	V
			When power supply falls	2.64	2.75	2.86	V
		V _{LVD6}	When power supply rises	2.61	2.71	2.81	V
			When power supply falls	2.55	2.65	2.75	V
		V _{LVD7}	When power supply rises	2.51	2.61	2.71	V
			When power supply falls	2.45	2.55	2.65	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode $(T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.6 Supply voltage rise time

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 LCD Characteristics

3.7.1 External resistance division method

(1) Static display mode

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μF	2 VL1 – 0.10	2 VL1	2 VL1	V	
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 μF	3 VL1 – 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GNDC1 = C2 = C3 = C4 = $0.47\text{ }\mu\text{F} \pm 30\%$

- 2.** This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- 3.** This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

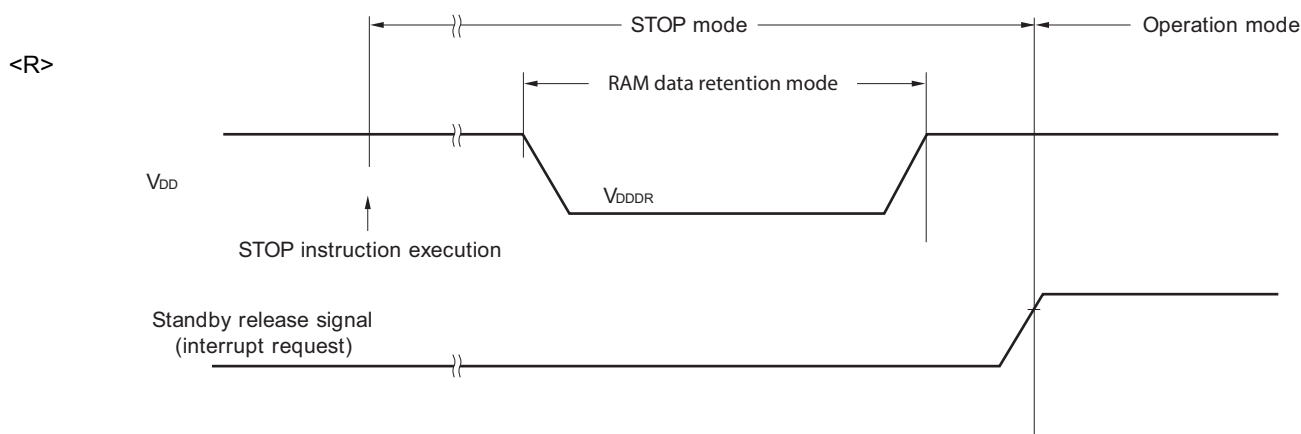
3.8 RAM Data Retention Characteristics

<R>

 $(T_A = -40$ to $+105^\circ\text{C})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.9 Flash Memory Programming Characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}	2.4 V ≤ V _{DD} ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Note 1, 2, 3}	C _{erwr}	Retained for 20 years T _A = 85°C ^{Note 4}	1,000			Times
Number of data flash rewrites ^{Note 1, 2, 3}		Retained for 1 year T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C ^{Note 4}	100,000			
		Retained for 20 years T _A = 85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. This temperature is the average value at which data are retained.

Remark When updating data multiple times, use the flash memory as one for updating data.

3.10 Dedicated Flash Memory Programmer Communication (UART)

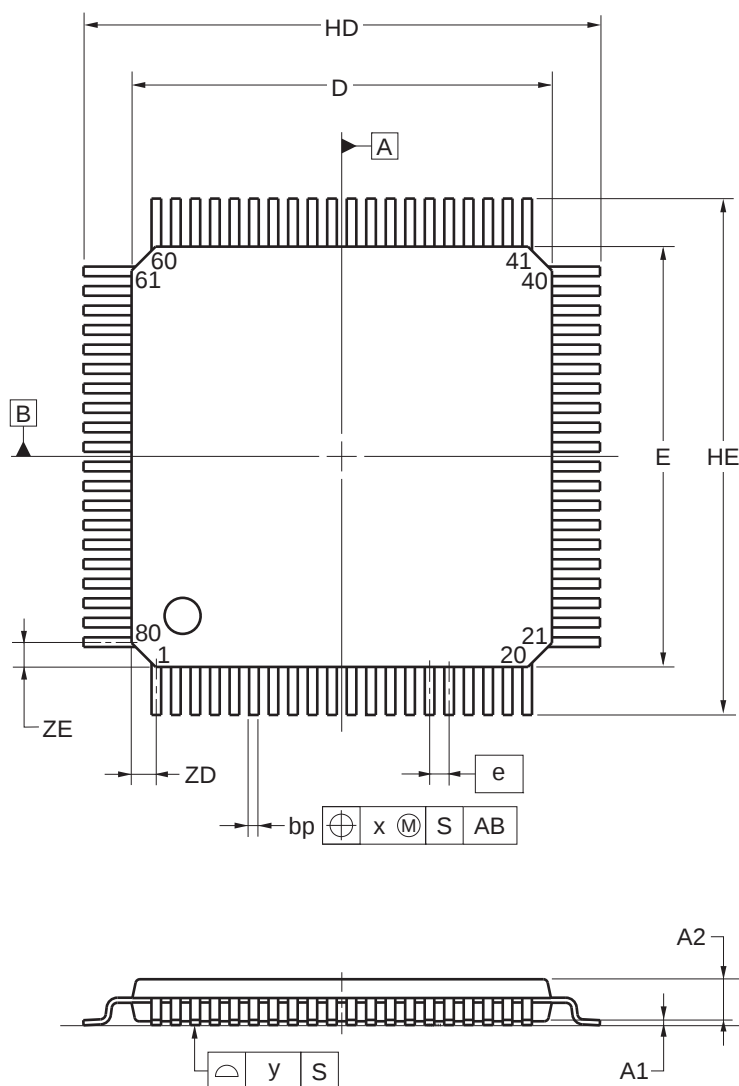
 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.2 80-pin Products

R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA, R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—