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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmaafa-x0

Pin Count	Package	Data Flash	Fields of Application[Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F10WLAAFA#30, R5F10WLAAFA#50, R5F10WLCAFA#30, R5F10WLCAFA#50, R5F10WLDAFA#30, R5F10WLDAFA#50, R5F10WLEAFA#30, R5F10WLEAFA#50, R5F10WLFAFA#30, R5F10WLFAFA#50, R5F10WLGAFA#30, R5F10WLGAFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A	R5F10WLAAFB#30, R5F10WLAAFB#50, R5F10WLCAFB#30, R5F10WLCAFB#50, R5F10WLDAFB#30, R5F10WLDAFB#50, R5F10WLEAFB#30, R5F10WLEAFB#50, R5F10WLFAFB#30, R5F10WLFAFB#50, R5F10WLGAFB#30, R5F10WLGAFB#50,
			G	R5F10WLAGFB#30, R5F10WLAGFB#50, R5F10WLCGFB#30, R5F10WLCGFB#50, R5F10WLDGFB#30, R5F10WLDGFB#50, R5F10WLEGFB#30, R5F10WLEGFB#50, R5F10WLFGFB#30, R5F10WLFGFB#50, R5F10WLGGFB#30, R5F10WLGGFB#50
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F10WMAAFA#30, R5F10WMAAFA#50, R5F10WMCAFA#30, R5F10WMCAFA#50, R5F10WMDAFA#30, R5F10WMDAFA#50, R5F10WMEAFA#30, R5F10WMEAFA#50, R5F10WMFAFA#30, R5F10WMFAFA#50, R5F10WMGAFA#30, R5F10WMGAFA#50
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F10WMAAFB#30, R5F10WMAAFB#50, R5F10WMCAFB#30, R5F10WMCAFB#50, R5F10WMDAFB#30, R5F10WMDAFB#50, R5F10WMEAFB#30, R5F10WMEAFB#50, R5F10WMFAFB#30, R5F10WMFAFB#50, R5F10WMGAFB#30, R5F10WMGAFB#50,
			G	R5F10WMAGFB#30, R5F10WMAGFB#50, R5F10WMCGFB#30, R5F10WMCGFB#50, R5F10WMDGFB#30, R5F10WMDGFB#50, R5F10WMEGFB#30, R5F10WMEGFB#50, R5F10WMFGFB#30, R5F10WMFGFB#50, R5F10WMGGFB#30, R5F10WMGGFB#50

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/L13.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.6 Outline of Functions

(1/2)

Item		64-pin	80-pin
		R5F10WLx (x = A, C-G)	R5F10WMx (x = A, C-G)
Code flash memory (KB)		16 to 128	16 to 128
Data flash memory (KB)		4	4
RAM (KB)		1 to 8[Note 1]	1 to 8[Note 1]
Address space		1 MB	
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Clock for 16-bit timer KB20		48 MHz (TYP.): V_{DD} = 2.7 to 5.5 V	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.6 to 5.5 V	
Low-speed on-chip oscillator		15 kHz (TYP.)	
General-purpose register		(8-bit register × 8) × 4 banks	
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f_{IH} = 24 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	49	65
	CMOS I/O	42 (N-ch O.D. I/O [V_{DD} withstand voltage]: 12)	58 (N-ch O.D. I/O [V_{DD} withstand voltage]: 18)
	CMOS input	5	5
	CMOS output	–	–
	N-ch O.D I/O (withstand voltage: 6 V)	2	2
Timer	16-bit timer TAU	8 channels	
	16-bit timer KB20	1 channel	
	Watchdog timer	1 channel	
	12-bit interval timer (IT)	1 channel	
	Real-time clock 2	1 channel	
	RTC2 output	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	
	Timer output	8 channels (PWM outputs: 7[Note 2]) (TAU used) 1 channel (timer KB20 used)	
	Remote control output function	1 (TAU used)	

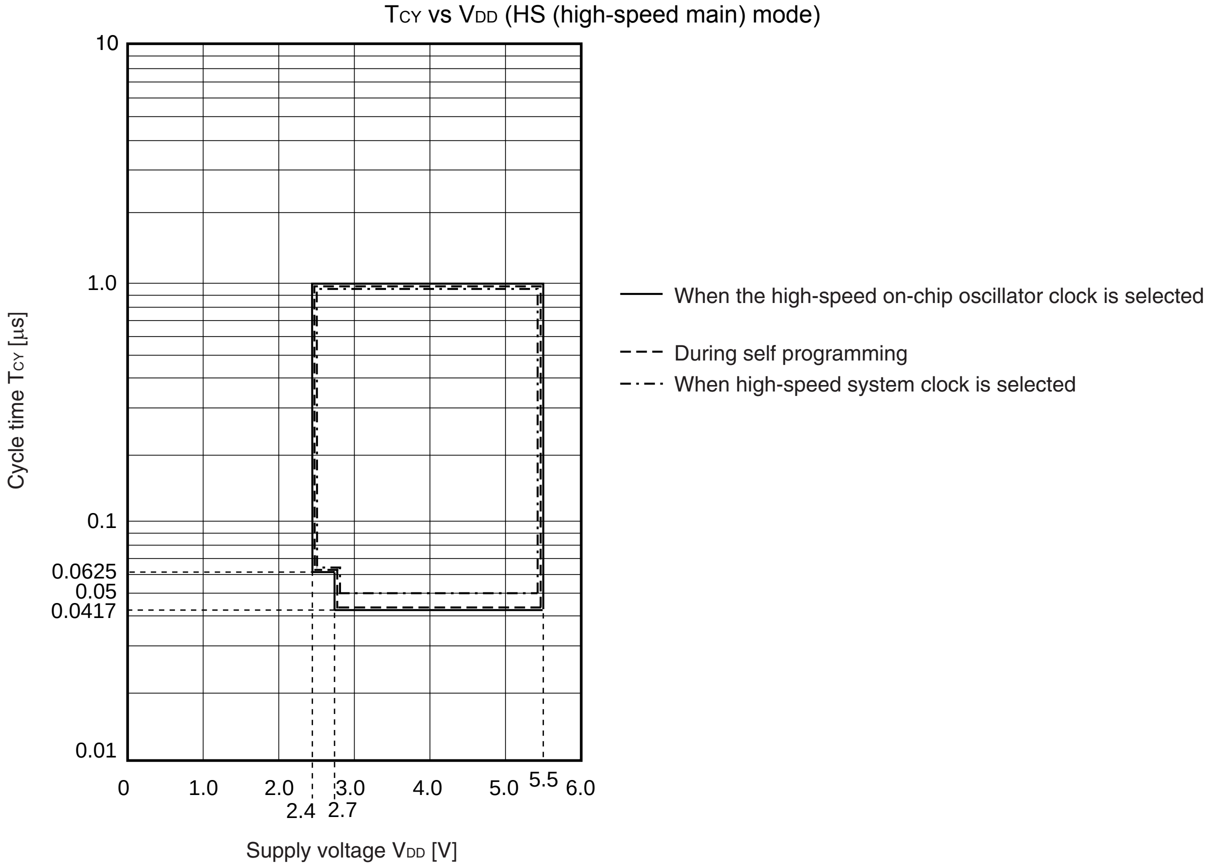
Notes 1. In the case of the 8 KB, this is about 7 KB when the self-programming function and data flash function are used.

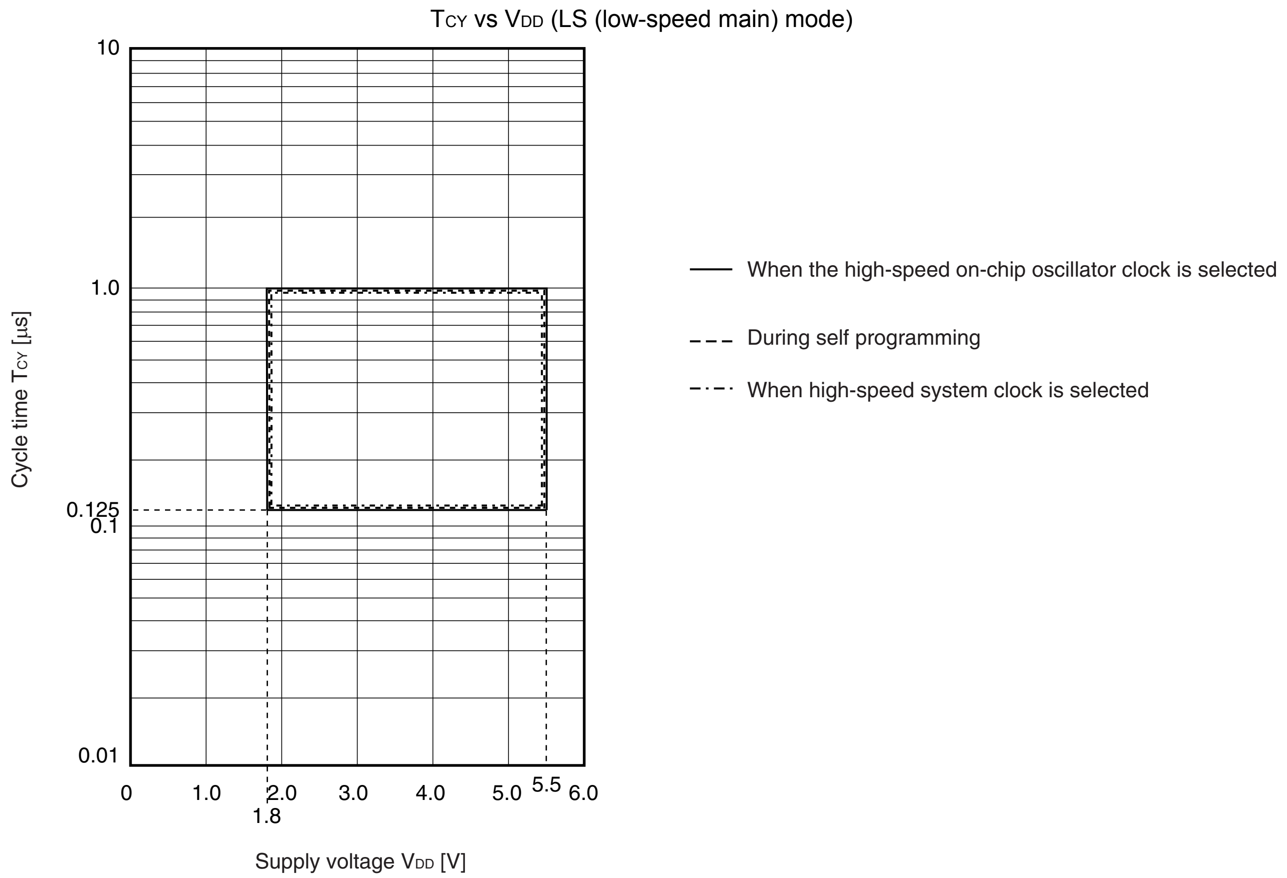
2. The number of outputs varies depending on the setting of the channels in use and the number of master channels (see **6.9.3 Operation as multiple PWM output function** in the RL78/L13 User's Manual.).

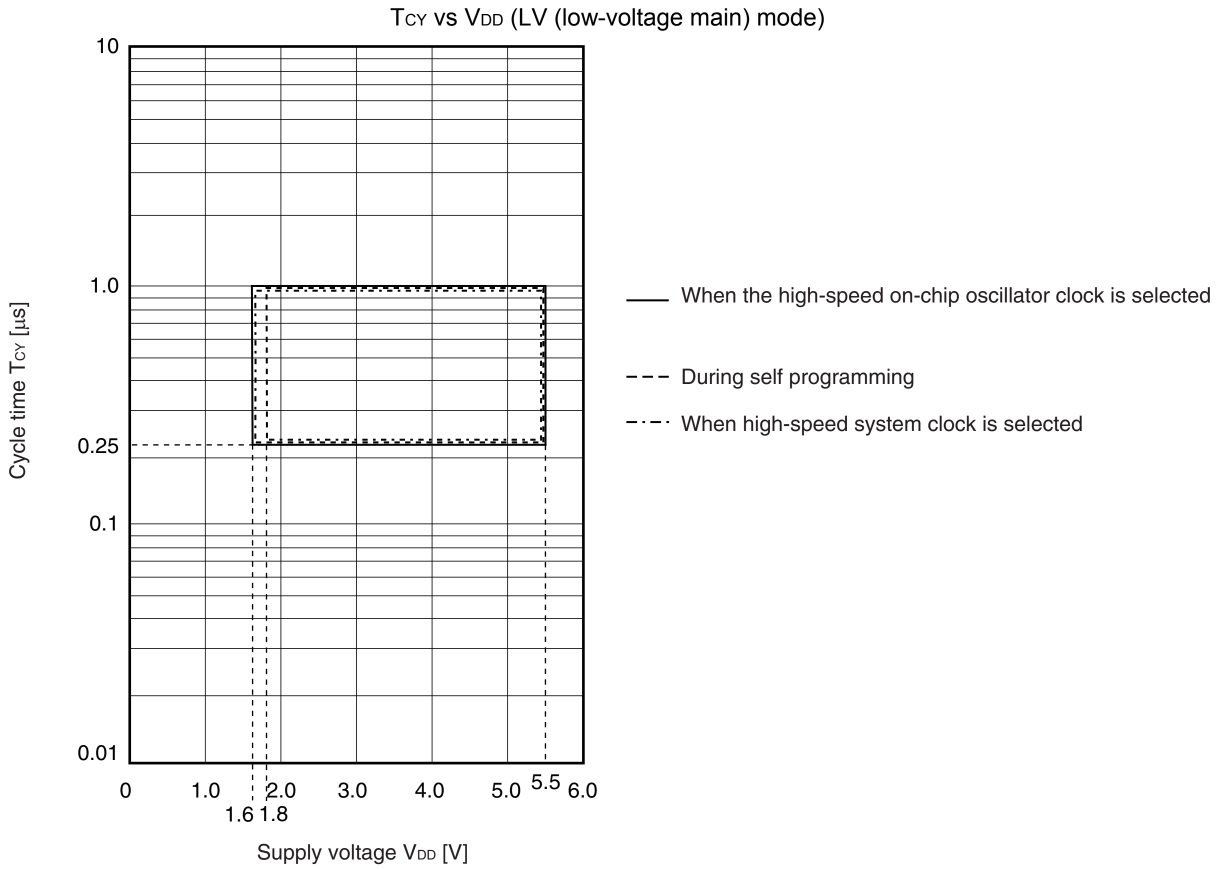
Note Operation is not possible if 1.6 V ≤ V_{DD} < 1.8 V in LV (low-voltage main) mode while the system is operating on the subsystem clock.

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)
m: Unit number (m = 0), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation




TCY vs VDD (LS (low-speed main) mode)
Cycle time TCY [µs]
10
1.0
0.125
0.1
0.01
0
1.0
2.0
3.0
4.0
5.0
5.5
6.0
1.8
Supply voltage VDD [V]
When the high-speed on-chip oscillator clock is selected
During self programming
When high-speed system clock is selected


TCY vs VDD (LV (low-voltage main) mode)
Cycle time TCY [µs]
10
1.0
0.25
0.1
0.01
0
1.0
2.0
3.0
4.0
5.0
5.5
6.0
1.6
1.8
Supply voltage VDD [V]
When the high-speed on-chip oscillator clock is selected
During self programming
When high-speed system clock is selected

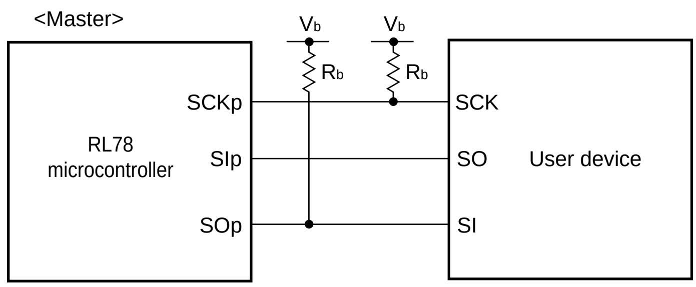
(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓)[Note 4]	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V (2.4 V[Note 1]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓)[Note 4]	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V (2.4 V[Note 1]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output[Note 4]	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V (2.4 V[Note 1]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Notes **1.** Condition in HS (high-speed main) mode
2. Use it with V_{DD} ≥ V_b.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
4. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Notes **1.** Transfer rate in SNOOZE mode: MAX. 1 Mbps

2. Condition in HS (high-speed main) mode

3. Use it with $V_{DD} \geq V_b$.

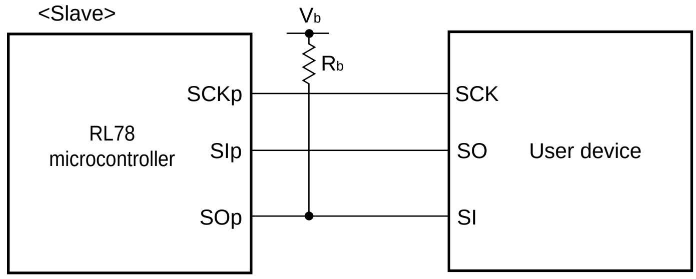
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



(3) I²C fast mode plus

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	–		–		kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		µs
Hold time when SCLA0 ="L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		–		–		µs
Hold time when SCLA0 ="H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		–		–		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	–		–		µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		–		–		µs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

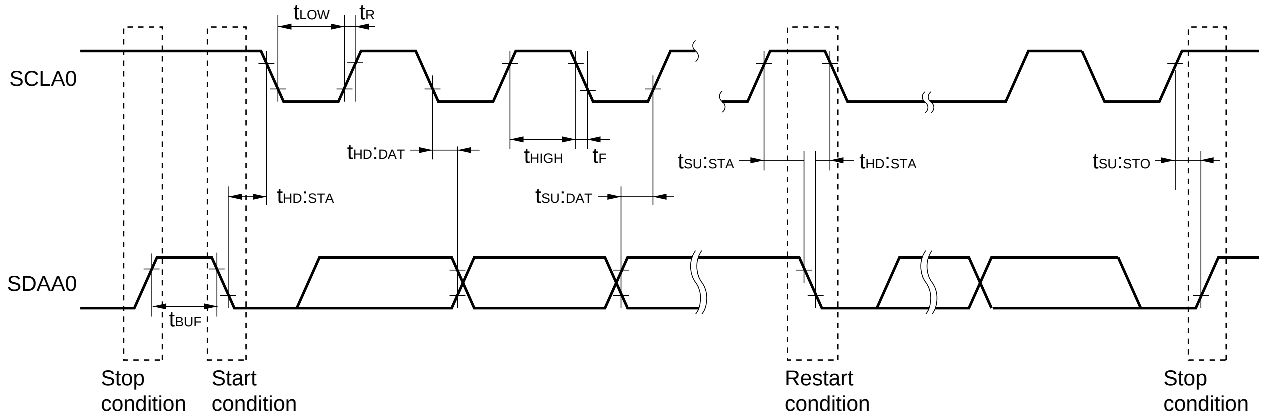
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the AV_{REFM} MAX. value.

Integral linearity error: Add ±0.5 LSB to the AV_{REFM} MAX. value.

Differential linearity error: Add ±0.2 LSB to the AV_{REFM} MAX. value.

2.6.2 Temperature sensor /internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register = 80H, T_A = +25°C		1.05		V
Internal reference output voltage	V_{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}				5	μs

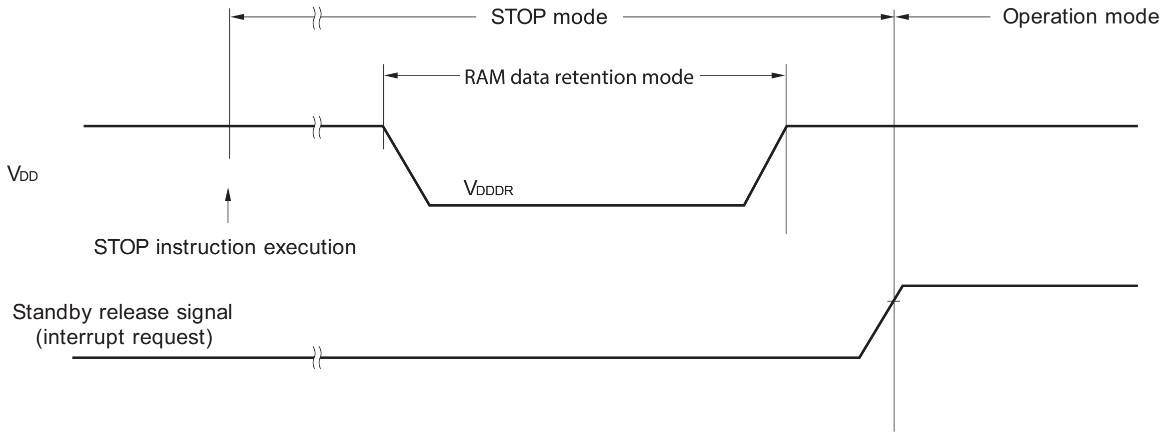
<R> 2.8 RAM Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

<R> **Caution Data in RAM are not retained if the CPU operates outside the specified operating voltage range. Therefore, place the CPU in STOP mode before the operating voltage drops below the specified range.**



2.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V	1		24	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

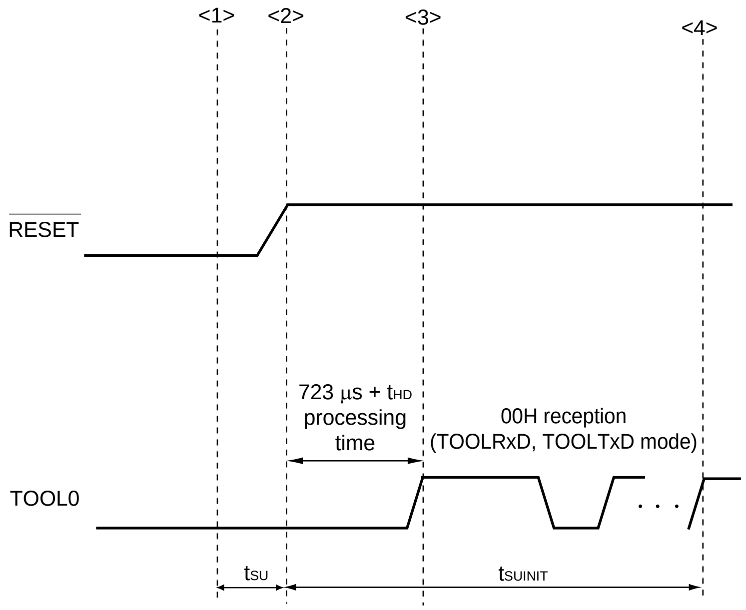
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.11 Timing Specifications for Switching Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and completion the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = –40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T_A = –40 to +105°C

R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB,
R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB
R5F10WMAGFB, R5F10WMCGFB, R5F10WMDGFB,
R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

Cautions 1. The RL78/L13 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L13 User's Manual.

3. Consult Renesas salesperson and distributor for derating when the product is used at T_A = +85°C to +105°C. Note that derating means "systematically lowering the load from the rated value to improve reliability".

<R> **Remark** When RL78/L13 is used in the range of T_A = -40 to +85°C, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)**.

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT})[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to +105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–2		+2	%
		–20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1		+1	%
		–40 to –20°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of real-time clock 2.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The value of the current for the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

6. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **21.3.3 SNOOZE mode** in the RL78/L13 User's Manual.

11. Current flowing only to the comparator circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator circuit operates.

12. Current flowing only to the LCD controller/driver. The value of the current for the RL78 microcontrollers is the sum of the supply current (I_{DD1} or I_{DD2}) and LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}), when the LCD controller/driver operates in operation mode or HALT mode. However, not including the current flowing into the LCD panel. Conditions of the TYP. value and MAX. value are as follows.

- Setting 20 pins as the segment function and blinking all
- Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
- Setting four time slices and 1/3 bias

13. Not including the current flowing into the external division resistor when using the external resistance division method.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

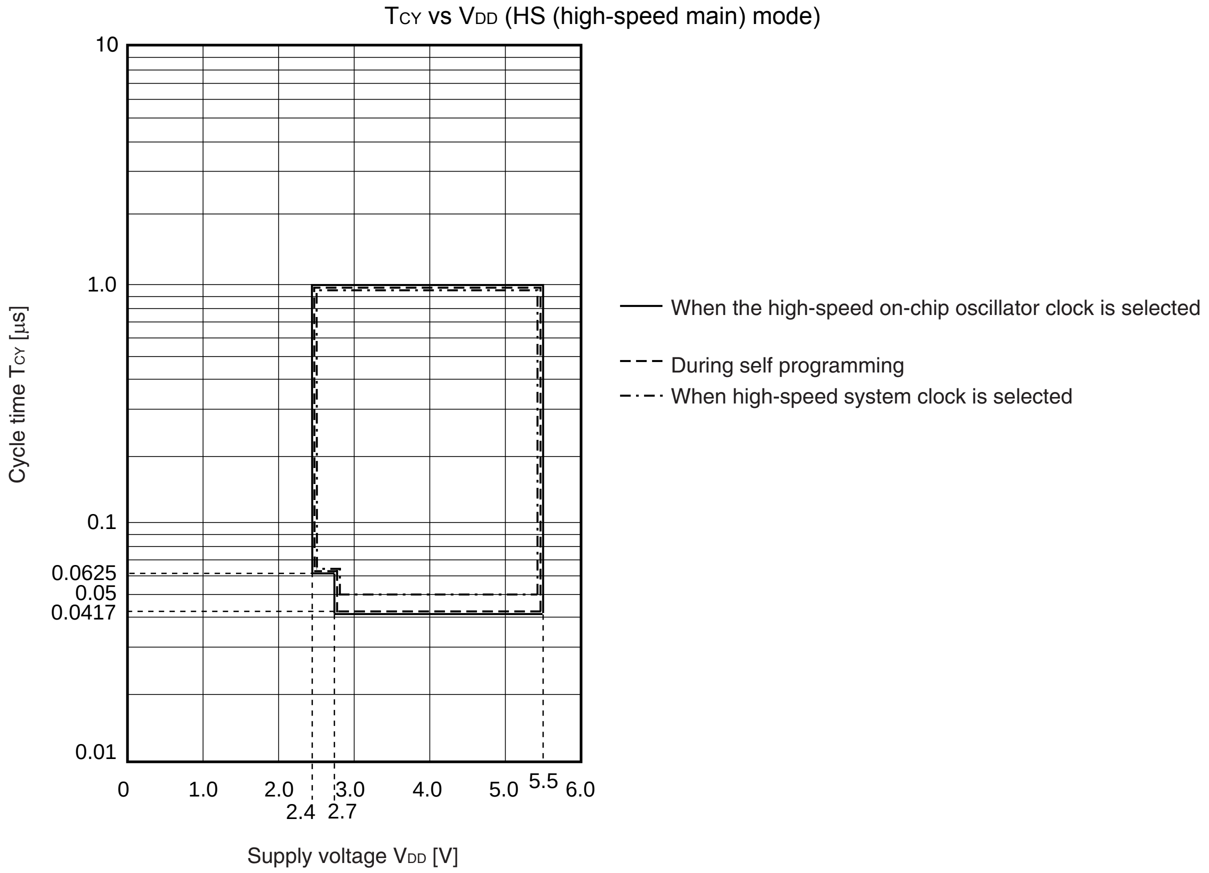
3. f_{CLK}: CPU/peripheral hardware clock frequency

4. The temperature condition for the TYP. value is T_A = 25°C.

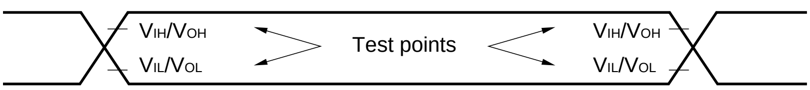
Note Specification under conditions where the duty factor is 50%.

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn)
m: Unit number (m = 0), n: Channel number (n = 0 to 7))

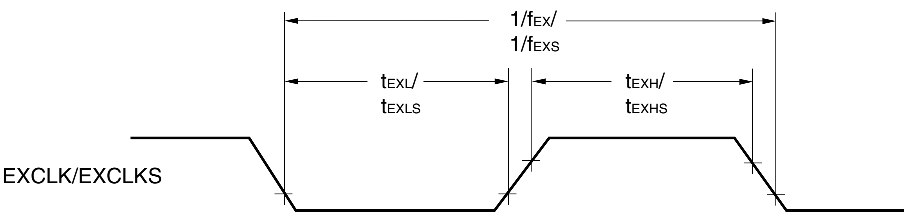
Minimum Instruction Execution Time during Main System Clock Operation



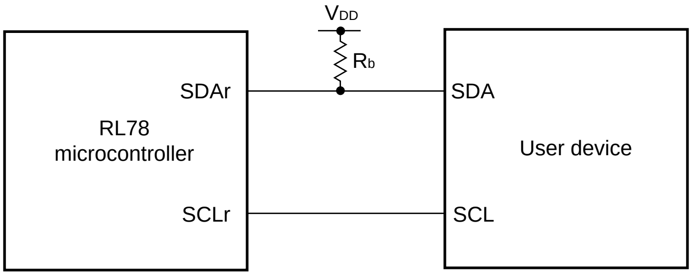
AC Timing Test Points



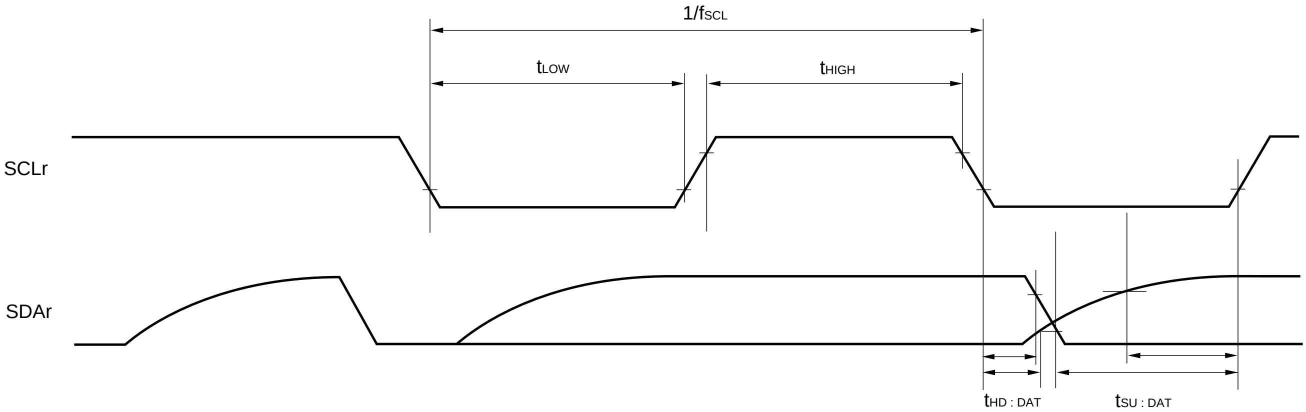
External System Clock Timing



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)

<R> **3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.0 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

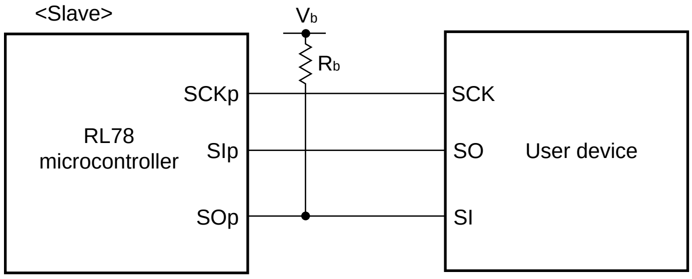
$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

CSI mode connection diagram (during communication at different potential)



Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps

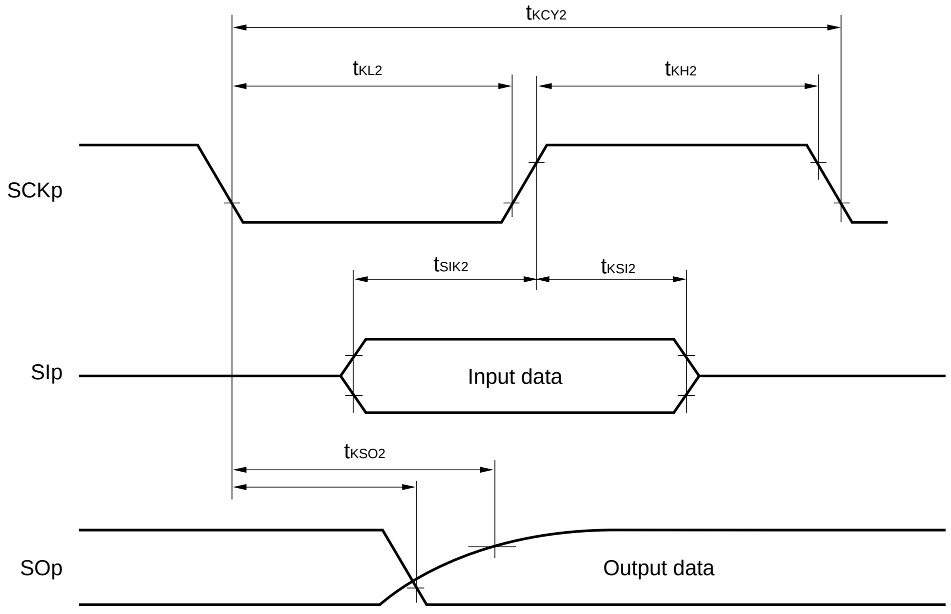
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

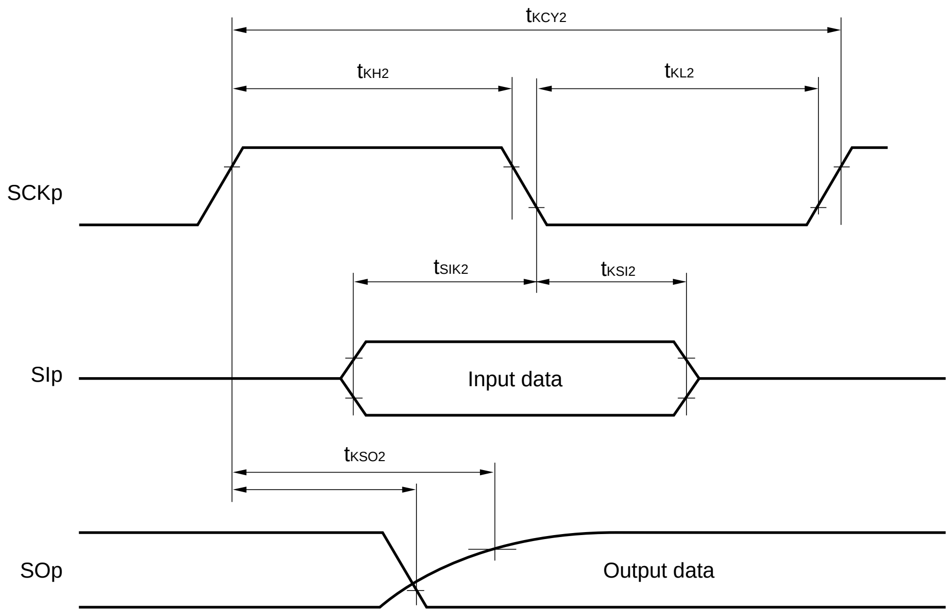
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

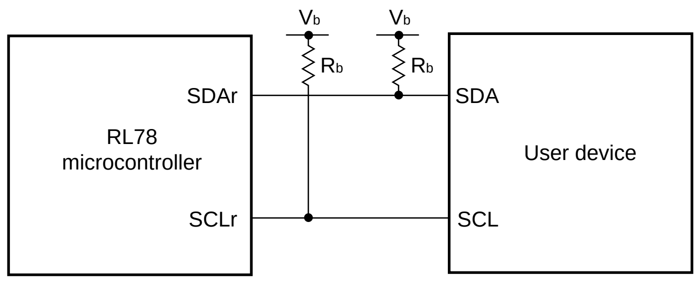


Remarks 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

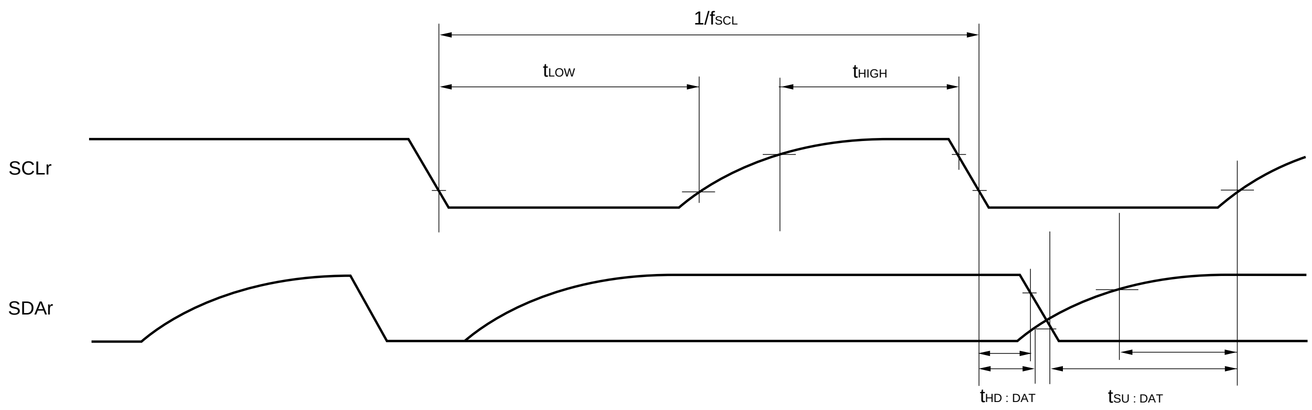
2. p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn) m: Unit number, n: Channel number (mn = 00, 02))

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remarks 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02)

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4[Note 1] = 0.47 μF[Note 2]	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4[Note 1] = 0.47 μF		2 V_{L1} – 0.10	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4[Note 1] = 0.47 μF		3 V_{L1} – 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF ± 30%

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).