



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

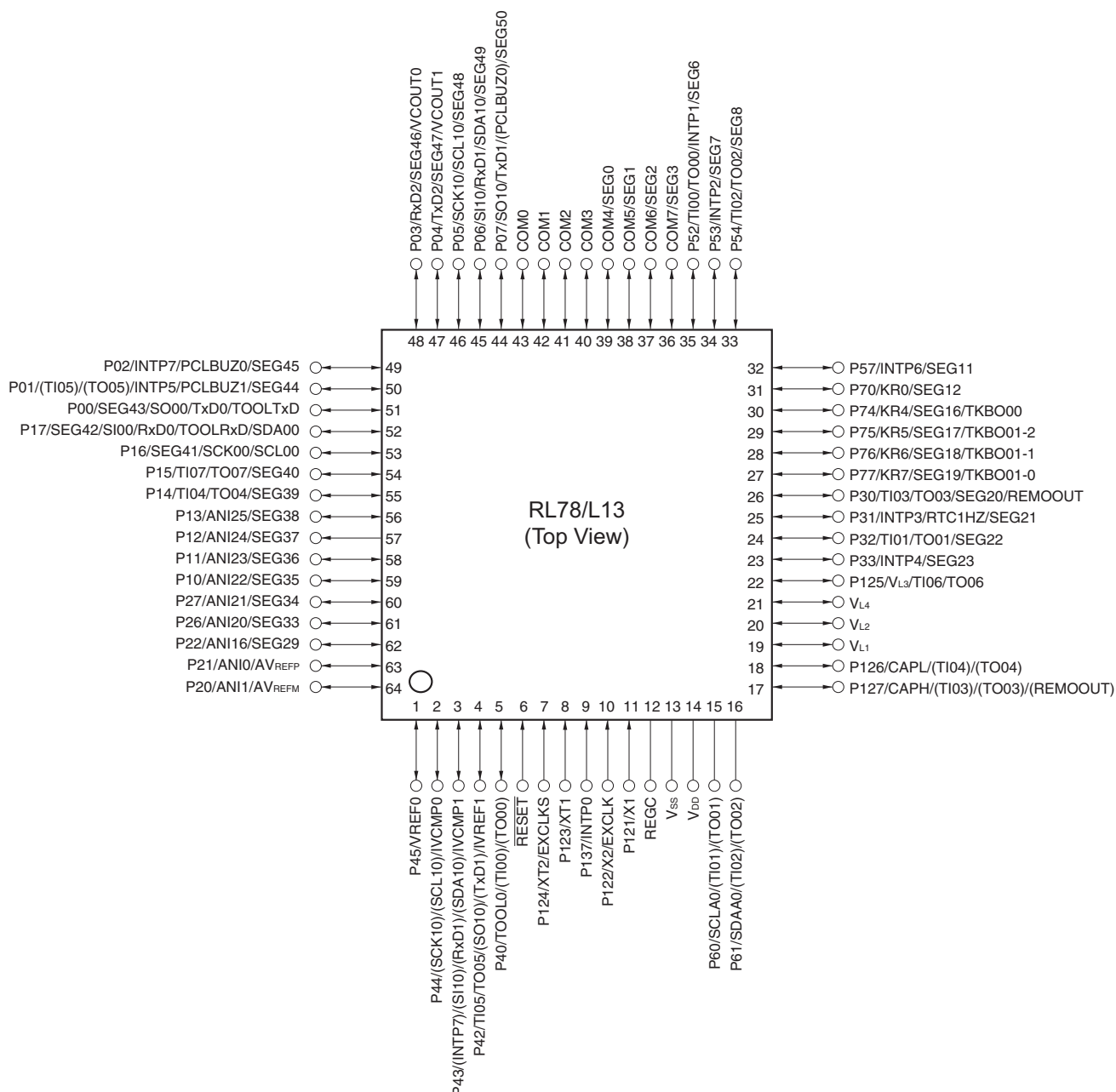
Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmaafb-30

1.3 Pin Configuration (Top View)

<R> 1.3.1 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 and P61 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI0, ANI1, ANI16 to ANI26	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to $1\ \mu\text{F}$). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be $6.5\ \text{V}$ or lower.

3. Do not exceed $AV_{REF(+)} + 0.3\ \text{V}$ in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF (+)}$: + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{HOCO} = 48 MHz ^{Note 3} , f _{IH} = 24 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V	2.0		mA
						V _{DD} = 3.0 V	2.0		mA
					Normal operation	V _{DD} = 5.0 V	3.8	6.5	mA
						V _{DD} = 3.0 V	3.8	6.5	mA
				f _{HOCO} = 24 MHz ^{Note 3} , f _{IH} = 24 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V	1.7		mA
						V _{DD} = 3.0 V	1.7		mA
					Normal operation	V _{DD} = 5.0 V	3.6	6.1	mA
						V _{DD} = 3.0 V	3.6	6.1	mA
				f _{HOCO} = 16 MHz ^{Note 3} , f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V	2.7	4.7	mA
						V _{DD} = 3.0 V	2.7	4.7	mA
			LS (low-speed main) mode ^{Note 5}	f _{HOCO} = 8 MHz ^{Note 3} , f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V	1.2	2.1	mA
						V _{DD} = 2.0 V	1.2	2.1	mA
			LV (low-voltage main) mode ^{Note 5}	f _{HOCO} = 4 MHz ^{Note 3} , f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V	1.2	1.8	mA
						V _{DD} = 2.0 V	1.2	1.8	mA
			HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input	3.0	5.1	mA
						Resonator connection	3.2	5.2	mA
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input	2.9	5.1	mA
						Resonator connection	3.2	5.2	mA
				f _{MX} = 16 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				f _{MX} = 16 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
			LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
				f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} , T _A = -40°C	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +25°C	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +50°C	Normal operation	Square wave input	4.1	7.1	μA
						Resonator connection	4.4	7.1	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +70°C	Normal operation	Square wave input	4.3	8.7	μA
						Resonator connection	4.7	8.7	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +85°C	Normal operation	Square wave input	4.7	12.0	μA
						Resonator connection	5.2	12.0	μA

(Notes and Remarks are listed on the next page.)

2.4 AC Characteristics

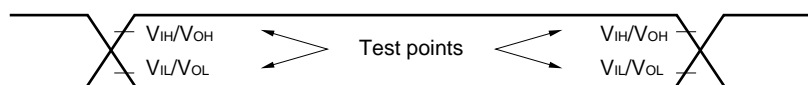
(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f _{SUB}) operation ^{Note}		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V			1.0		4.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} < 1.8 V			120			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}				1/f _{MCK} +10			ns
TO00 to TO07, TKBO00, TKBO01-0 to TKBO01-2 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			12	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ V _{DD} ≤ 5.5 V			16	MHz	
			2.7 V ≤ V _{DD} < 4.0 V			8	MHz	
			2.4 V ≤ V _{DD} < 2.7 V			4	MHz	
		LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
			1.6 V ≤ V _{DD} < 1.8 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V			4	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0 to INTP7		1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	t _{KRH} , t _{KRL}	KR0 to KR7		1.8 V ≤ V _{DD} ≤ 5.5 V	250			ns
				1.6 V ≤ V _{DD} < 1.8 V	1			μs
IH-PWM output restart input high-level width	t _{IHR}	INTP0 to INTP7			2			f _{CLK}
TMKB2 forced output stop input high-level width	t _{IHR}	INTP0 to INTP2			2			f _{CLK}
RESET low-level width	t _{RSL}				10			μs

(Note and Remark are listed on the next page.)

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate ^{Note 1}		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		4.0		1.3		0.6	Mbps
		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		—		1.3		0.6	Mbps
		$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		—		—		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		—		—		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

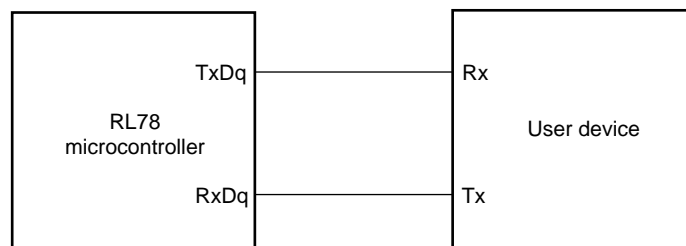
HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Trans mission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V)			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V)			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			1.8 V (2.4 V ^{Note 8}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V)			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Use it with V_{DD} ≥ V_b.

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ($2.4\text{ V}^{\text{Note 8}}$) $\leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

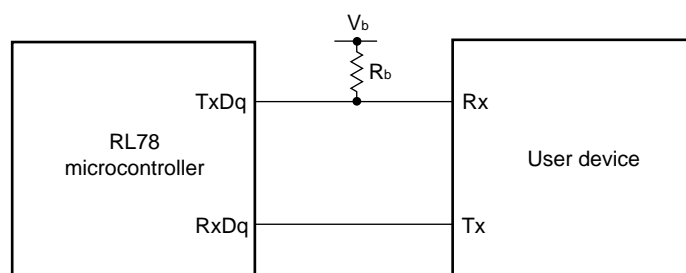
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.
8. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



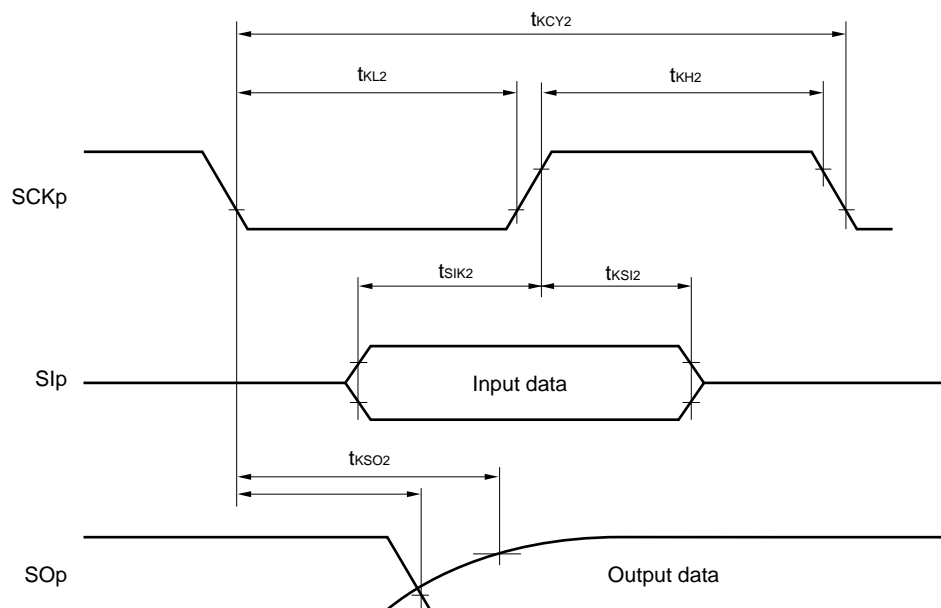
(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

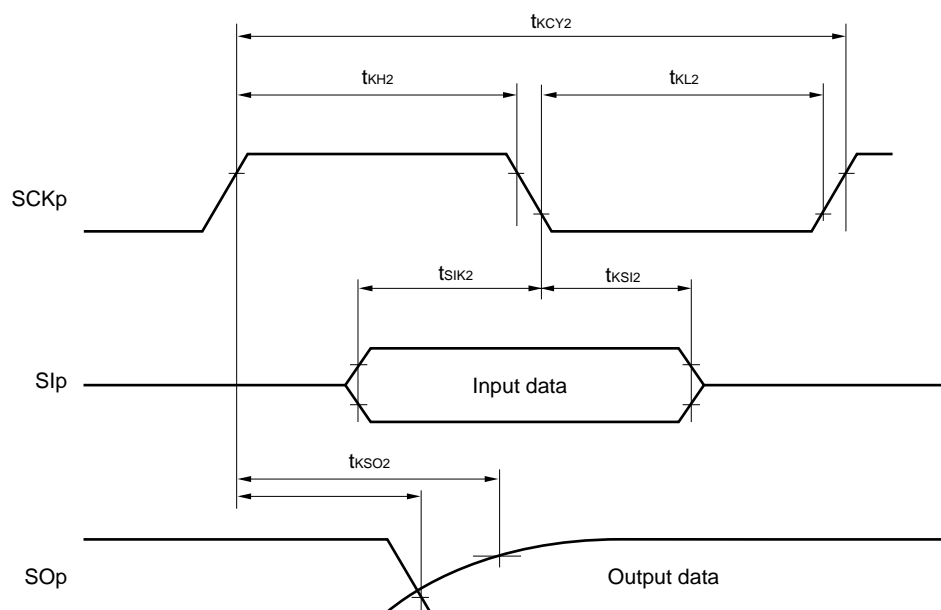
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		200		1150		1150		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		121		479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOP output ^{Note 1}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130		130		130	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		33		110		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOP output ^{Note 2}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			10		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- 2.** p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn)
 m: Unit number, n: Channel number (mn = 00, 02))

(1) I²C standard mode (2/2)(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V	250		250		250		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	250		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	0	3.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ V _{DD} ≤ 5.5 V	—	—	—	—	4.7		μs

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.
 3. Condition in HS (high-speed main) mode

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3},
Reference voltage (-) = AVREFM^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the AVREFM MAX. value.

Integral linearity error: Add ±0.5 LSB to the AVREFM MAX. value.

Differential linearity error: Add ±0.2 LSB to the AVREFM MAX. value.

2.6.2 Temperature sensor /internal reference voltage characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMPS25}	ADS register = 80H, T _A = +25°C		1.05		V
Internal reference output voltage	V _{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t _{AMP}				5	μs

(2) 1/4 bias method**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} −0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} −0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} −0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = C5 = 0.47\text{ }\mu\text{F} \pm 30\%$

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.7.3 Capacitor split method**(1) 1/3 bias method****($T_A = -40$ to $+85^\circ\text{C}$, $2.2\text{ V} \leq V_D \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}	$\frac{2}{3} V_{L4} - 0.1$	$\frac{2}{3} V_{L4}$	$\frac{2}{3} V_{L4} + 0.1$	V
V_{L1} voltage	V_{L1}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}	$\frac{1}{3} V_{L4} - 0.1$	$\frac{1}{3} V_{L4}$	$\frac{1}{3} V_{L4} + 0.1$	V
Capacitor split wait time ^{Note 1}	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = 0.47\text{ }\mu\text{F} \pm 30\%$

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-3.0 ^{Note 2}	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130			-45.0	mA
		(When duty = 70% ^{Note 3})			-15.0	mA
					-7.0	mA
	I _{OH2}	Per pin for P20 and P21			-0.1 ^{Note 2}	mA
		Total of all pins (When duty = 70% ^{Note 3})			-0.2	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).

- Total output current of pins = $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OH} = -45.0\text{ mA}$

$$\text{Total output current of pins} = (-45.0 \times 0.7)/(80 \times 0.01) = -39.375\text{ mA}$$

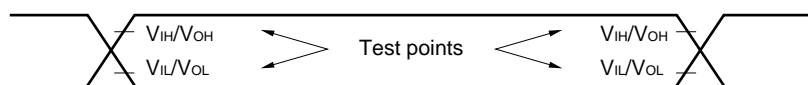
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

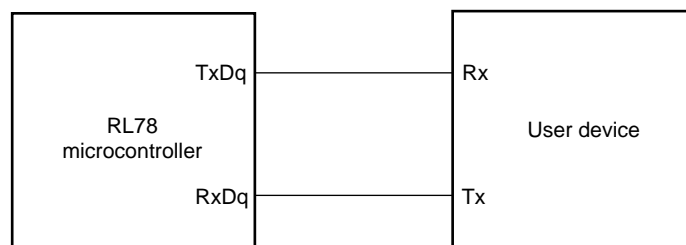
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate ^{Note}				$f_{MCK}/12$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps

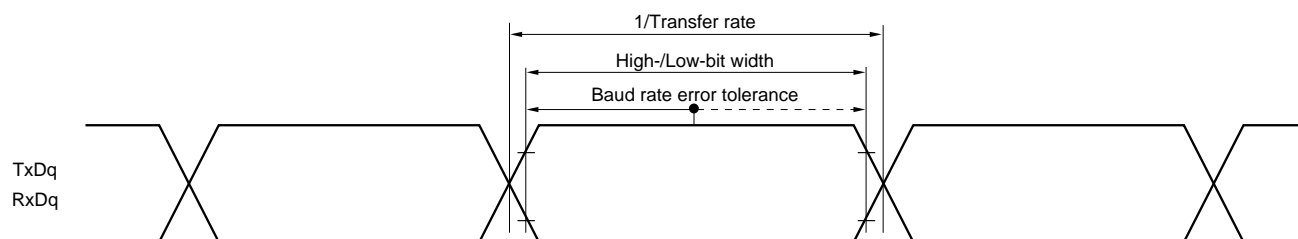
Note Transfer rate in the SNOOZE mode is 4800 bps only.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



- Remarks**
1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334 ^{Note 1}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500 ^{Note 1}		ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 76$		ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{KSI1}		38		ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}		50	ns

Notes 1. The value must also be equal to or more than $4/f_{CLK}$.**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**5.** C is the load capacitance of the SCKp and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM and POM numbers (g = 0, 1)**2.** f_{MCK} : Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V	2.0 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V	1.2 ^{Note 4}	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

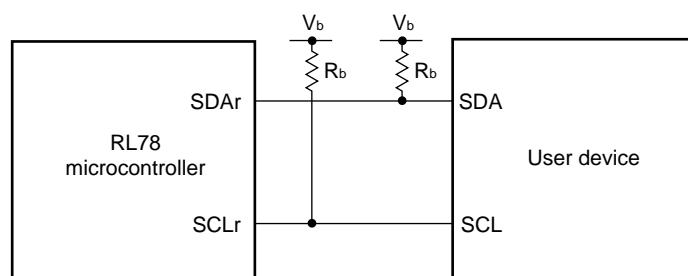
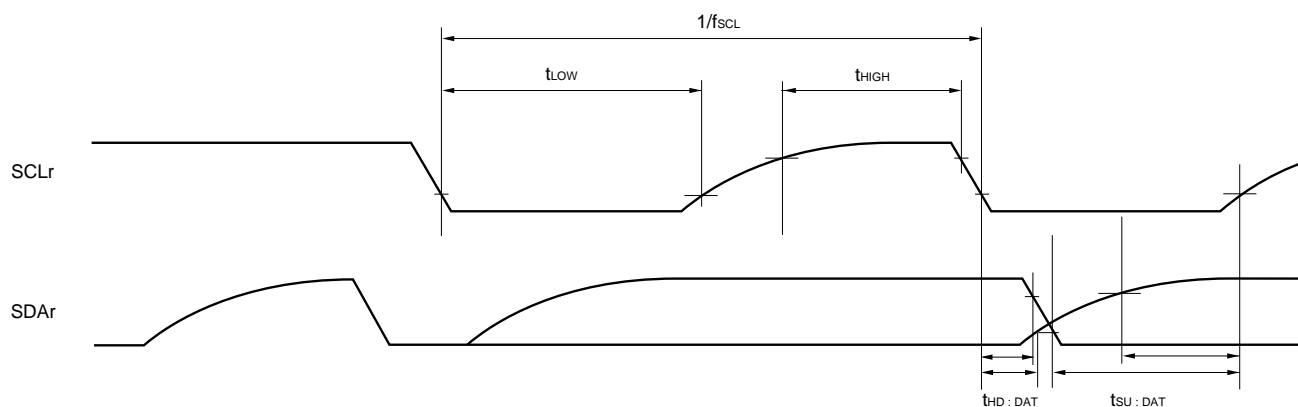
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

(2) 1/4 bias method**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} – 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} – 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} – 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = C5 = 0.47\text{ }\mu\text{F} \pm 30\%$

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.7.3 Capacitor split method**(1) 1/3 bias method****($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_D \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}	$\frac{2}{3} V_{L4} - 0.1$	$\frac{2}{3} V_{L4}$	$\frac{2}{3} V_{L4} + 0.1$	V
V_{L1} voltage	V_{L1}	C1 to C4 = $0.47\text{ }\mu\text{F}$ ^{Note 2}	$\frac{1}{3} V_{L4} - 0.1$	$\frac{1}{3} V_{L4}$	$\frac{1}{3} V_{L4} + 0.1$	V
Capacitor split wait time ^{Note 1}	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = 0.47\text{ }\mu\text{F} \pm 30\%$

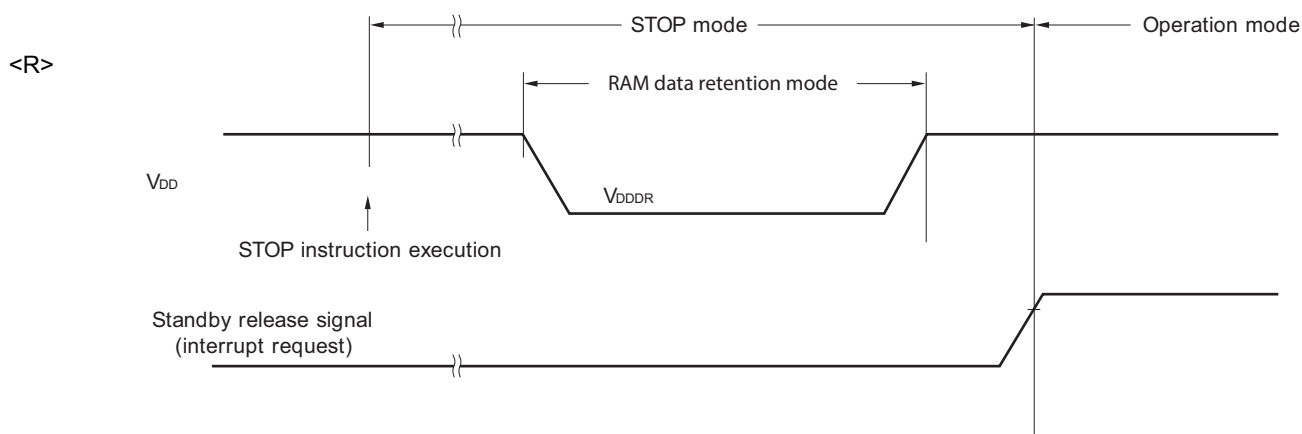
3.8 RAM Data Retention Characteristics

<R>

($T_A = -40$ to $+105^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.9 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Note 1, 2, 3}	Cenwr	Retained for 20 years TA = 85°C ^{Note 4}	1,000			Times
Number of data flash rewrites ^{Note 1, 2, 3}		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C ^{Note 4}	100,000			
		Retained for 20 years TA = 85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. This temperature is the average value at which data are retained.

Remark When updating data multiple times, use the flash memory as one for updating data.

3.10 Dedicated Flash Memory Programmer Communication (UART)

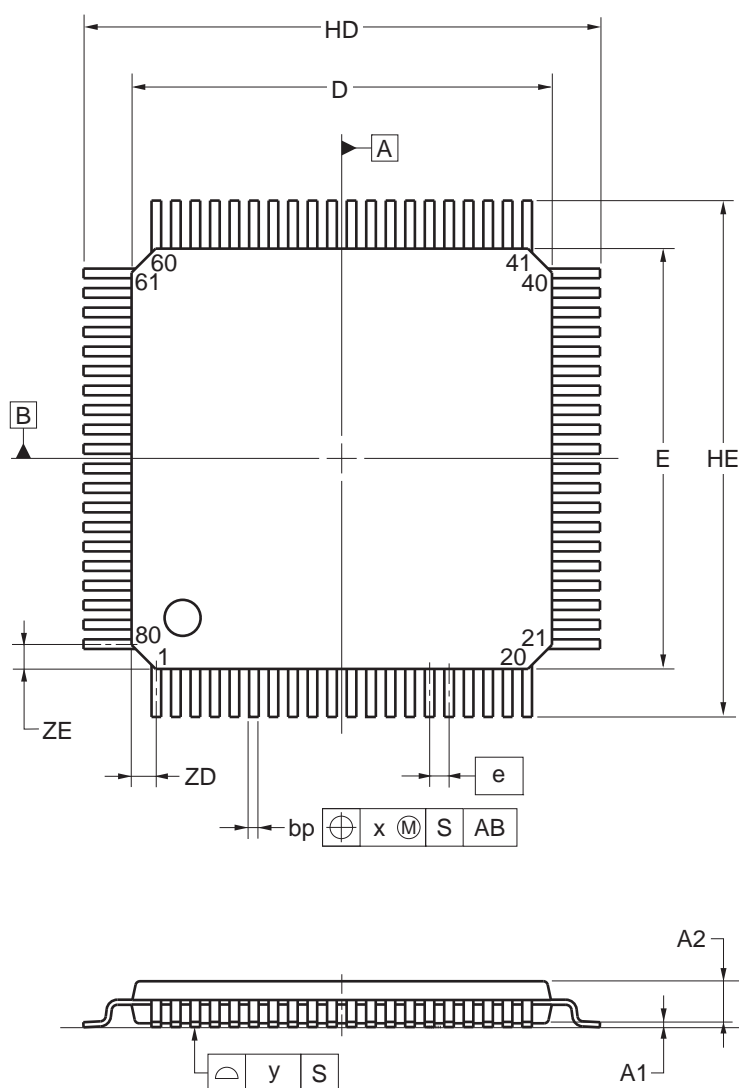
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.2 80-pin Products

R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA, R5F10WMEAFA, R5F10WMFAFA, R5F10WMGAFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—