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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmcafa-x0

○ ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/L13	
			64 pins	80 pins
128 KB	4 KB	8 KB[Note]	R5F10WLG	R5F10WMG
96 KB	4 KB	6 KB	R5F10WLF	R5F10WMF
64 KB	4 KB	4 KB	R5F10WLE	R5F10WME
48 KB	4 KB	2 KB	R5F10WLD	R5F10WMD
32 KB	4 KB	1.5 KB	R5F10WLC	R5F10WMC
16 KB	4 KB	1 KB	R5F10WLA	R5F10WMA

Note This is about 7 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3** in the RL78/L13 User's Manual.)

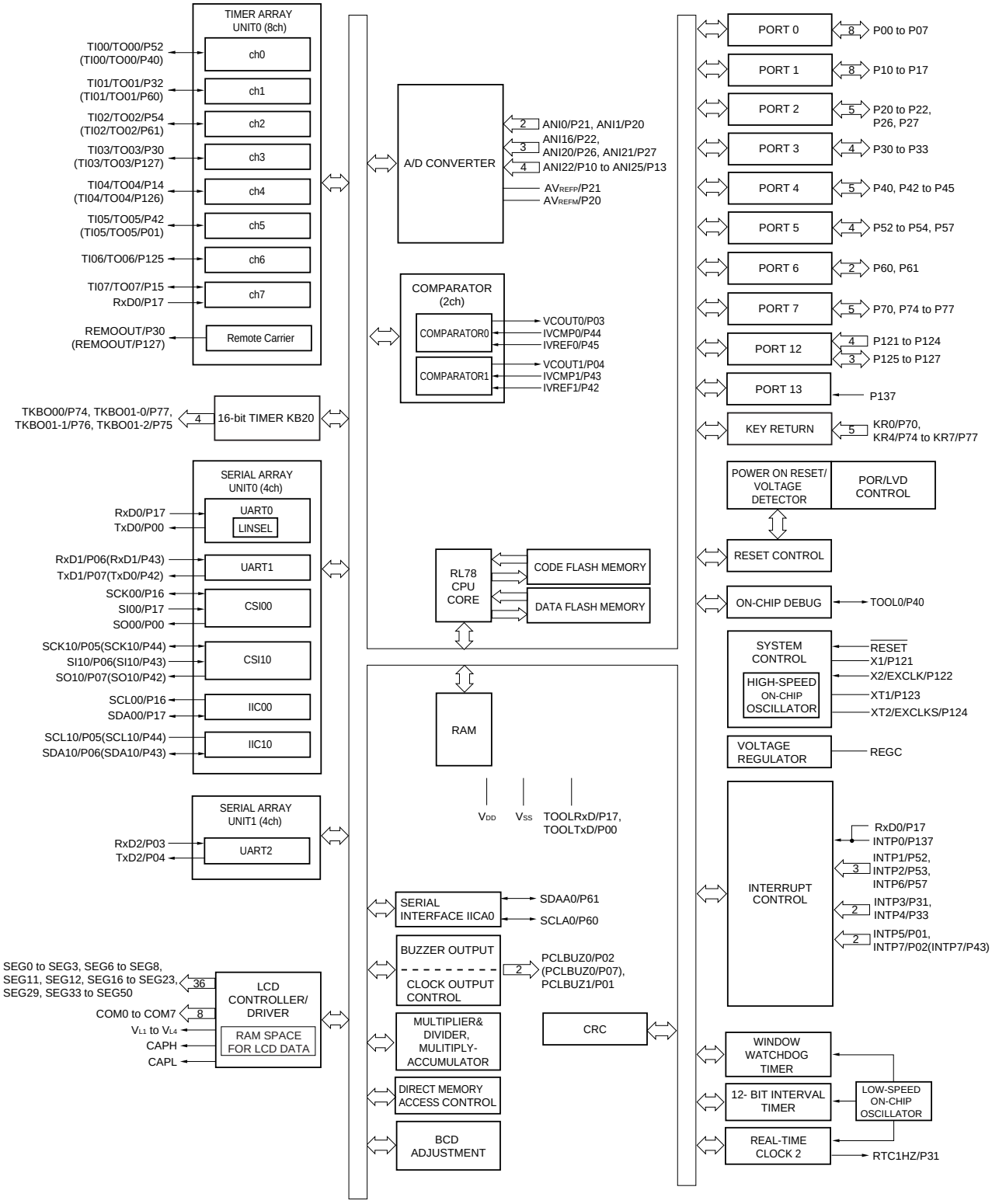
Pin Count	Package	Data Flash	Fields of Application[Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F10WLAAFA#30, R5F10WLAAFA#50, R5F10WLCAFA#30, R5F10WLCAFA#50, R5F10WLDAFA#30, R5F10WLDAFA#50, R5F10WLEAFA#30, R5F10WLEAFA#50, R5F10WLFAFA#30, R5F10WLFAFA#50, R5F10WLGAFA#30, R5F10WLGAFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A G	R5F10WLAAFB#30, R5F10WLAAFB#50, R5F10WLCAFB#30, R5F10WLCAFB#50, R5F10WLDAFB#30, R5F10WLDAFB#50, R5F10WLEAFB#30, R5F10WLEAFB#50, R5F10WLFAFB#30, R5F10WLFAFB#50, R5F10WLGAFB#30, R5F10WLGAFB#50, R5F10WLAGFB#30, R5F10WLAGFB#50, R5F10WLCGFB#30, R5F10WLCGFB#50, R5F10WLDGFB#30, R5F10WLDGFB#50, R5F10WLEGFB#30, R5F10WLEGFB#50, R5F10WLFGFB#30, R5F10WLFGFB#50, R5F10WLGGFB#30, R5F10WLGGFB#50
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F10WMAAFA#30, R5F10WMAAFA#50, R5F10WMCAFA#30, R5F10WMCAFA#50, R5F10WMDAFA#30, R5F10WMDAFA#50, R5F10WMEAFA#30, R5F10WMEAFA#50, R5F10WMFAFA#30, R5F10WMFAFA#50, R5F10WMGAFA#30, R5F10WMGAFA#50
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A G	R5F10WMAAFB#30, R5F10WMAAFB#50, R5F10WMCAFB#30, R5F10WMCAFB#50, R5F10WMDAFB#30, R5F10WMDAFB#50, R5F10WMEAFB#30, R5F10WMEAFB#50, R5F10WMFAFB#30, R5F10WMFAFB#50, R5F10WMGAFB#30, R5F10WMGAFB#50, R5F10WMAGFB#30, R5F10WMAGFB#50, R5F10WMCGFB#30, R5F10WMCGFB#50, R5F10WMDGFB#30, R5F10WMDGFB#50, R5F10WMEGFB#30, R5F10WMEGFB#50, R5F10WMFGFB#30, R5F10WMFGFB#50, R5F10WMGGFB#30, R5F10WMGGFB#50

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/L13.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.5 Block Diagram

1.5.1 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

(2/2)

Item		64-pin	80-pin
		R5F10WLx (x = A, C-G)	R5F10WMx (x = A, C-G)
Clock output/buzzer output controller		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/10-bit resolution A/D converter		9 channels	12 channels
Comparator		2 channels	
Serial interface		[64-pin] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART: 1 channel [80-pin] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART: 2 channels	
	I^2C bus	1 channel	
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output	36 (32)Note 1	51 (47)Note 1
	Common signal output	4 (8)Note 1	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)	
DMA controller		4 channels	
Vectored interrupt sources	Internal	32	35
	External	11	11
Key interrupt		5	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction executionNote 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)	
Voltage detector		• Rising edge: 1.67 V to 4.06 V (14 steps) • Falling edge: 1.63 V to 3.98 V (14 steps)	
On-chip debug function		Provided	
Power supply voltage		V_{DD} = 1.6 to 5.5 V (TA = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (TA = -40 to +105°C)	
Operating ambient temperature		Consumer applications: T_A = –40 to +85°C Industrial applications: T_A = –40 to +105°C	

Notes 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. This reset occurs when instruction code FFH is executed.
This reset does not occur during emulation using an in-circuit emulator or an on-chip debugging emulator.

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130				20.0[Note 2]	mA
		Per pin for P60 and P61				15.0[Note 2]	mA
		Total of P40 to P47, P130 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			9.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			4.5	mA
		Total of P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P70 to P77, P125 to P127 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			90.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			20.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70%[Note 3])				160.0	mA
	I_{OL2}	Per pin for P20 and P21				0.4[Note 2]	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ V_{DD} ≤ 5.5 V			0.8	mA

Notes 1. Value of the current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin

2. Do not exceed the total current value.

3. Output current value under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 70.0 mA

Total output current of pins = (70.0 × 0.7)/(80 × 0.01) ≅ 61.25 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer.

6. Not including the current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

3. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

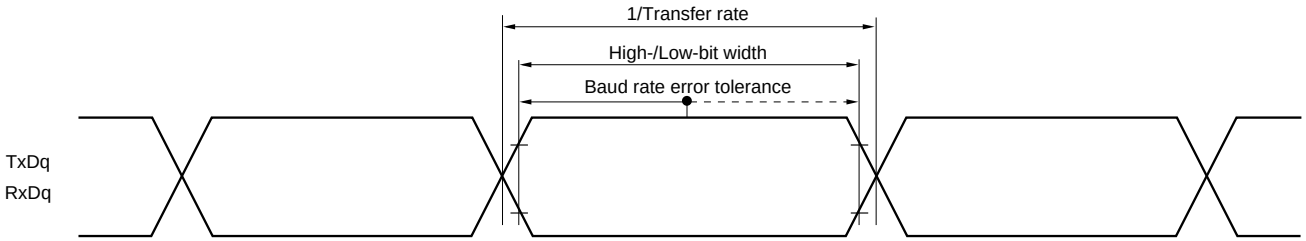
5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1						0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 2, 3	f_{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4						0.04		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz					0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V				1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1						75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1						75.0		μA
LVD operating current	I_{LVD} Notes 1, 7						0.08		μA
Comparator operating current	I_{CMP} Notes 1, 11	V_{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				6.5		μA
			Comparator low-speed mode				1.7		μA
		V_{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode				8.0		μA
			Comparator high-speed mode				4.0		μA
			Comparator low-speed mode				1.3		μA
Self-programming operating current	I_{FSP} Notes 1, 9						2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8						2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	While the mode is shifting Note 10				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV_{REFP} = V_{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation					0.70	0.84	mA
LCD operating current	I_{LCD1} Notes 1, 12, 13	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.20	μA
	I_{LCD2} Note 1, 12	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V (V_{LCD} = 04H)		0.85	2.20	μA
					V_{DD} = 5.0 V, V_{L4} = 5.1 V (V_{LCD} = 12H)		1.55	3.70	μA
	I_{LCD3} Note 1, 12	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20	0.50	μA

(**Notes** and **Remarks** are listed on the next page.)

UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Notes 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V (2.4 V[Note 8]) ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

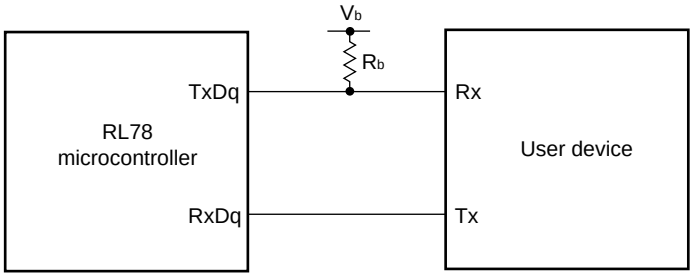
* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

8. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

4. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK}+ 135[Note 4]		1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK}+ 135[Note 4]		1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		ns
		1.8 V (2.4 V[Note 2]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 3], C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		1/f_{MCK}+ 190[Note 4]		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V (2.4 V[Note 2]) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 3], C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Condition in HS (high-speed main) mode

3. Use it with $V_{DD} \geq V_b$.

4. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(3) I^2C fast mode plus

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	–		–		kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		μs
Hold time when SCLA0 =“L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		–		–		μs
Hold time when SCLA0 =“H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		–		–		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	–		–		μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		–		–		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		–		–		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

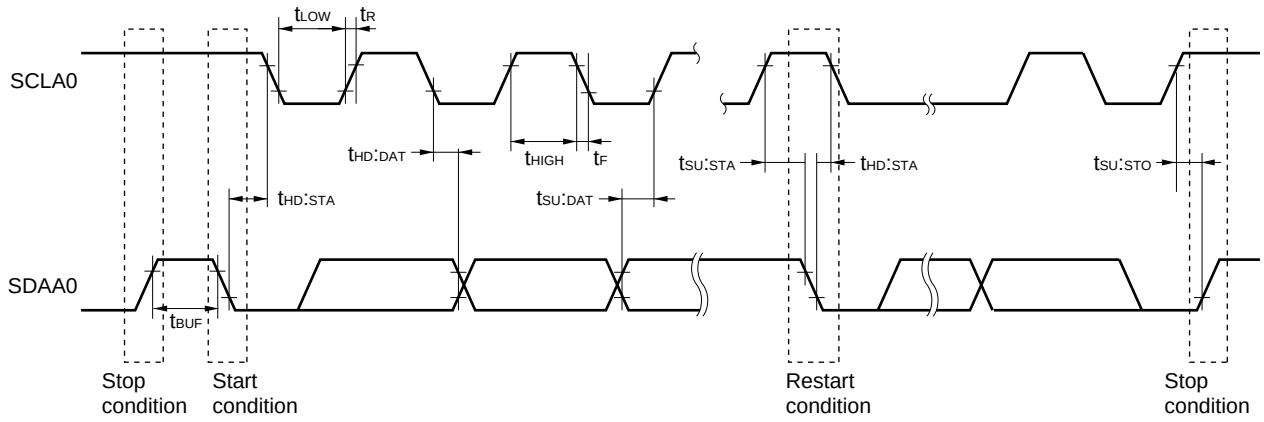
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4[Note 1] = 0.47 μF[Note 2]	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4[Note 1] = 0.47 μF		$2 V_{L1} – 0.10$	$2 V_{L1}$	$2 V_{L1}$	V
Tripler output voltage	V_{L4}	C1 to C4[Note 1] = 0.47 μF		$3 V_{L1} – 0.15$	$3 V_{L1}$	$3 V_{L1}$	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF ± 30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **5.4 System Clock Oscillator** in the RL78/L13 User's Manual.

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequencyNotes 1, 2	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy		+85 to +105°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–2		+2	%
		–20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1		+1	%
		–40 to –20°C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **AC Characteristics** for the instruction execution time.

3.3.2 Supply current characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	HS (high-speed main) mode Note 5	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.0		mA
						V_{DD} = 3.0 V		2.0		mA
					Normal operation	V_{DD} = 5.0 V		3.8	7.0	mA
						V_{DD} = 3.0 V		3.8	7.0	mA
				f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		mA
					Normal operation	V_{DD} = 5.0 V		3.6	6.5	mA
						V_{DD} = 3.0 V		3.6	6.5	mA
				f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.7	5.0	mA
						V_{DD} = 3.0 V		2.7	5.0	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	5.4	mA
						Resonator connection		3.2	5.6	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.9	5.4	mA
						Resonator connection		3.2	5.6	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4, T_A = –40°C	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +25°C	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +50°C	Normal operation	Square wave input		4.1	7.1	μA
						Resonator connection		4.4	7.1	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +70°C	Normal operation	Square wave input		4.3	8.7	μA
						Resonator connection		4.7	8.7	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +85°C	Normal operation	Square wave input		4.7	12.0	μA
						Resonator connection		5.2	12.0	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +105°C	Normal operation	Square wave input		6.4	35.0	μA
						Resonator connection		6.6	35.0	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation (AMPHS1 = 1). The current flowing into the LCD controller/driver, 16-bit timer KB20, real-time clock 2, 12-bit interval timer, and watchdog timer is not included.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

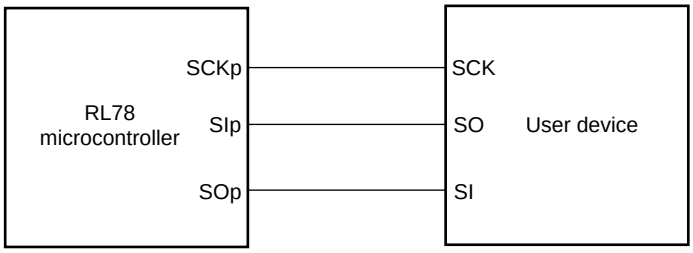
2. f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

3. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

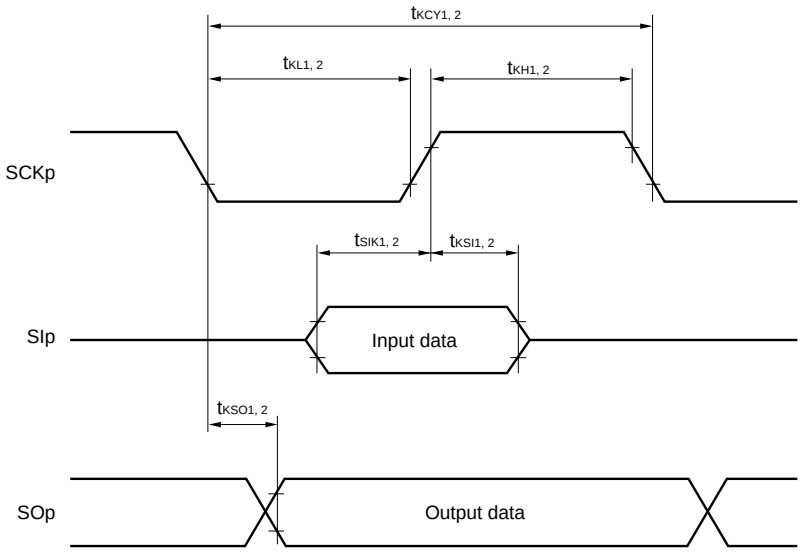
4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

5. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

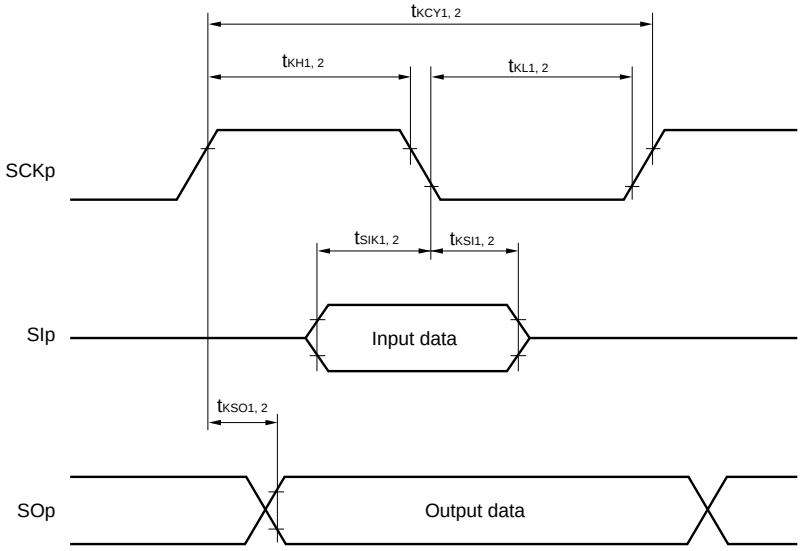
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 10)

2. m: Unit number, n: Channel number (mn = 00, 02)

(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 220 Note 2		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 580 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(**Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Reference Voltage / Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0, ANI1	–	See **3.6.1 (2)**.	See **3.6.1 (3)**.
ANI16 to ANI25	See **3.6.1 (1)**.		
Internal reference voltage Temperature sensor output voltage	See **3.6.1 (1)**.		–

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pins: ANI16 to ANI25, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

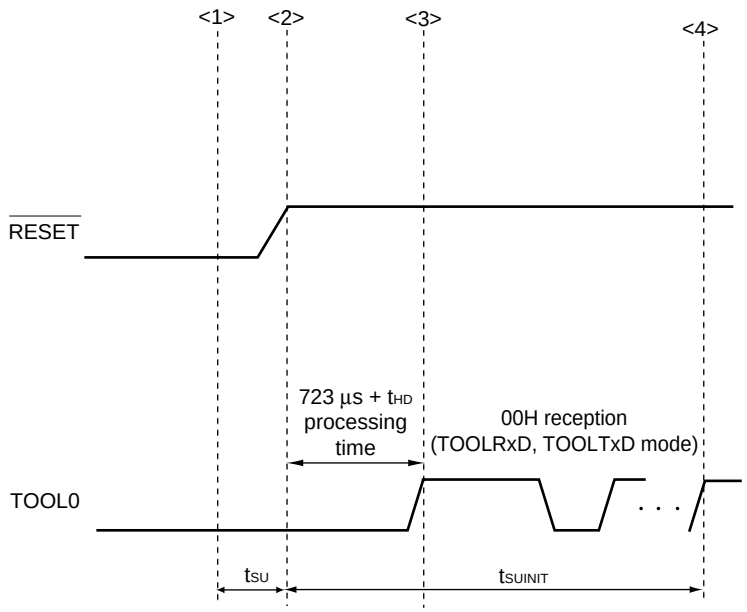
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}[Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI16 to ANI25	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD}[Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution AV_{REFP} = V_{DD}[Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}[Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI25		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))		V_{BGR}[Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode))		V_{TMPS25}[Note 4]			V

(**Notes** are listed on the next page.)

3.11 Timing Specifications for Switching Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and completion the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)