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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmdafa-30

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.5 Block Diagram

1.5.1 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.



2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to +85°C)

Target productsA: Consumer applications; TA = -40 to +85°CR5F10WLAAFA, R5F10WLCAFA, R5F10WLDAFA,R5F10WLEAFA, R5F10WLFAFA, R5F10WLGAFA,R5F10WLAAFB, R5F10WLCAFB, R5F10WLDAFB,R5F10WLEAFB, R5F10WLFAFB, R5F10WLGAFB,R5F10WMAAFA, R5F10WMCAFA, R5F10WMDAFA,R5F10WMEAFA, R5F10WMCAFA, R5F10WMGAFA,R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFA,R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFA,R5F10WMEAFA, R5F10WMCAFB, R5F10WMGAFA,R5F10WMAAFB, R5F10WMCAFB, R5F10WMDAFB,R5F10WMEAFB, R5F10WMCAFB, R5F10WMDAFB,

G: Industrial applications; when using T_A = -40 to +105°C specification products at T_A = -40 to +85°C R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB, R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB R5F10WMAGFB, R5F10WMCGFB, R5F10WMDGFB, R5F10WMEGFB, R5F10WEGFB, R5F10WEGFB,

- Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 - 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L13 User's Manual.



Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57,	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -10.0 \ \text{mA} \end{array}$	Vdd - 1.5			V
		P70 to P77, P125 to P127, P130	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OH1}} = -3.0 \ \text{mA} \end{array}$	Vdd - 0.7			V
			$\begin{array}{l} 2.7 \ \text{V} \leq \text{V}_{\text{DD}} \leq 5.5 \ \text{V}, \\ \text{I}_{\text{OH1}} = -2.0 \ \text{mA} \end{array}$	$V_{\text{DD}}-0.6$			V
			1.8 V \leq Vdd \leq 5.5 V, Іон1 = -1.5 mA	$V_{\text{DD}}-0.5$			V
			$\begin{array}{l} 1.6 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}, \\ \text{I}_{\text{OH1}} = -1.0 \text{ mA} \end{array}$	$V_{\text{DD}}-0.5$			V
	Vон2	P20 and P21	1.6 V \leq Vdd \leq 5.5 V, Ioh2 = -100 μ A	$V_{\text{DD}} - 0.5$			V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 20 \ \text{mA} \end{array} \end{array} \label{eq:eq:observed_eq}$			1.3	V
			$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 8.5 \ mA \end{array} \end{array} \label{eq:DD}$			0.7	V
			$\begin{array}{l} 2.7 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 3.0 \ mA \end{array} \end{array} \label{eq:DD}$			0.6	V
			$2.7 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V},$ lol1 = 1.5 mA			0.4	V
			$\begin{array}{l} 1.8 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL1}} = 0.6 \ mA \end{array} \end{array} \label{eq:DD}$			0.4	V
			$1.6 \text{ V} \le \text{V}_{\text{DD}} < 1.8 \text{ V},$ Iol1 = 0.3 mA			0.4	V
	V _{OL2}	P20 and P21	$1.6 V \le V_{DD} \le 5.5 V,$ Iol2 = 400 μA			0.4	V
	Vol3	P60 and P61	$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL3}} = 15.0 \ \text{mA} \end{array}$			2.0	V
			$\begin{array}{l} 4.0 \ V \leq V_{\text{DD}} \leq 5.5 \ V, \\ I_{\text{OL3}} = 5.0 \ mA \end{array}$			0.4	V
			$2.7 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V},$ $I_{\text{OL3}} = 3.0 \text{ mA}$			0.4	V
			$1.8 \text{ V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V},$ Iol3 = 2.0 mA			0.4	V
			$1.6 V \le V_{DD} < 1.8 V$, Iol3 = 1.0 mA			0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



(TA = -40 to +85°C, 1.6 V \leq VDD \leq 5.5 V, Vss = 0 V)

(2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	DD2Note 2	HALT	HS (high-speed	fHOCO = 48 MHz ^{Note 4} ,	V _{DD} = 5.0 V		0.71	1.95	mA
current ^{Note 1}		mode	main) mode ^{note} 7	fı⊢ = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.71	1.95	
				fносо = 24 MHz ^{Note 4} ,	V _{DD} = 5.0 V		0.49	1.64	mA
				fı⊢ = 24 MHz ^{Note 4}	V _{DD} = 3.0 V		0.49	1.64	
				fносо = 16 MHz ^{Note 4} ,	V _{DD} = 5.0 V		0.43	1.11	mA
			fı⊢ = 16 MHz ^{Note 4}	V _{DD} = 3.0 V		0.43	1.11		
			LS (low-speed	fносо = 8 MHz ^{Note 4} ,	V _{DD} = 3.0 V		280	770	μA
		main) mode 7	main) mode ^{note} 7	fiH = 8 MHz Note 4	V _{DD} = 2.0 V		280	770	
			LV (low-voltage	f _{HOCO} = 4 MHz ^{Note 4} ,	V _{DD} = 3.0 V		430	700	μA
			main) mode ^{Note 7}	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 2.0 V		430	700	
			HS (high-speed	f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.31	1.42	mA
			main) mode ^{Note} 7	V _{DD} = 5.0 V	Resonator connection		0.48	1.42	
				f _{MX} = 20 MHz ^{Note 3} ,	Square wave input		0.29	1.42	mA
				V _{DD} = 3.0 V	Resonator connection		0.48	1.42	
				f _{MX} = 16 MHz ^{Note 3} ,	Square wave input		0.26	0.86	mA
				V _{DD} = 5.0 V	Resonator connection		0.45	1.15	
				f _{MX} = 16 MHz ^{Note 3} ,	Square wave input		0.25	0.86	mA
			V _{DD} = 3.0 V	Resonator connection		0.44	1.15		
				f _{MX} = 10 MHz ^{Note 3} ,	Square wave input		0.20	0.63	mA
		V _{DD} = 5.0 V	Resonator connection		0.28	0.71			
					f _{MX} = 10 MHz ^{Note 3} ,	Square wave input		0.19	0.63
					V _{DD} = 3.0 V	Resonator connection		0.28	0.71
			LS (low-speed	f _{MX} = 8 MHz ^{Note 3} ,	Square wave input		100	560	μA
			main) mode ^{Note 7}	V _{DD} = 3.0 V	Resonator connection		160	560	
				f _{MX} = 8 MHz ^{Note 3} ,	Square wave input		100	560	μA
				V _{DD} = 2.0 V	Resonator connection		160	560	
			Subsystem	fsue = 32.768 kHz ^{Note 5} ,	Square wave input		0.34	0.62	μA
			clock operation	T _A = -40°C	Resonator connection		0.51	0.80	
				fsue = 32.768 kHz ^{Note 5} ,	Square wave input		0.38	0.62	μA
				T _A = +25°C	Resonator connection		0.57	0.80	
				fsuв = 32.768 kHz ^{Note 5} ,	Square wave input		0.46	2.30	μA
				T _A = +50°C	Resonator connection		0.67	2.49	
				fsue = 32.768 kHz ^{Note 5} ,	Square wave input		0.65	4.03	μA
				TA = +70°C	Resonator connection		0.91	4.22	
				fsub = 32.768 kHz ^{Note 5} ,	Square wave input		1.00	8.04	μA
				TA - +03 C	Resonator connection		1.31	8.23	
	DD3 ^{Note 6}	STOP	T _A = -40°C				0.18	0.52	μA
		mode	T _A = +25°C				0.24	0.52	
			$T_A = +50^{\circ}C$				0.33	2.21	
			$I_A = +70^{\circ}C$				0.53	3.94	
			I _A = +85°C				0.93	7.95	

(Notes and Remarks are listed on the next page.)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

2. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))





UART mode bit width (during communication at different potential) (reference)

- Remarks 1.
 R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
 - **2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 - fMCK: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))



- Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps
 - 2. Condition in HS (high-speed main) mode
 - 3. Use it with $V_{DD} \ge V_b$.
 - **4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - **6.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp[↑]" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)





3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to +105°C)

This chapter describes the following electrical specifications. Target products G: Industrial applications $T_A = -40$ to $+105^{\circ}C$

R5F10WLAGFB, R5F10WLCGFB, R5F10WLDGFB, R5F10WLEGFB, R5F10WLFGFB, R5F10WLGGFB R5F10WMAGFB, R5F10WMCGFB, R5F10WMDGFB, R5F10WMEGFB, R5F10WMFGFB, R5F10WMGGFB

- Cautions 1. The RL78/L13 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 - 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 With functions for each product in the RL78/L13 User's Manual.
 - Consult Renesas salesperson and distributor for derating when the product is used at T_A = +85°C to +105°C. Note that derating means "systematically lowering the load from the rated value to improve reliability".
- Remark When RL78/L13 is used in the range of $T_A = -40$ to +85°C, see CHAPTER 2 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to +85°C).



Parameter	Symbol		Conditions	Ratings	Unit
LCD voltage	V _{L1}	V∟1 voltage ^{Note 1}		–0.3 to +2.8 and –0.3 to V _{L4} +0.3	V
	VL2	VL2 voltage ^{Note 1}		–0.3 to VL4 +0.3Note 2	V
	VL3	VL3 voltage ^{Note 1}		–0.3 to VL4 +0.3 $^{\text{Note 2}}$	V
	VL4	VL4 voltage ^{Note 1}		–0.3 to +6.5	V
	VLCAP	CAPL, CAPH volt	age ^{Note 1}	–0.3 to VL4 +0.3Note 2	V
	Vout	COM0 to COM7	External resistance division method	–0.3 to V_{DD} +0.3 $^{\text{Note 2}}$	V
		SEG0 to SEG50	Capacitor split method	-0.3 to V_DD +0.3 $^{\rm Note\ 2}$	V
		output voltage	Internal voltage boosting method	–0.3 to VL4 +0.3 $^{\rm Note\ 2}$	V

Absolute Maximum Ratings (2/3)

- **Notes 1.** This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μ F ± 30%) and connect a capacitor (0.47 μ F ± 30%) between the CAPL and CAPH pins.
 - 2. Must be 6.5 V or lower.
- Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Vss: Reference voltage



Parameter	Symbol	Condition	ns		MIN.	TYP.	MAX.	Unit
Input leakage current, high	Ішні	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	$V_1 = V_{DD}$				1	μA
	Ілна	P20 and P21, RESET	VI = VDD				1	μA
	Ілнз	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	I21 to P124 Vi = V _{DD} 1, X2, XT1, XT2, EXCLK, (CLKS)				1	μA
				Resonator connected			10	μA
Input leakage current, low	Ilili	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	Vi = Vss				-1	μA
	ILIL2	P20 and P21, RESET	VI = VSS				-1	μA
	Ilili3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VSS	In input port mode and when external clock is input			-1	μA
				Resonator connected			-10	μA
On-chip pull-up resistance	Ruı	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	VI = VSS		10	20	100	kΩ
	Ru2	P40 to P44	VI = Vss		10	20	100	kΩ

(TA = -40 to +105°C, 2.4 V \leq VDD \leq 5.5 V, Vss = 0 V)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- **Remarks 1.** R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
 - **2.** r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)
- <R>
- 3. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)



Parameter	Symbol		Conditions	HS (high-spee	ed main) Mode	Unit
				MIN.	MAX.	
Transfer rate		Reception	$\begin{array}{l} 4.0 \ V \leq V_{DD} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V \end{array}$		fмск/12 ^{Note}	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps
			$\begin{array}{l} 2.7 \ V \leq V_{DD} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V \end{array}$		fмск/12 ^{Note}	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps
			$\begin{array}{l} 2.4 \ V \leq V_{DD} < 3.3 \ V, \\ 1.6 \ V \leq V_b \leq 2.0 \ V \end{array}$		fмск/12 ^{Note}	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2.0	Mbps

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) ($T_A = -40$ to +105°C, 2.4 V \leq V_{DD} \leq 5.5 V, V_{SS} = 0 V)

Note Transfer rate in SNOOZE mode is 4800 bps only.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (Vbb tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VH and VL, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

- **2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
- fMCK: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)



Notes 5. The smaller maximum transfer rate derived by using fMCK/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V \leq V_DD < 3.3 V and 1.6 V \leq V_b \leq 2.0 V

Maximum transfer rate = $\frac{1}{(0 \times 10 \times 10)}$ [bps]

$$\{-C_b \times R_b \times \ln (1 - \frac{10}{V_b})\} \times 3$$

Baud rate error (theoretical value) = $\frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 [\%]$

- * This value is the theoretical value of the relative difference between the transmission and reception sides.
- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.
- Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)







UART mode bit width (during communication at different potential) (reference)

- **Remarks 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
 - **2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)

3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))



Parameter	Symbol	Symbol Conditions		ed main) Mode	Unit
			MIN.	MAX.	
SIp setup time (to SCKp↓) ^{Note 2}	tsiĸ1	$\begin{array}{l} 4.0 \; V \leq V_{DD} \leq 5.5 \; V, \; 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 20 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$	88		ns
		$\begin{array}{l} 2.7 \; V \leq V_{DD} < 4.0 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 20 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	88		ns
		$\begin{array}{l} 2.4 \ V \leq V_{DD} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$	220		ns
SIp hold time (from SCKp↓) ^{Note 2}	tksii		38		ns
		$\label{eq:VD} \begin{array}{l} 2.7 \; V \leq V_{DD} < 4.0 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 20 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	38		ns
		$\begin{array}{l} 2.4 \ V \leq V_{DD} < 3.3 \ V, \ 1.6 \ V \leq V_b \leq 2.0 \ V, \\ C_b = 30 \ pF, \ R_b = 5.5 \ k\Omega \end{array}$	38		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	tkso1	$\begin{array}{l} 4.0 \; V \leq V_{DD} \leq 5.5 \; V, \; 2.7 \; V \leq V_b \leq 4.0 \; V, \\ C_b = 20 \; pF, \; R_b = 1.4 \; k\Omega \end{array}$		50	ns
		$\label{eq:VDD} \begin{array}{l} 2.7 \; V \leq V_{DD} < 4.0 \; V, \; 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 20 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$		50	ns
		$\label{eq:VDD} \hline $2.4~V \le V_{DD}$ < $3.3~V$, $1.6~V \le V_{b}$ \le $2.0~V$,} \\ C_{b}$ = $30~pF$, R_{b} = $5.5~k\Omega$ }$		50	ns

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2) $(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

CSI mode connection diagram (during communication at different potential)



- Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 - 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.
- **Remarks 1.** R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage
 - p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02),
 g: PIM and POM number (g = 0, 1)
 - **3.** fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00))





CSI mode serial transfer timing (master mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





Remark p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)



(7)	Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp external clock input)
	$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

Parameter	Symbol	C	Conditions	HS (high-spee	ed main) Mode	Unit
					MAX.	
SCKp cycle time Note 1	tkCY2	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	20 MHz < fмск	24/f мск		ns
		$2.7 V \le V_b \le 4.0 V$	8 MHz < fмск ≤ 20 MHz	20/f мск		ns
			$4 \text{ MHz} < f_{MCK} \le 8 \text{ MHz}$	16/fмск		ns
			fмск ≤ 4 MHz	12/fмск		ns
		$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 4.0 \text{ V},$	20 MHz < fмск	32/f мск		ns
		$2.3 V {\leq} V_b {\leq} 2.7 V$	16 MHz < fмск ≤ 20 MHz	28/fмск		ns
			8 MHz < f_MCK \leq 16 MHz	24/f мск		ns
			4 MHz < fмск ≤ 8 MHz	16/fмск		ns
			fмск ≤ 4 MHz	12/fмск		ns
		$2.4 \text{ V} \le \text{V}_{\text{DD}} < 3.3 \text{ V},$	20 MHz < fмск	72/fмск		ns
		$1.6 V \le V_b \le 2.0 V$	16 MHz < fмск ≤ 20 MHz	64/f мск		ns
			8 MHz < fмск ≤ 16 MHz	52/f мск		ns
			4 MHz < fмск ≤ 8 MHz	32/f мск		ns
			fмск ≤ 4 MHz	20/ f мск		ns
SCKp high-/low-level width	tkh2, tkl2	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	$2.7~V \leq V_b \leq 4.0~V$	tkcy2/2 - 24		ns
		$2.7 \text{ V} \le \text{V}_{\text{DD}} < 4.0 \text{ V}_{\text{PD}}$	$2.3~V \leq V_{b} \leq 2.7~V$	tkcy2/2 - 36		ns
		$2.4~V \leq V_{\text{DD}} < 3.3~V,$	$1.6~V \leq V_b \leq 2.0~V$	tkcy2/2 – 100		ns
SIp setup time	tsik2	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	$2.7~V \leq V_b \leq 4.0~V$	1/fмск + 40		ns
(to SCKp↑) ^{Note 2}		$2.7 \text{ V} \le \text{V}_{\text{DD}} < 4.0 \text{ V}_{\text{PD}}$	$2.3~V \leq V_{b} \leq 2.7~V$	1/fмск + 40		ns
		$2.4~V \leq V_{\text{DD}} < 3.3~V,$	$1.6~V \leq V_{b} \leq 2.0~V$	1/fмск + 60		ns
SIp hold time	tksi2	$4.0~V \leq V_{\text{DD}} \leq 5.5~V,$	$2.7~V \leq V_b \leq 4.0~V$	1/fмск + 62		ns
(from SCKp↑) ^{Note 3}		$2.7~V \leq V_{\text{DD}} \leq 4.0~V,$	$2.3~V \leq V_{b} \leq 2.7~V$	1/fмск + 62		ns
		$2.4~V \leq V_{\text{DD}} \leq 3.3~V,$	$1.6~V \leq V_b \leq 2.0~V$	1/fмск + 62		ns
Delay time from SCKp \downarrow to	tkso2	$4.0~V \le V_{\text{DD}} \le 5.5~V,$	$2.7~V \leq V_{b} \leq 4.0~V,$		2/fмск + 240	ns
SOp output ^{Note 4}		C _b = 30 pF, R _b = 1.4	ŧkΩ			
		$2.7 V \le V_{DD} < 4.0 V$, $C_b = 30 pF$, $R_b = 2.7$, 2.3 V \leq V _b \leq 2.7 V, 7 k Ω		2/fмск + 428	ns
		$2.4 \text{ V} \le \text{V}_{\text{DD}} < 3.3 \text{ V},$ $C_{\text{b}} = 30 \text{ pF}, \text{ R}_{\text{b}} = 5.5 \text{ s}$	$1.6 \text{ V} \leq \text{V}_{\text{b}} \leq 2.0 \text{ V},$ 5 kΩ		2/fмск + 1146	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)



3.5.2 Serial interface IICA

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}, \text{V}_{\text{SS}} = 0 \text{ V})$

Parameter	Symbol	Conditions	HS (high-speed main) Mode			Unit	
			Standar	d Mode	Fast	Mode	
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsc∟	Fast mode: fc⊥κ≥ 3.5 MHz	_	_	0	400	kHz
		Normal mode: fc⊥κ≥ 1 MHz	0	100	_	-	kHz
Setup time of restart condition	tsu:sta		4.7		0.6		μs
Hold time ^{Note 1}	thd:sta		4.0		0.6		μs
Hold time when SCLA0 = "L"	t LOW		4.7		1.3		μs
Hold time when SCLA0 = "H"	tніgн		4.0		0.6		μs
Data setup time (reception)	tsu:dat		250		100		ns
Data hold time (transmission)Note 2	thd:dat		0 ^{Note 3}	3.45	0 ^{Note 3}	0.9	μs
Setup time of stop condition	tsu:sto		4.0		0.6		μs
Bus-free time	t BUF		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of the:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

 $\begin{array}{ll} \mbox{Standard mode:} & C_b = 400 \mbox{ pF}, \mbox{ R}_b = 2.7 \mbox{ } k\Omega \\ \mbox{Fast mode:} & C_b = 320 \mbox{ pF}, \mbox{ R}_b = 1.1 \mbox{ } k\Omega \\ \end{array}$

IICA serial transfer timing





3.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection	Supply voltage level	VLVD0	When power supply rises	3.90	4.06	4.22	V
voltage			When power supply falls	3.83	3.98	4.13	V
		VLVD1	When power supply rises	3.60	3.75	3.90	V
			When power supply falls	3.53	3.67	3.81	V
		VLVD2	When power supply rises	3.01	3.13	3.25	V
			When power supply falls	2.94	3.06	3.18	V
		VLVD3	When power supply rises	2.90	3.02	3.14	V
			When power supply falls	2.85	2.96	3.07	V
		VLVD4	When power supply rises	2.81	2.92	3.03	V
			When power supply falls	2.75	2.86	2.97	V
		VLVD5	When power supply rises	2.71	2.81	2.92	V
			When power supply falls	2.64	2.75	2.86	V
		VLVD6	When power supply rises	2.61	2.71	2.81	V
			When power supply falls	2.55	2.65	2.75	V
		VLVD7	When power supply rises	2.51	2.61	2.71	V
			When power supply falls	2.45	2.55	2.65	V
Minimum puls	se width	t∟w		300			μs
Detection del	ay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(TA = -40 to +105°C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

Parameter	Symbol		Conc	MIN.	TYP.	MAX.	Unit	
Interrupt and reset	VLVD5	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
mode V	VLVD4		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V	
	Vlvd3	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V	
			Falling interrupt voltage	2.85	2.96	3.07	V	
	VLVD0	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V	
				Falling interrupt voltage	3.83	3.98	4.13	V

3.6.6 Supply voltage rise time

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, \text{ Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} rise slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.



(2) 1/4 bias method

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	VL1	C1 to C5 ^{Note 1}	VLCD = 04H	0.90	1.00	1.08	V
		= 0.47 μ F ^{Note 2}	VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	VL2	C1 to C5 ^{Note 1} = 0.47 μ F		2 VL1-0.08	2 VL1	2 VL1	V
Tripler output voltage	VL3	C1 to C5 ^{Note 1} = 0.47 μ F		3 VL1-0.12	3 VL1	3 VL1	V
Quadruply output voltage	VL4	C1 to C5 ^{Note 1} = 0.47 μ F		4 VL1-0.16	4 VL1	4 VL1	V
Reference voltage setup time ^{Note 2}	tvwait1			5			ms
Voltage boost wait time ^{Note 3}	tvwait2	C1 to C5 ^{Note 1} = 0.47 μ F		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

- C1: A capacitor connected between CAPH and CAPL
- C2: A capacitor connected between V_{L1} and GND
- C3: A capacitor connected between V_{L2} and GND
- C4: A capacitor connected between $V_{\mbox{\tiny L3}}$ and GND
- C5: A capacitor connected between $V_{{\scriptscriptstyle L4}}$ and GND
- C1 = C2 = C3 = C4 = C5 = 0.47 μ F ± 30%
- 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.7.3 Capacitor split method

(1) 1/3 bias method

$(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{V}_D \le 5.5 \text{ V}, \text{V}_{SS} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VL4 voltage	VL4	C1 to C4 = 0.47 μ F ^{Note 2}		VDD		V
VL2 voltage	VL2	C1 to C4 = 0.47 μ F ^{Note 2}	2/3 VL4 -	2/3 VL4	2/3 VL4 +	V
			0.1		0.1	
VL1 voltage	VL1	C1 to C4 = 0.47 μ F ^{Note 2}	1/3 VL4 -	1/3 VL4	1/3 VL4 +	V
			0.1		0.1	
Capacitor split wait time ^{Note 1}	tvwait		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

- C2: A capacitor connected between $V_{\mbox{\tiny L1}}$ and GND
- C3: A capacitor connected between $V_{\mbox{\tiny L2}}$ and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 pF±30 %

