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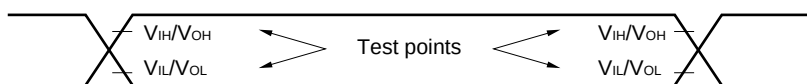
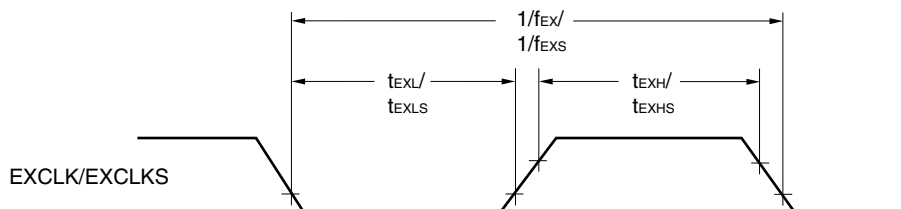
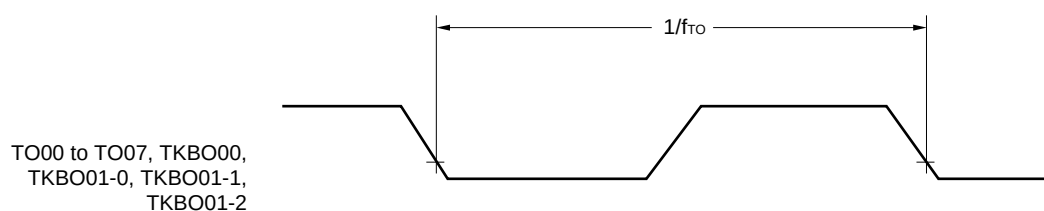
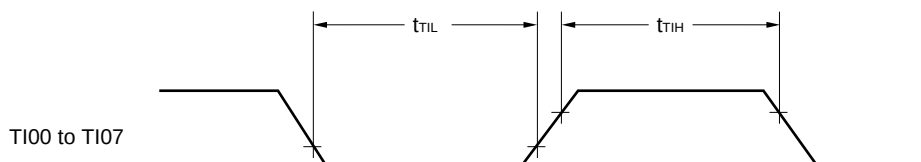
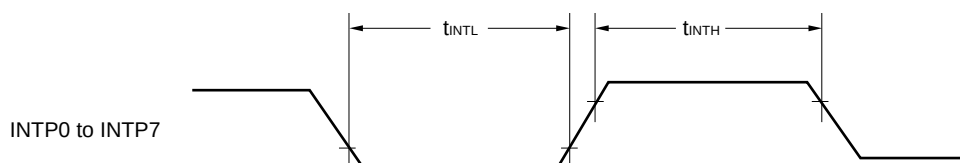
Details

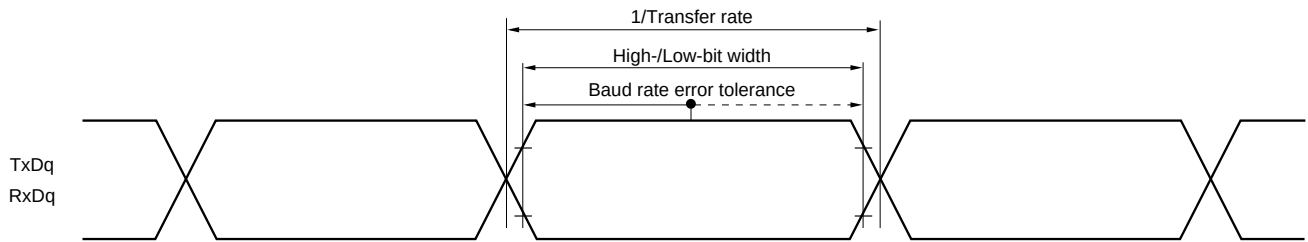
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmdafb-30

○ ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/L13	
			64 pins	80 pins
128 KB	4 KB	8 KB ^{Note}	R5F10WLG	R5F10WMG
96 KB	4 KB	6 KB	R5F10WLF	R5F10WMF
64 KB	4 KB	4 KB	R5F10WLE	R5F10WME
48 KB	4 KB	2 KB	R5F10WLD	R5F10WMD
32 KB	4 KB	1.5 KB	R5F10WLC	R5F10WMC
16 KB	4 KB	1 KB	R5F10WLA	R5F10WMA

Note This is about 7 KB when the self-programming function and data flash function are used. (For details, see **CHAPTER 3** in the RL78/L13 User's Manual.)

AC Timing Test Points**External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing**

UART mode bit width (during communication at same potential) (reference)

- Remarks**
1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 2. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Trans mission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V)			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V)			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			1.8 V (2.4 V ^{Note 8}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V)			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Use it with V_{DD} ≥ V_b.

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ($2.4\text{ V}^{\text{Note 8}}$) $\leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

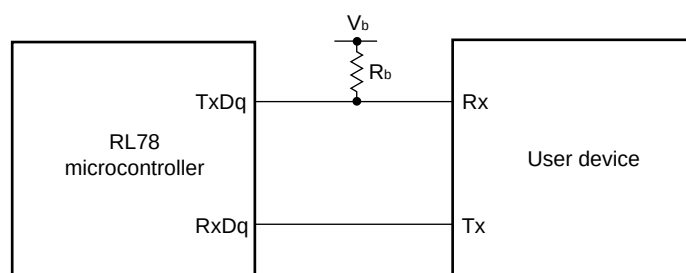
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.
8. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

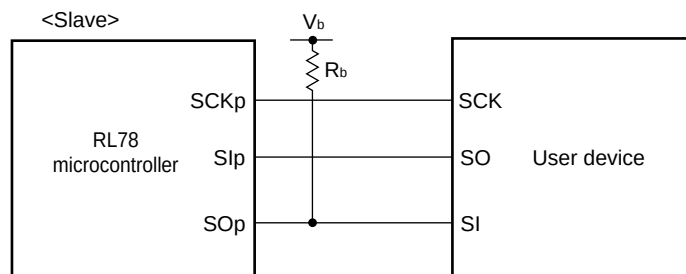
Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number ($m = 0$), n: Channel number ($n = 0$),
g: PIM and POM number ($g = 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number ($mn = 00$))
 4. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

- Notes**
1. Transfer rate in SNOOZE mode: MAX. 1 Mbps
 2. Condition in HS (high-speed main) mode
 3. Use it with $V_{DD} \geq V_b$.
 4. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Sip setup time becomes “to $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 5. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Sip hold time becomes “from $SCKp\downarrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
 6. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from $SCKp\uparrow$ ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

Caution Select the TTL input buffer for the Sip pin and $SCKp$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 135^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 135^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		$1/f_{MCK} + 190^{\text{Note 4}}$		ns
Data hold time (transmission)	$t_{HD:DAT}$	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	0	355	0	355	0	355	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	355	0	355	0	355	ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.**2.** Condition in HS (high-speed main) mode**3.** Use it with $V_{DD} \geq V_b$.**4.** Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(2) I²C fast mode(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		100		100		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V (2.4 V ^{Note 3}) ≤ V _{DD} ≤ 5.5 V		1.3		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

3. Condition in HS (high-speed main) mode

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), target pins: ANI0, ANI16 to ANI25

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3},
Reference voltage (–) = AVREFM^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. See 2.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the AVREFM MAX. value.

Integral linearity error: Add ±0.5 LSB to the AVREFM MAX. value.

Differential linearity error: Add ±0.2 LSB to the AVREFM MAX. value.

2.6.2 Temperature sensor /internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMPS25}	ADS register = 80H, T _A = +25°C		1.05		V
Internal reference output voltage	V _{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t _{AMP}				5	μs

2.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	When power supply rises	3.98	4.06	4.14	V
			When power supply falls	3.90	3.98	4.06	V
		V _{LVD1}	When power supply rises	3.68	3.75	3.82	V
			When power supply falls	3.60	3.67	3.74	V
		V _{LVD2}	When power supply rises	3.07	3.13	3.19	V
			When power supply falls	3.00	3.06	3.12	V
		V _{LVD3}	When power supply rises	2.96	3.02	3.08	V
			When power supply falls	2.90	2.96	3.02	V
		V _{LVD4}	When power supply rises	2.86	2.92	2.97	V
			When power supply falls	2.80	2.86	2.91	V
		V _{LVD5}	When power supply rises	2.76	2.81	2.87	V
			When power supply falls	2.70	2.75	2.81	V
		V _{LVD6}	When power supply rises	2.66	2.71	2.76	V
			When power supply falls	2.60	2.65	2.70	V
		V _{LVD7}	When power supply rises	2.56	2.61	2.66	V
			When power supply falls	2.50	2.55	2.60	V
		V _{LVD8}	When power supply rises	2.45	2.50	2.55	V
			When power supply falls	2.40	2.45	2.50	V
		V _{LVD9}	When power supply rises	2.05	2.09	2.13	V
			When power supply falls	2.00	2.04	2.08	V
		V _{LVD10}	When power supply rises	1.94	1.98	2.02	V
			When power supply falls	1.90	1.94	1.98	V
		V _{LVD11}	When power supply rises	1.84	1.88	1.91	V
			When power supply falls	1.80	1.84	1.87	V
		V _{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
		V _{LVD13}	When power supply rises	1.64	1.67	1.70	V
			When power supply falls	1.60	1.63	1.66	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

2.7 LCD Characteristics

2.7.1 External resistance division method

(1) Static display mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

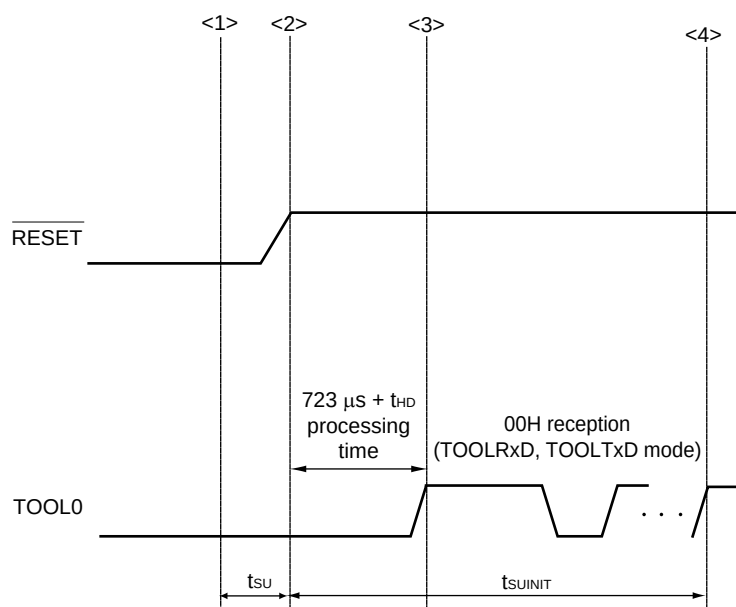
($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.11 Timing Specifications for Switching Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and completion the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (3/3)

Absolute Maximum Ratings (TA = 25 °C) (1/3)						
	Parameter	Symbol	Conditions		Ratings	Unit
<R>	Output current, high	IOH1	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−40	mA
<R>			Total of all pins −170 mA	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	−170	mA
<R>		IOH2	Per pin	P20, P21	−0.5	mA
<R>			Total of all pins		−1	mA
<R>	Output current, low	IOL1	Per pin	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P125 to P127, P130	40	mA
<R>			Total of all pins 170 mA	P40 to P47, P130	70	mA
				P00 to P07, P10 to P17, P22 to P27, P30 to P35, P50 to P57, P60, P61, P70 to P77, P125 to P127	100	mA
<R>		IOL2	Per pin	P20, P21	1	mA
<R>			Total of all pins		2	mA
		Operating ambient temperature	TA	In normal operation mode		−40 to +105
	In flash memory programming mode			°C		
	Storage temperature	Tstg			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{HOCO} = 48\text{ MHz}$ ^{Note 3} , $f_{IH} = 24\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0\text{ V}$		2.0		mA
						$V_{DD} = 3.0\text{ V}$		2.0		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.8	7.0	mA
						$V_{DD} = 3.0\text{ V}$		3.8	7.0	mA
				$f_{HOCO} = 24\text{ MHz}$ ^{Note 3} , $f_{IH} = 24\text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0\text{ V}$		1.7		mA
						$V_{DD} = 3.0\text{ V}$		1.7		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.6	6.5	mA
						$V_{DD} = 3.0\text{ V}$		3.6	6.5	mA
				$f_{HOCO} = 16\text{ MHz}$ ^{Note 3} , $f_{IH} = 16\text{ MHz}$ ^{Note 3}	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	5.0	mA
						$V_{DD} = 3.0\text{ V}$		2.7	5.0	mA
			HS (high-speed main) mode ^{Note 5}	$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	5.4	mA
						Resonator connection		3.2	5.6	mA
				$f_{MX} = 20\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		2.9	5.4	mA
						Resonator connection		3.2	5.6	mA
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
				$f_{MX} = 10\text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	3.2	mA
						Resonator connection		1.9	3.2	mA
			Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.0	5.4	μA
						Resonator connection		4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.1	7.1	μA
						Resonator connection		4.4	7.1	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	8.7	μA
						Resonator connection		4.7	8.7	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.7	12.0	μA
						Resonator connection		5.2	12.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ ^{Note 4} , $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.4	35.0	μA
						Resonator connection		6.6	35.0	μA

(Notes and Remarks are listed on the next page.)

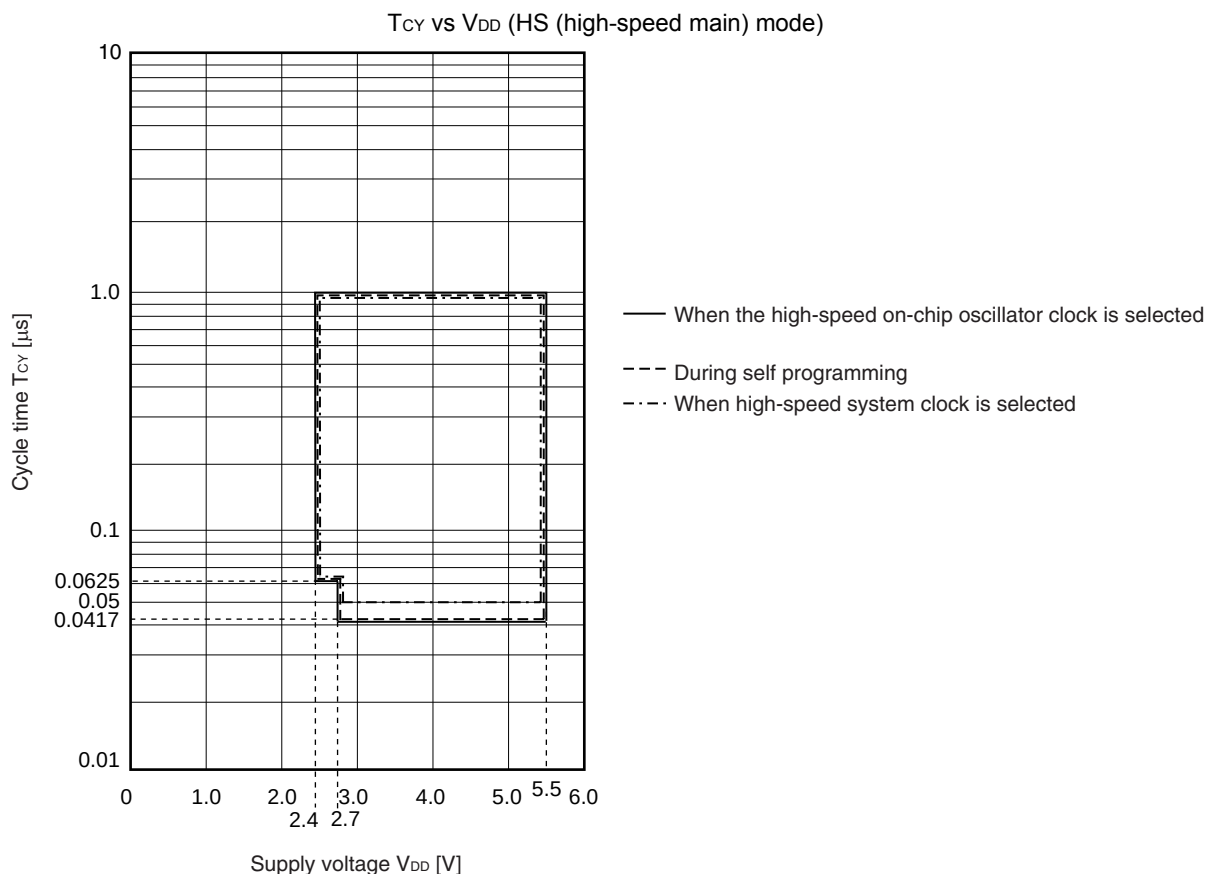
Note Specification under conditions where the duty factor is 50%.

Remark f_{MCK} : Timer array unit operation clock frequency

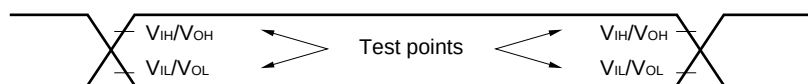
(Operation clock to be set by the CKS_{mn0}, CKS_{mn1} bits of timer mode register mn (TMR_{mn})

m: Unit number (m = 0), n: Channel number (n = 0 to 7))

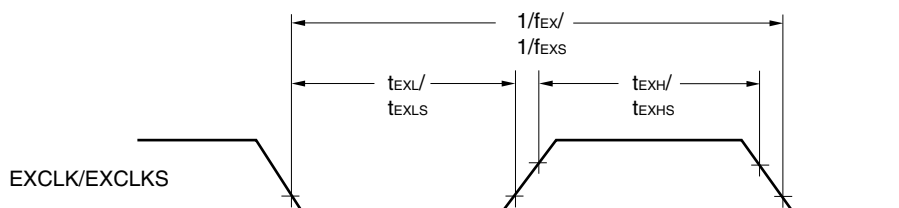
Minimum Instruction Execution Time during Main System Clock Operation

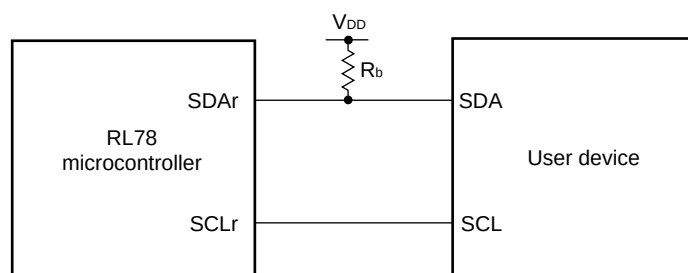
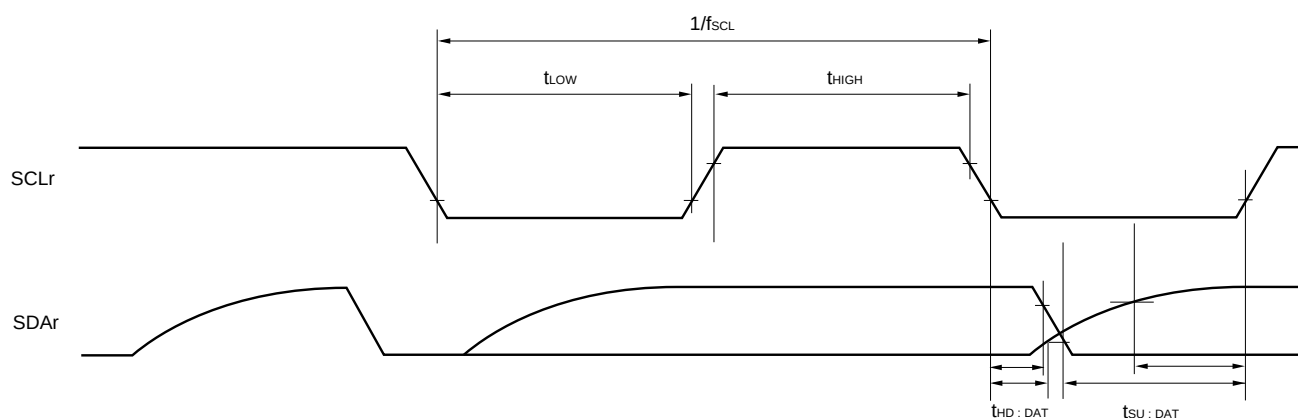


AC Timing Test Points



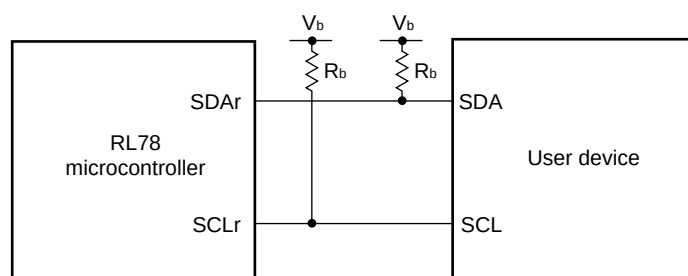
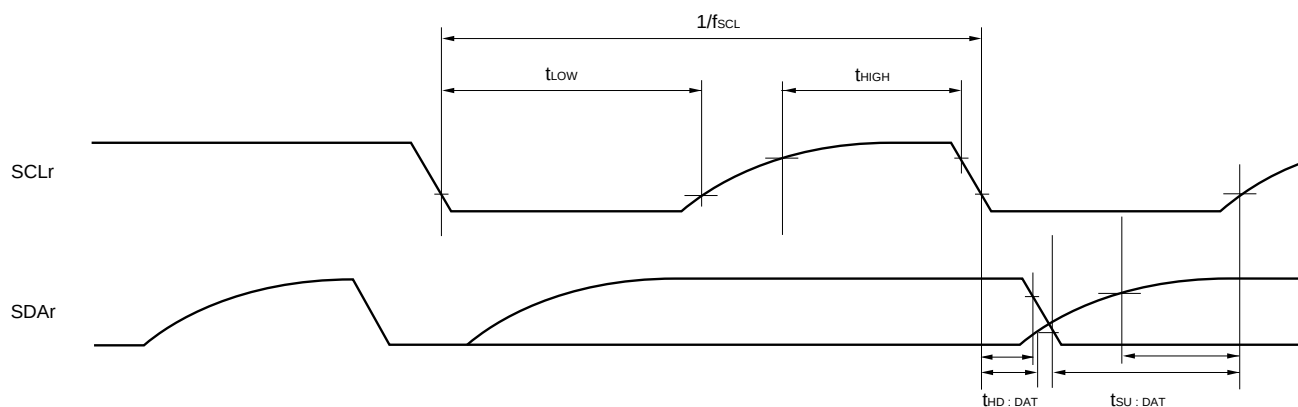
External System Clock Timing



Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 10), g: PIM and POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0-3), mn = 00-03, 10-13)

<R>

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 0, 1)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))

3.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μF	2 VL1 – 0.10	2 VL1	2 VL1	V	
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 μF	3 VL1 – 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GNDC1 = C2 = C3 = C4 = $0.47\ \mu\text{F} \pm 30\%$

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Revision History	RL78/L13 Data Sheet
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Rev.	Date	Description	
		Page	Summary
0.01	Apr 13, 2012	-	First Edition issued
0.02	Oct 31, 2012	-	Change of the number of segment pins • 64-pin products: 36 pins • 80-pin products: 51 pins
2.10	Aug 12, 2016	1	Modification of features of 16-bit timer and 16-bit timer KB20 (IH) in 1.1 Features
		5	Addition of product name (RL78/L13) and description (Top View) in 1.3.1 64-pin products
		6	Addition of product name (RL78/L13) and description (Top View) in 1.3.2 80-pin products
		10	Modification of functional overview of main system clock in 1.6 Outline of Functions
		15	Modification of description in Absolute Maximum Ratings (3/3)
		17, 18	Modification of description in 2.3.1 Pin characteristics
		38	Modification of remark 3 in 2.5.1 (4) During communication at same potential (simplified I ² C mode)
		68	Modification of the title and note, and addition of caution in 2.8 RAM Data Retention Characteristics
		70	Addition of Remark
		74	Modification of description in Absolute Maximum Ratings (T _A = 25 °C) (3/3)
		76	Modification of description in 3.3.1 Pin characteristics
		95	Modification of remark 3 in 3.5.1 (4) During communication at same potential (simplified I ² C mode)
		118	Modification of the title and note, and addition of caution in 3.8 RAM Data Retention Characteristics

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