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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

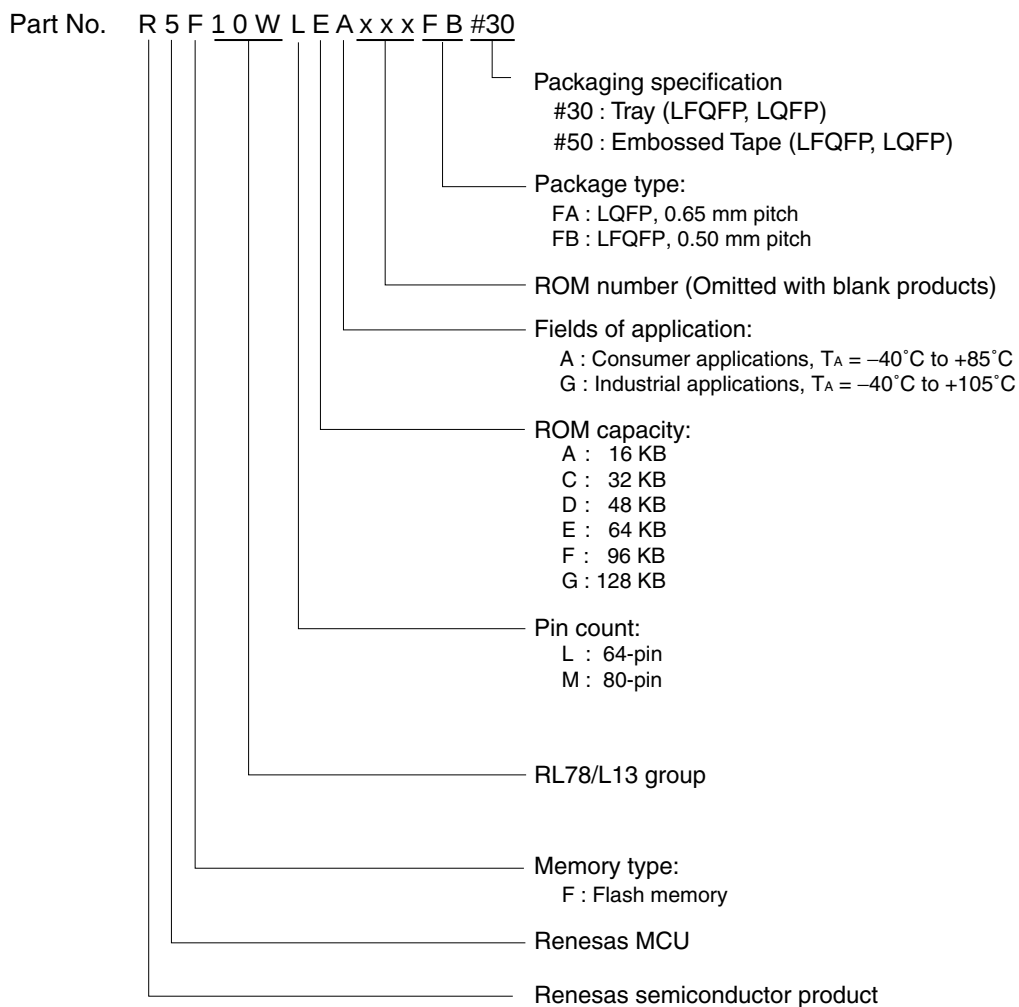
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmgafa-30

1.2 List of Part Numbers

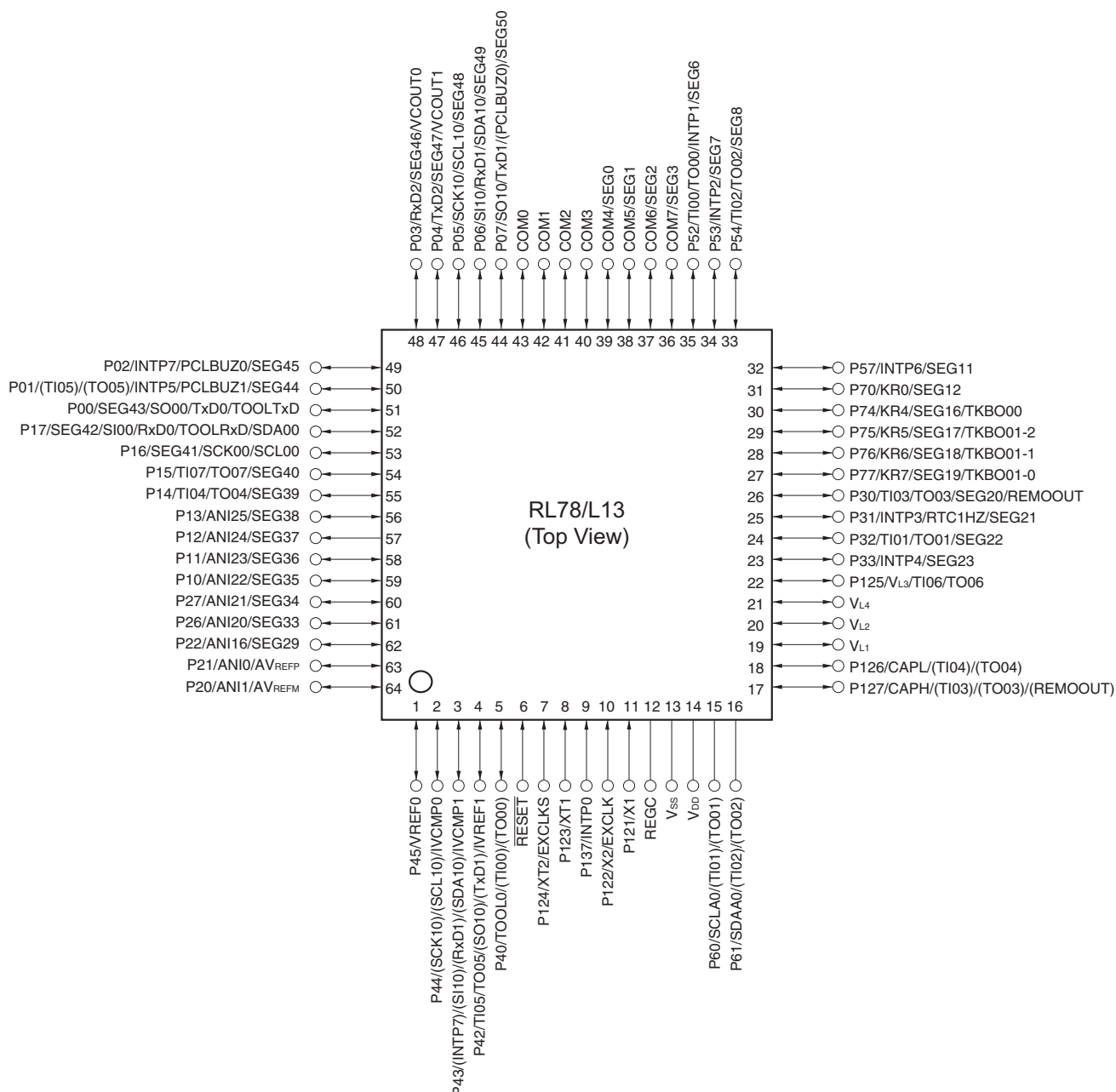
Figure 1-1. Part Number, Memory Size, and Package of RL78/L13



1.3 Pin Configuration (Top View)

<R> 1.3.1 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

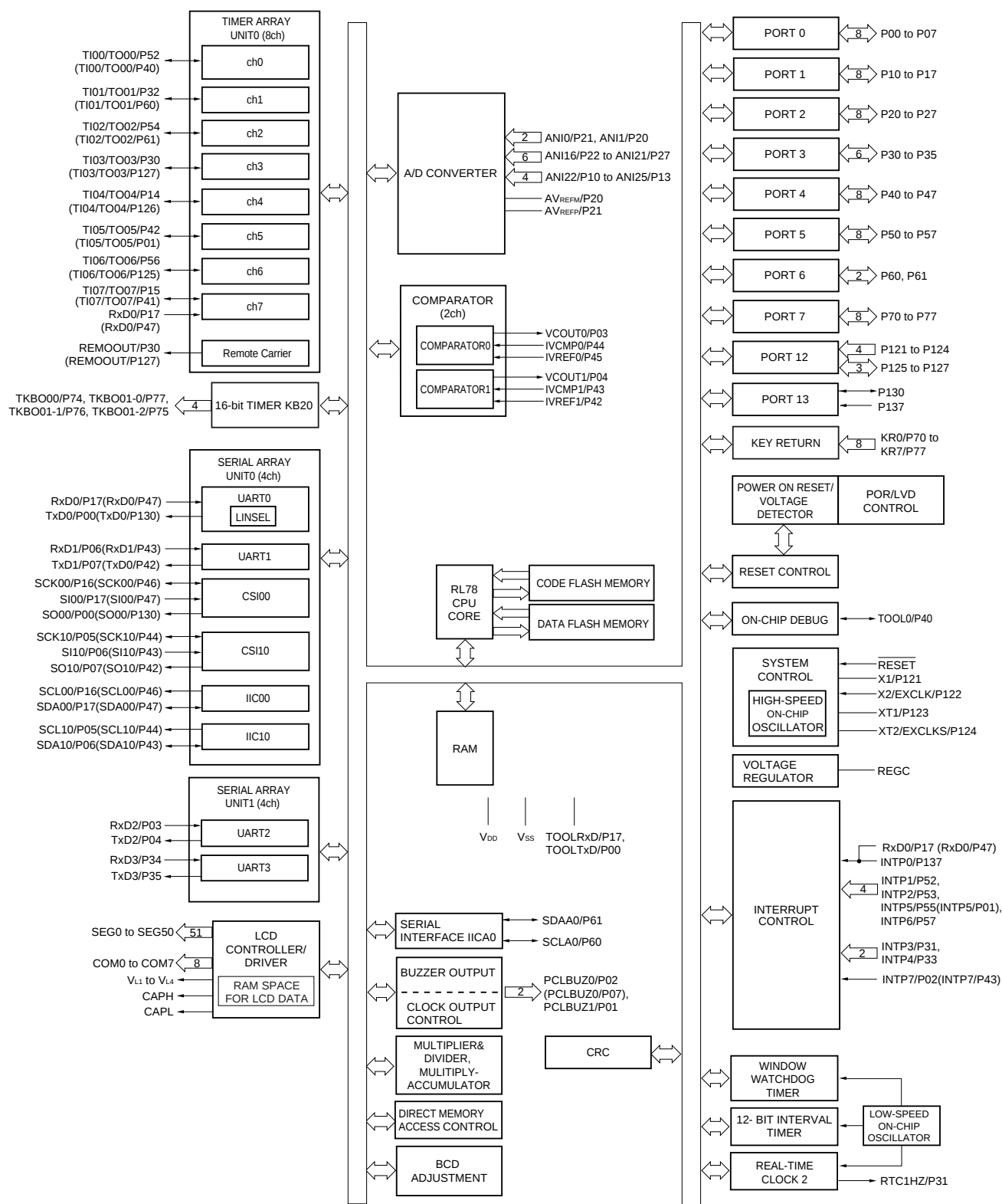


Caution Connect the REGC pin to VSS via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

1.5.2 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/L13 User's Manual.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{DD}				1	μA
	I _{LH2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{DD}				1	μA
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port mode and when external clock is input			1	μA
				Resonator connected			10	μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{SS}				−1	μA
	I _{LIL2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{SS}				−1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port mode and when external clock is input			−1	μA
				Resonator connected			−10	μA
On-chip pull-up resistance	R _{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	V _I = V _{SS}	2.4 V ≤ V _{DD} < 5.5 V	10	20	100	kΩ
				1.6 V ≤ V _{DD} < 2.4 V	10	30	100	kΩ
	R _{U2}	P40 to P44	V _I = V _{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

 $(T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ¹	I_{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	$f_{HOCO} = 48\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 24\text{ MHz}^{\text{Note 3}}$	Basic operation	$V_{DD} = 5.0\text{ V}$	2.0		mA
						$V_{DD} = 3.0\text{ V}$	2.0		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$	3.8	6.5	mA
						$V_{DD} = 3.0\text{ V}$	3.8	6.5	mA
				$f_{HOCO} = 24\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 24\text{ MHz}^{\text{Note 3}}$	Basic operation	$V_{DD} = 5.0\text{ V}$	1.7		mA
						$V_{DD} = 3.0\text{ V}$	1.7		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$	3.6	6.1	mA
						$V_{DD} = 3.0\text{ V}$	3.6	6.1	mA
				$f_{HOCO} = 16\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 16\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 5.0\text{ V}$	2.7	4.7	mA
						$V_{DD} = 3.0\text{ V}$	2.7	4.7	mA
			LS (low-speed main) mode ^{Note 5}	$f_{HOCO} = 8\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 8\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 3.0\text{ V}$	1.2	2.1	mA
						$V_{DD} = 2.0\text{ V}$	1.2	2.1	mA
			LV (low-voltage main) mode ^{Note 5}	$f_{HOCO} = 4\text{ MHz}^{\text{Note 3}}$, $f_{IH} = 4\text{ MHz}^{\text{Note 3}}$	Normal operation	$V_{DD} = 3.0\text{ V}$	1.2	1.8	mA
						$V_{DD} = 2.0\text{ V}$	1.2	1.8	mA
			HS (high-speed main) mode ^{Note 5}	$f_{MX} = 20\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	3.0	5.1	mA
						Resonator connection	3.2	5.2	mA
				$f_{MX} = 20\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	2.9	5.1	mA
						Resonator connection	3.2	5.2	mA
				$f_{MX} = 16\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				$f_{MX} = 16\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	2.5	4.4	mA
						Resonator connection	2.7	4.5	mA
				$f_{MX} = 10\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
				$f_{MX} = 10\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	1.9	3.0	mA
						Resonator connection	1.9	3.0	mA
			LS (low-speed main) mode ^{Note 5}	$f_{MX} = 8\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
				$f_{MX} = 8\text{ MHz}^{\text{Note 2}}$, $V_{DD} = 2.0\text{ V}$	Normal operation	Square wave input	1.1	2.0	mA
						Resonator connection	1.1	2.0	mA
			Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = -40^\circ\text{C}$	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +25^\circ\text{C}$	Normal operation	Square wave input	4.0	5.4	μA
						Resonator connection	4.3	5.4	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +50^\circ\text{C}$	Normal operation	Square wave input	4.1	7.1	μA
						Resonator connection	4.4	7.1	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +70^\circ\text{C}$	Normal operation	Square wave input	4.3	8.7	μA
						Resonator connection	4.7	8.7	μA
				$f_{SUB} = 32.768\text{ kHz}^{\text{Note 4}}$, $T_A = +85^\circ\text{C}$	Normal operation	Square wave input	4.7	12.0	μA
						Resonator connection	5.2	12.0	μA

(Notes and Remarks are listed on the next page.)

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	HS (high-speed main) mode ^{Note 7}	f _{HOCO} = 48 MHz ^{Note 4} , f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.71	1.95	mA	
					V _{DD} = 3.0 V		0.71	1.95		
				f _{HOCO} = 24 MHz ^{Note 4} , f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.49	1.64	mA	
					V _{DD} = 3.0 V		0.49	1.64		
				f _{HOCO} = 16 MHz ^{Note 4} , f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.43	1.11	mA	
					V _{DD} = 3.0 V		0.43	1.11		
			LS (low-speed main) mode ^{Note 7}	f _{HOCO} = 8 MHz ^{Note 4} , f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		280	770	μA	
					V _{DD} = 2.0 V		280	770		
			LV (low-voltage main) mode ^{Note 7}	f _{HOCO} = 4 MHz ^{Note 4} , f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		430	700	μA	
					V _{DD} = 2.0 V		430	700		
			HS (high-speed main) mode ^{Note 7}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	1.42	mA	
					Resonator connection		0.48	1.42		
					f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.29	1.42	mA
						Resonator connection		0.48	1.42	
					f _{MX} = 16 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.26	0.86	mA
						Resonator connection		0.45	1.15	
				f _{MX} = 16 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.25	0.86	mA	
					Resonator connection		0.44	1.15		
		f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V		Square wave input		0.20	0.63	mA		
				Resonator connection		0.28	0.71			
		f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V		Square wave input		0.19	0.63	mA		
				Resonator connection		0.28	0.71			
		LS (low-speed main) mode ^{Note 7}	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		100	560	μA		
				Resonator connection		160	560			
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		100	560	μA		
				Resonator connection		160	560			
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} , T _A = −40°C	Square wave input		0.34	0.62	μA		
				Resonator connection		0.51	0.80			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +25°C	Square wave input		0.38	0.62	μA		
				Resonator connection		0.57	0.80			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +50°C	Square wave input		0.46	2.30	μA		
				Resonator connection		0.67	2.49			
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +70°C	Square wave input		0.65	4.03	μA		
				Resonator connection		0.91	4.22			
		f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +85°C	Square wave input		1.00	8.04	μA			
			Resonator connection		1.31	8.23				
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.18	0.52	μA
			T _A = +25°C					0.24	0.52	
			T _A = +50°C					0.33	2.21	
			T _A = +70°C					0.53	3.94	
			T _A = +85°C					0.93	7.95	

(Notes and Remarks are listed on the next page.)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps
			1.8 V (2.4 V ^{Note 4}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		f _{MCK} /6 ^{Note s1, 2}		f _{MCK} /6 ^{Notes 1, 2}		f _{MCK} /6 ^{Notes 1, 2}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		4.0		1.3		0.6	Mbps

Notes 1. Transfer rate in SNOOZE mode is 4800 bps only.**2.** Use it with V_{DD} ≥ V_b.**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)**4.** Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

Notes 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} (2.4\text{ V}^{\text{Note 8}}) \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

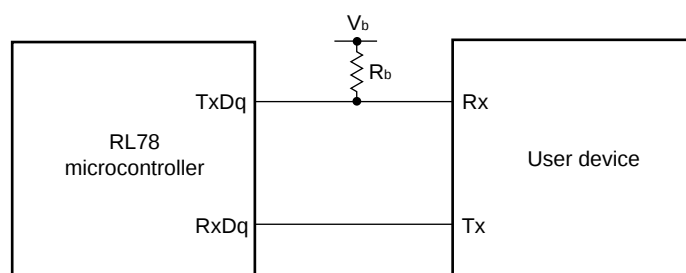
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.
8. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		200		1150		1150		ns
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		t _{KCY1} /2 – 120		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		121		479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOP output ^{Note 1}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130		130		130	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		23		110		110		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		33		110		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↑ to SOP output ^{Note 2}	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			10		10		10	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			10		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	20 MHz < f _{MCK}	12/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	20 MHz < f _{MCK}	16/f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}	20 MHz < f _{MCK}	36/f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	10/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		t _{KCY2} /2 – 12		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		t _{KCY2} /2 – 18		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		t _{KCY2} /2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 4}	t _{SIK2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 5}	t _{SI2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3}		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOP output ^{Note 6}	t _{KSO2}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573		2/f _{MCK} + 573		2/f _{MCK} + 573	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD13}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V _{LVD12}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVD11}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V _{LVD4}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD11}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V _{LVD10}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVD9}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVD8}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVD7}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVD6}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.6 Supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} rising slope	SV _{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	VL1	C1 to C4 ^{Note 1} = 0.47 μ F ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	VL2	C1 to C4 ^{Note 1} = 0.47 μ F	2 VL1 – 0.10	2 VL1	2 VL1	V	
Tripler output voltage	VL4	C1 to C4 ^{Note 1} = 0.47 μ F	3 VL1 – 0.15	3 VL1	3 VL1	V	
Reference voltage setup time ^{Note 2}	tVWAIT1		5			ms	
Voltage boost wait time ^{Note 3}	tVWAIT2	C1 to C4 ^{Note 1} = 0.47 μ F	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF ± 30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.8$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 and P61 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P20 to P27, P30 to P35, P40 to P47, P50 to P57, P60, P61, P70 to P77, P121 to P127, P130, P137	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI0, ANI1, ANI16 to ANI26	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF(+)} + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)} + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

3. Vss: Reference voltage

Absolute Maximum Ratings (2/3)

Parameter	Symbol	Conditions	Ratings	Unit
LCD voltage	V_{L1}	V_{L1} voltage ^{Note 1}	-0.3 to $+2.8$ and -0.3 to $V_{L4} + 0.3$	V
	V_{L2}	V_{L2} voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{L3}	V_{L3} voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{L4}	V_{L4} voltage ^{Note 1}	-0.3 to $+6.5$	V
	V_{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to $V_{L4} + 0.3$ ^{Note 2}	V
	V_{OUT}	COM0 to COM7 SEG0 to SEG50 output voltage	External resistance division method	-0.3 to $V_{DD} + 0.3$ ^{Note 2}
			Capacitor split method	-0.3 to $V_{DD} + 0.3$ ^{Note 2}
			Internal voltage boosting method	-0.3 to $V_{L4} + 0.3$ ^{Note 2}

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1} , V_{L2} , V_{L3} , and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor ($0.47 \mu\text{F} \pm 30\%$) and connect a capacitor ($0.47 \mu\text{F} \pm 30\%$) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS} : Reference voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
	V _{OH2}	P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
	V _{OL2}	P20 and P21	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V _{OL3}	P60 and P61	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the real-time clock 2 is included. The current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 6. The current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(TA = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} ^{Note 1}						0.20		μA
RTC2 operating current	I _{RTC} ^{Notes 1, 2, 3}	f _{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 2, 4}						0.04		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 2, 5}	f _{IL} = 15 kHz					0.22		μA
A/D converter operating current	I _{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V				1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V				0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} ^{Note 1}						75.0		μA
Temperature sensor operating current	I _{TMPS} ^{Note 1}						75.0		μA
LVD operating current	I _{LVD} ^{Notes 1, 7}						0.08		μA
Comparator operating current	I _{CMP} ^{Notes 1, 11}	V _{DD} = 5.0 V, Regulator output voltage = 2.1 V	Window mode				12.5		μA
			Comparator high-speed mode				6.5		μA
			Comparator low-speed mode				1.7		μA
		V _{DD} = 5.0 V, Regulator output voltage = 1.8 V	Window mode				8.0		μA
			Comparator high-speed mode				4.0		μA
			Comparator low-speed mode				1.3		μA
Self-programming operating current	I _{FSP} ^{Notes 1, 9}						2.00	12.20	mA
BGO operating current	I _{BGO} ^{Notes 1, 8}						2.00	12.20	mA
SNOOZE operating current	I _{SNOZ} ^{Note 1}	ADC operation	While the mode is shifting ^{Note 10}				0.50	0.60	mA
			During A/D conversion, in low voltage mode, AV _{REFP} = V _{DD} = 3.0 V				1.20	1.44	mA
		CSI/UART operation							0.70
LCD operating current	I _{LCD1} ^{Notes 1, 12, 13}	External resistance division method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 5.0 V, V _{L4} = 5.0 V		0.04	0.20.	μA
					V _{DD} = 3.0 V, V _{L4} = 3.0 V (V _{LCD} = 04H)		0.85	2.20	μA
	I _{LCD2} ^{Note 1, 12}	Internal voltage boosting method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices		V _{DD} = 5.0 V, V _{L4} = 5.1 V (V _{LCD} = 12H)		1.55	3.70
					I _{LCD3} ^{Note 1, 12}	Capacitor split method	f _{LCD} = f _{SUB} LCD clock = 128 Hz	1/3 bias, four time slices	V _{DD} = 3.0 V, V _{L4} = 3.0 V

(Notes and Remarks are listed on the next page.)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334 ^{Note 1}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500 ^{Note 1}		ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 76$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 3}	t_{KSI1}		38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}		50	ns

Notes 1. The value must also be equal to or more than $4/f_{CLK}$.**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**5.** C is the load capacitance of the SCKp and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM and POM numbers (g = 0, 1)**2.** f_{MCK} : Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02))

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$24/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$20/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$20\text{ MHz} < f_{MCK}$	$32/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$72/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$	ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$t_{KCY2}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$t_{KCY2}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$t_{KCY2}/2 - 100$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 2}	t_{SIK2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 3}	t_{KSI2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 4}	t_{KSO2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{MCK} + 240$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{MCK} + 1146$	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

3.6.3 Comparator

(T_A = -40 to $+105^\circ\text{C}$, 2.4 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		V _{DD} – 1.4	V
	Ivcmp		–0.3		V _{DD} + 0.3	V
Output delay	td	V _{DD} = 3.0 V Input slew rate > 50 mV/ μs	Comparator high-speed mode, standard mode		1.2	μs
			Comparator high-speed mode, window mode		2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0 μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode	0.66V _{DD}	0.76V _{DD}	0.86V _{DD}	V
Low-electric-potential reference voltage	VTW–	Comparator high-speed mode, window mode	0.14V _{DD}	0.24V _{DD}	0.34V _{DD}	V
Operation stabilization wait time	t _{CMP}		100			μs
Internal reference output voltage ^{Note}	V _{BGR}	2.4 V $\leq$ V _{DD} $\leq$ 5.5 V, HS (high-speed main) mode	1.38	1.45	1.50	V

Note Cannot be used in subsystem clock operation and STOP mode.

3.6.4 POR circuit characteristics

(T_A = -40 to $+105^\circ\text{C}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	When power supply rises	1.45	1.51	1.57	V
	V _{PDR}	When power supply falls	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset operation when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode and when the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset operation between when V_{DD} falls below 0.7 V and when V_{DD} rises to V_{POR} or higher.

