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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

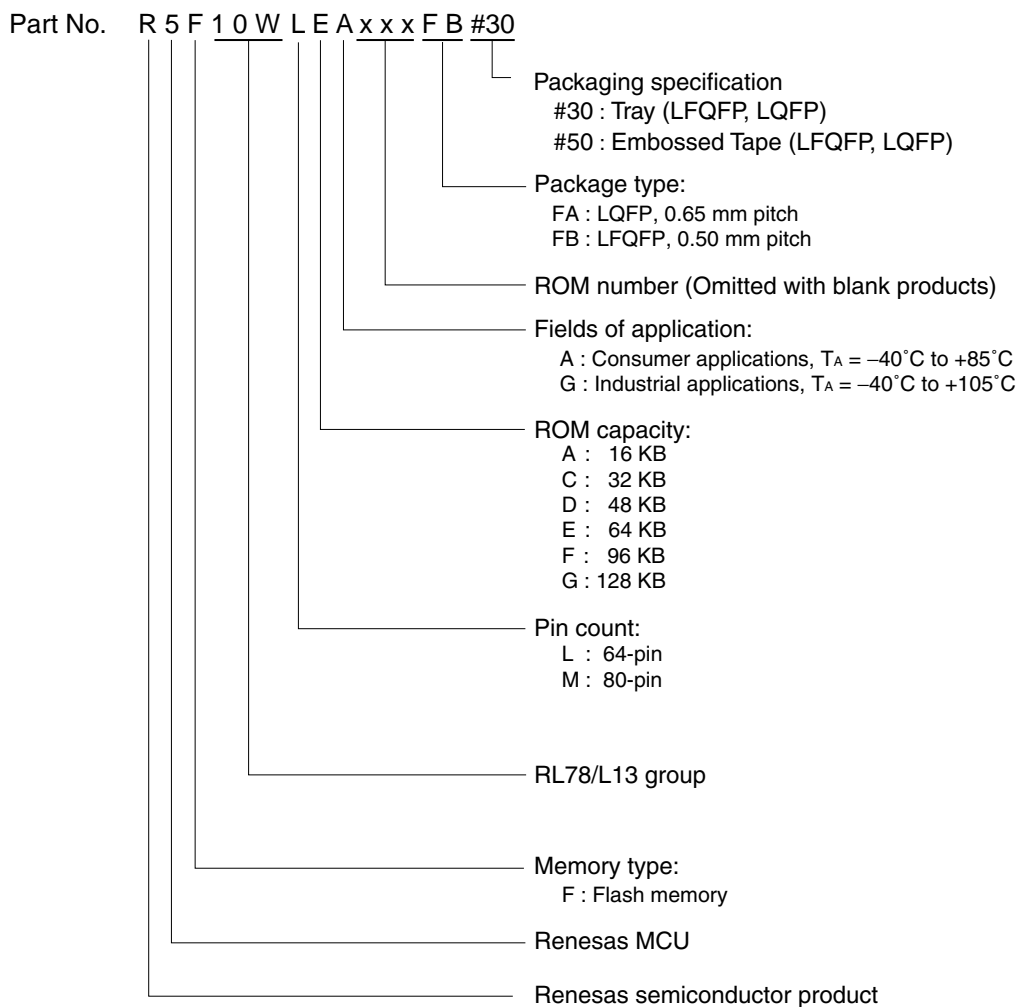
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10wmgafb-50

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/L13



Pin Count	Package	Data Flash	Fields of Application ^{Note}	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F10WLAAFA#30, R5F10WLAAFA#50, R5F10WLCAFA#30, R5F10WLCAFA#50, R5F10WLDAFA#30, R5F10WLDAFA#50, R5F10WLEAFA#30, R5F10WLEAFA#50, R5F10WLFAFA#30, R5F10WLFAFA#50, R5F10WLGAFB#30, R5F10WLGAFB#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A G	R5F10WLAAFB#30, R5F10WLAAFB#50, R5F10WLCAFB#30, R5F10WLCAFB#50, R5F10WLDAFB#30, R5F10WLDAFB#50, R5F10WLEAFB#30, R5F10WLEAFB#50, R5F10WLFAFB#30, R5F10WLFAFB#50, R5F10WLAGFB#30, R5F10WLAGFB#50, R5F10WLCGFB#30, R5F10WLCGFB#50, R5F10WLDGFB#30, R5F10WLDGFB#50, R5F10WLEGFB#30, R5F10WLEGFB#50, R5F10WLFGB#30, R5F10WLFGB#50, R5F10WLGGB#30, R5F10WLGGB#50
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F10WMAAFA#30, R5F10WMAAFA#50, R5F10WMCAFA#30, R5F10WMCAFA#50, R5F10WMDAFA#30, R5F10WMDAFA#50, R5F10WMEAFA#30, R5F10WMEAFA#50, R5F10WMFAFA#30, R5F10WMFAFA#50, R5F10WMGAFA#30, R5F10WMGAFA#50
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A G	R5F10WMAAFB#30, R5F10WMAAFB#50, R5F10WMCAFB#30, R5F10WMCAFB#50, R5F10WMDAFB#30, R5F10WMDAFB#50, R5F10WMEAFB#30, R5F10WMEAFB#50, R5F10WMFAFB#30, R5F10WMFAFB#50, R5F10WMGAFB#30, R5F10WMGAFB#50, R5F10WMAGFB#30, R5F10WMAGFB#50, R5F10WMCGB#30, R5F10WMCGB#50, R5F10WMDGFB#30, R5F10WMDGFB#50, R5F10WMEGFB#30, R5F10WMEGFB#50, R5F10WMFGFB#30, R5F10WMFGFB#50, R5F10WMGGFB#30, R5F10WMGGFB#50

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/L13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -10.0\text{ mA}$	$V_{DD} - 1.5$		V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$V_{DD} - 0.7$		V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$V_{DD} - 0.6$		V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$V_{DD} - 0.5$		V
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH1} = -1.0\text{ mA}$	$V_{DD} - 0.5$		V
	V_{OH2}	P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 20\text{ mA}$		1.3	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$, $I_{OL1} = 0.3\text{ mA}$		0.4	V
	V_{OL2}	P20 and P21	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V_{OL3}	P60 and P61	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$, $I_{OL3} = 1.0\text{ mA}$		0.4	V

Caution P00, P04 to P07, P16, P17, P35, P42 to P44, P46, P47, P53 to P56, and P130 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{DD}				1	μA
	I _{LH2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{DD}				1	μA
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port mode and when external clock is input			1	μA
				Resonator connected			10	μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{SS}				−1	μA
	I _{LIL2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{SS}				−1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port mode and when external clock is input			−1	μA
				Resonator connected			−10	μA
On-chip pull-up resistance	R _{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	V _I = V _{SS}	2.4 V ≤ V _{DD} < 5.5 V	10	20	100	kΩ
				1.6 V ≤ V _{DD} < 2.4 V	10	30	100	kΩ
	R _{U2}	P40 to P44	V _I = V _{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When setting ultra-low power consumption oscillation ($AMPHS1 = 1$). The current flowing into the LCD controller/driver, 16-bit timer KB20, real-time clock 2, 12-bit interval timer, and watchdog timer is not included.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Trans mission	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V)			2.8 ^{Note 2}		2.8 ^{Note 2}	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V)			1.2 ^{Note 4}		1.2 ^{Note 4}	Mbps
			1.8 V (2.4 V ^{Note 8}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate (C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V)			0.43 ^{Note 7}		0.43 ^{Note 7}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

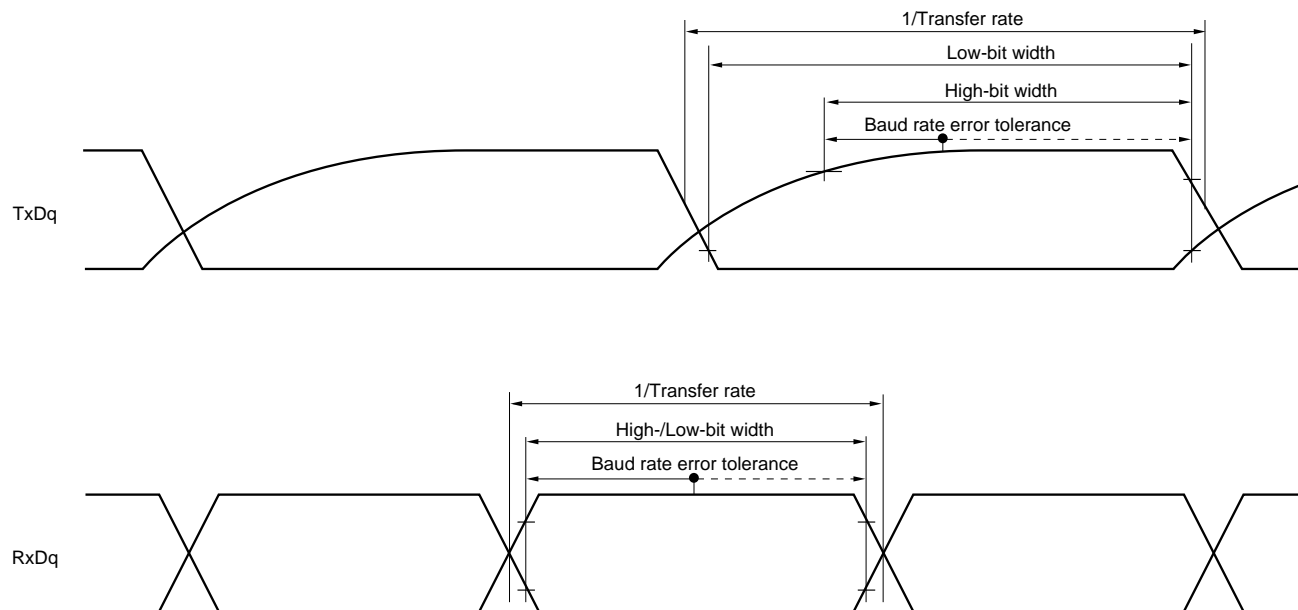
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.
- Use it with V_{DD} ≥ V_b.

UART mode bit width (during communication at different potential) (reference)

- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
- 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1550		1550		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1550		1550		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	1150		1550		1550		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1150		1550		1550		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	245		610		610		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	200		610		610		ns
		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	675		610		610		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	600		610		610		ns
		$1.8\text{ V} (2.4\text{ V}^{\text{Note 2}}) \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}^{\text{Note 3}}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	610		610		610		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		1/f _{MCK} + 190 ^{Note 4}		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V (2.4 V ^{Note 2}) ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Condition in HS (high-speed main) mode

3. Use it with V_{DD} ≥ V_b.4. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVD13}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V _{LVD12}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVD11}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V _{LVD4}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD11}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V _{LVD10}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVD9}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVD8}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVD7}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVD6}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVD4}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.6 Supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V _{DD} rising slope	SV _{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I _{LIH1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{DD}				1 μA
	I _{LIH2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{DD}				1 μA
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port mode and when external clock is input			1 μA
				Resonator connected			10 μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P40 to P47, P50 to P57, P70 to P77, P125 to P127, P130, P137	V _I = V _{SS}				−1 μA
	I _{LIL2}	P20 and P21, $\overline{\text{RESET}}$	V _I = V _{SS}				−1 μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port mode and when external clock is input			−1 μA
				Resonator connected			−10 μA
On-chip pull-up resistance	R _{U1}	P00 to P07, P10 to P17, P22 to P27, P30 to P35, P45 to P47, P50 to P57, P70 to P77, P125 to P127, P130	V _I = V _{SS}		10	20	100 kΩ
	R _{U2}	P40 to P44	V _I = V _{SS}		10	20	100 kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, comparator, I/O port, on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped.
When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the real-time clock 2 is included. The current flowing into the clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 6. The current flowing into the real-time clock 2, clock output/buzzer output, 12-bit interval timer, and watchdog timer is not included.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }24\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (48 MHz max.)
 3. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)
 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 5. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	334 ^{Note 1}		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	500 ^{Note 1}		ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 76$		ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{KSI1}		38		ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}		50	ns

Notes 1. The value must also be equal to or more than $4/f_{CLK}$.**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**5.** C is the load capacitance of the SCKp and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0), n: Channel number (n = 0, 2),
g: PIM and POM numbers (g = 0, 1)**2.** f_{MCK} : Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Reception			
		4.0 V $\leq V_{DD} \leq 5.5\text{ V}$, 2.7 V $\leq V_b \leq 4.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.7 V $\leq V_{DD} < 4.0\text{ V}$, 2.3 V $\leq V_b \leq 2.7\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps
		2.4 V $\leq V_{DD} < 3.3\text{ V}$, 1.6 V $\leq V_b \leq 2.0\text{ V}$		$f_{MCK}/12^{\text{Note}}$	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 24\text{ MHz}$, $f_{MCK} = f_{CLK}$		2.0	Mbps

Note Transfer rate in SNOOZE mode is 4800 bps only.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V \leq V _{DD} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V	Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 k Ω , V _b = 2.7 V	2.0 ^{Note 2}	Mbps
			2.7 V \leq V _{DD} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V	Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 k Ω , V _b = 2.3 V	1.2 ^{Note 4}	Mbps
			2.4 V \leq V _{DD} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V	Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 k Ω , V _b = 1.6 V	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V \leq V_{DD} \leq 5.5 V and 2.7 V \leq V_b \leq 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V \leq V_{DD} < 4.0 V and 2.3 V \leq V_b \leq 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

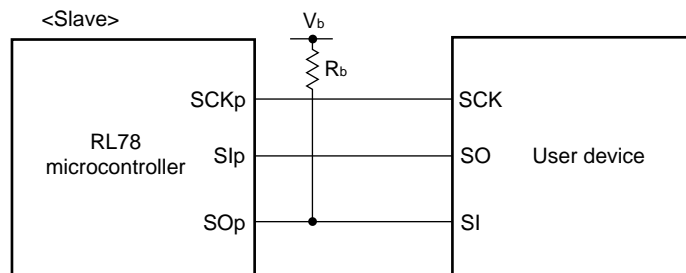
* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$24/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$20/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$20\text{ MHz} < f_{MCK}$	$32/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$28/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$24/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$12/f_{MCK}$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$20\text{ MHz} < f_{MCK}$	$72/f_{MCK}$	ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$64/f_{MCK}$	ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$52/f_{MCK}$	ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$32/f_{MCK}$	ns
			$f_{MCK} \leq 4\text{ MHz}$	$20/f_{MCK}$	ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$t_{KCY2}/2 - 24$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$t_{KCY2}/2 - 36$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$t_{KCY2}/2 - 100$		ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 40$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 60$		ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{HSI2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$1/f_{MCK} + 62$		ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$1/f_{MCK} + 62$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO2}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{MCK} + 240$	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{MCK} + 428$	ns
		$2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{MCK} + 1146$	ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

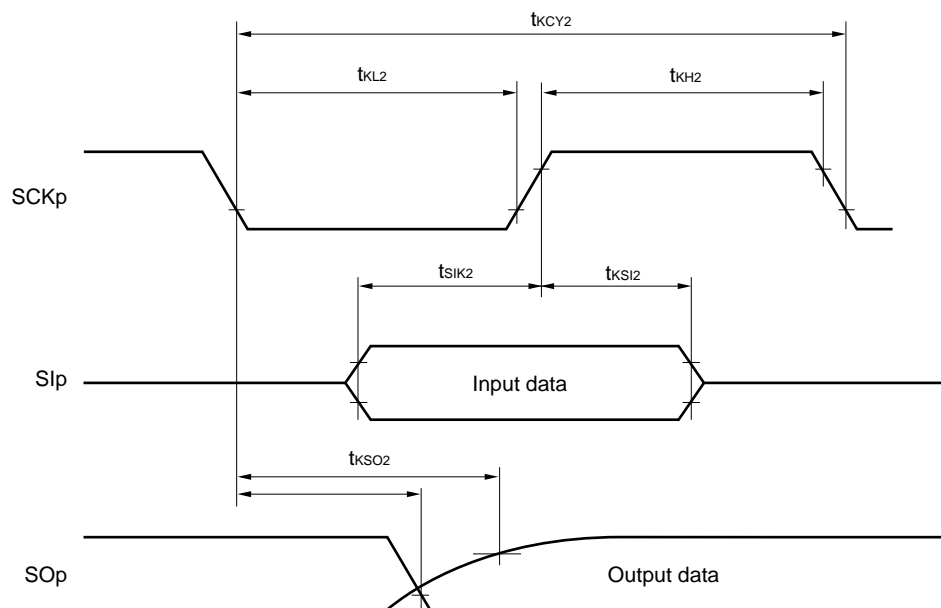
CSI mode connection diagram (during communication at different potential)

Notes 1. Transfer rate in SNOOZE mode: MAX. 1 Mbps

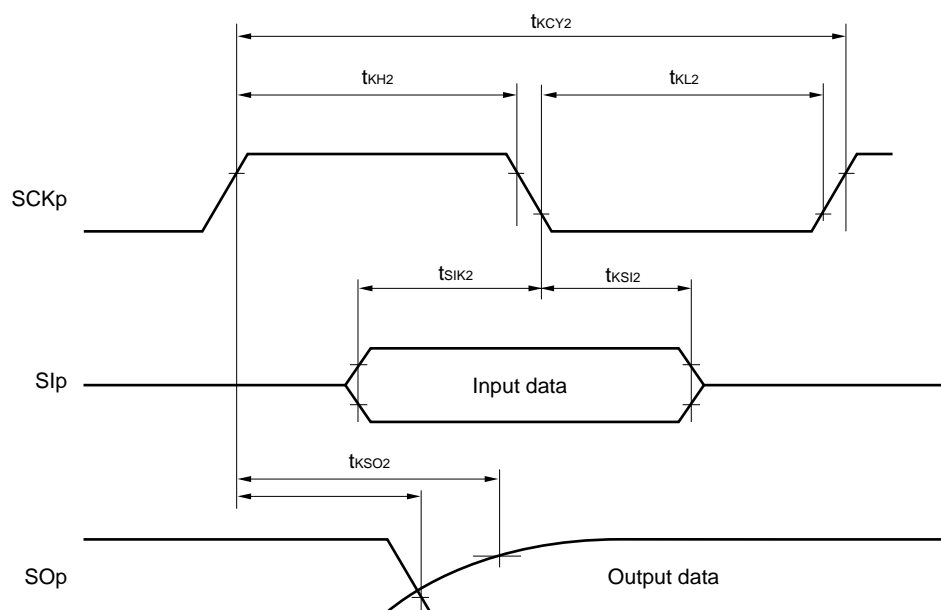
2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The SIp setup time becomes “to SCKp↓” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
3. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The SIp hold time becomes “from SCKp↓” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
4. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp↑” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[\text{F}]$: Communication line (SO_p) load capacitance, $V_b[\text{V}]$: Communication line voltage
- 2.** p: CSI number (p = 00, 10), m: Unit number, n: Channel number (mn = 00, 02), g: PIM and POM number (g = 0, 1)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn})
 m: Unit number, n: Channel number (mn = 00, 02))

(2) 1/4 bias method**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF ^{Note 2}	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} – 0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} – 0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} – 0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L3} and GNDC5: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = C5 = 0.47\ \mu\text{F} \pm 30\%$

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.7.3 Capacitor split method**(1) 1/3 bias method****($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_D \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = $0.47\ \mu\text{F}$ ^{Note 2}		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = $0.47\ \mu\text{F}$ ^{Note 2}	$\frac{2}{3} V_{L4} - 0.1$	$\frac{2}{3} V_{L4}$	$\frac{2}{3} V_{L4} + 0.1$	V
V_{L1} voltage	V_{L1}	C1 to C4 = $0.47\ \mu\text{F}$ ^{Note 2}	$\frac{1}{3} V_{L4} - 0.1$	$\frac{1}{3} V_{L4}$	$\frac{1}{3} V_{L4} + 0.1$	V
Capacitor split wait time ^{Note 1}	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GNDC3: A capacitor connected between V_{L2} and GNDC4: A capacitor connected between V_{L4} and GND $C1 = C2 = C3 = C4 = 0.47\ \mu\text{F} \pm 30\%$

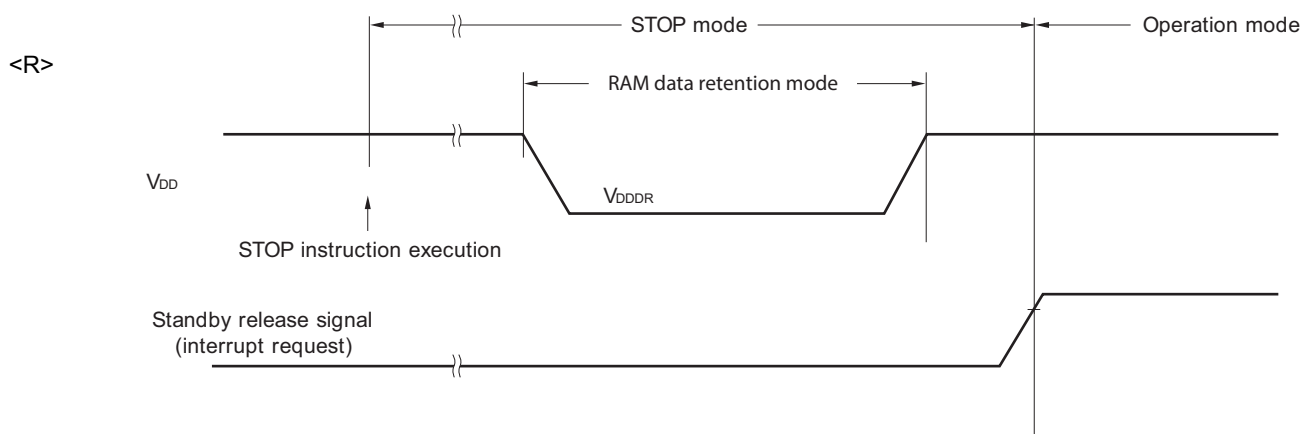
3.8 RAM Data Retention Characteristics

<R>

($T_A = -40$ to $+105^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

<R> **Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.9 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f _{CLK}	2.4 V ≤ V _{DD} ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Note 1, 2, 3}	C _{erwr}	Retained for 20 years T _A = 85°C ^{Note 4}	1,000			Times
Number of data flash rewrites ^{Note 1, 2, 3}		Retained for 1 year T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C ^{Note 4}	100,000			
		Retained for 20 years T _A = 85°C ^{Note 4}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. This temperature is the average value at which data are retained.

Remark When updating data multiple times, use the flash memory as one for updating data.

3.10 Dedicated Flash Memory Programmer Communication (UART)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps